Design, testing, and modeling of radio frequency and digital circuits using metal-ferroelectric-semiconductor field-effect transistors

Mitchell Ryan Hunt
DESIGN, TESTING, AND MODELING OF RADIO FREQUENCY AND DIGITAL CIRCUITS USING METAL-FERROELECTRIC-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

by

MITCHELL RYAN HUNT

A DISSERTATION

Submitted in partial fulfillment of the requirements for the degree of Doctorate of Science in Engineering in The Department of Electrical and Computer Engineering to The School of Graduate Studies of The University of Alabama in Huntsville

HUNTSVILLE, ALABAMA

2020
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We, the undersigned members of the Graduate Faculty of The University of Alabama in Huntsville, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering.

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ABSTRACT
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In this dissertation, a novel device, the ferroelectric transistor, is studied, modeled, and applied to various circuit designs. Empirical data of several devices are presented alongside the theory behind the device operation. This theoretical understanding of the device is then used as the basis for a physically derived model, which is shown to agree with the experimental collected data. Lastly, these new devices are applied to several circuit designs ranging from digital to radio frequency and new operation of these circuits developed to highlight the unique and interesting features afforded by the addition of a ferroelectric layer.

The primary focus of this work is the physically derived model, which computes the polarization of the ferroelectric material and resulting current in the semiconductor channel as a function of the applied electric field and polarization state. Limited use of empirically defined constants is employed, resulting in strong agreement with the current hysteresis with varying gate voltage with very little reliance on fabricated devices. The basis for a polarization retention model is also presented.

Since ferroelectric devices are rarely available, experimental data collected to characterize the devices are presented and highlight the unique features of these novel transistors. Additionally, experimental data of the devices applied to radio frequency and digital circuits are presented. With the use of these ferroelectric transistors, new
operation of the circuits is defined. In the ring oscillator, the ferroelectric material polarization is used as an additional tuning mechanism, resulting in increased operation frequency range. In digital circuits, the nonvolatile retention of the ferroelectric material is used as an additional storage device, and the variable conductivity of the channel gives rise to new operational modes. Most notable is the capability to store an additional data bit in the 1T1C memory cell.
ACKNOWLEDGEMENTS

First, I would like to acknowledge my advisor Dr. Fat Duen Ho for his continued guidance and help since we started working together in the spring of 2009. His classes and instruction gave me the foundation needed to complete this body of work, and his ideas and analytical approach provided the inspiration for all of the topics discussed in this dissertation. Countless hours of mentorship by Dr. Ho have given me the background, direction, and motivation to expand my knowledge in electrical engineering and physics, continue researching new electronic devices, and ultimately complete this dissertation. I will forever be grateful his enthusiasm, advice, and willingness to help me with any and every issue that I encountered.

Several graduate students, present and former, have helped me design, build, test, analyze, and model FeFETs and circuits using them. In particular, Dr. Rana Sayyah, Mr. Cody Mitchell, Ms. Crystal Laws, and Mr. Todd MacLeod have all been instrumental to my success, and I am deeply thankful to them for their help. Dr. Sayyah and Mr. MacLeod helped me work on many analog circuits, both design and modeling as well as device characterization. We have spent many hours in the lab collecting and re-collecting data, especially remnant tests, and I would have been lost without their help and guidance. Mr. Mitchell and Ms. Laws have helped design and test various digital and radio frequency circuits. Much of the analysis and ideas presented in this work were the byproduct of numerous, late hours in the lab troubleshooting circuit designs and reviewing data.

I would also like to acknowledge Joe Evans at Radiant Technologies for supplying all of the transistors used for device characterization and circuit design and
testing in addition to his guidance on the device operation. His novel components formed
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Without his continued support of our research, insight into the transistors, and effort
developing and providing additional transistors, this research would not have been
possible.

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allowed me to perform the research necessary to complete this dissertation.
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<tr>
<td>$\varepsilon_r$</td>
<td>Relative permittivity</td>
</tr>
<tr>
<td>$a$</td>
<td>Lattice parameter, typically along $x$-axis; acceleration</td>
</tr>
<tr>
<td>$b$</td>
<td>Lattice parameter, typically along $y$-axis</td>
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<tr>
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\( \sigma \) Surface charge density

\( i \) Square root of negative one

\( h \) Reduced Planck constant

\( \psi \) Wave function

\( \varphi \) Time component of the wave function

\( \psi \) Spatial component of the wave function

\( m \) Mass

\( \nabla \) Del operator

\( g_m \) Transconductance

\( i_{DS} \) Combined AC and DC drain-to-source current

\( v_{GS} \) Combined AC and DC gate-to-source voltage

\( V_{th} \) Transistor threshold voltage

\( C_{GS} \) Transistor gate-to-source capacitance

\( Q_S \) Charge exiting transistor source terminal

\( k_2 \) Spring constant (\( x^2 \) term)

\( k_4 \) Spring constant (\( x^4 \) term)

\( \lambda \) Lattice parameter

\( B \) Magnetic flux density

\( \Delta x \) Numerical derivative spatial step

\( \Delta t \) Numerical derivative time step

\( \gamma \) Crystal distortion ratio

\( J \) Current density

\( \phi \) Unnormalized wave function
\( \rho \)  Charge density; resistivity
\( x_n \)  Depletion region extent into n-type material
\( x_p \)  Depletion region extent into p-type material
\( \epsilon_a \)  Permittivity of acceptor material
\( \epsilon_d \)  Permittivity of donor material; Lennard-Jones potential well-depth
\( I \)  Current
\( e \)  Elementary charge
\( \mu \)  Carrier mobility
\( V_{DS} \)  DC drain-to-source voltage
\( W \)  Transistor channel width
\( L \)  Transistor channel length
\( T_S \)  Semiconductor thickness
\( R \)  Resistance
\( v_G \)  Combined AC and DC gate voltage
\( v_{GS} \)  Combined AC and DC gate-to-source voltage
\( v_{SG} \)  Combined AC and DC source-to-gate voltage
\( i_{DS} \)  Combined AC and DC drain-to-source current
\( A \)  Lennard-Jones potential repulsive coefficient
\( B \)  Lennard-Jones potential attractive coefficient
\( r_m \)  Lennard-Jones potential minimum radius

\( C_{store} \)  Storage capacitor
\( C_{sense} \)  Read cycle sense capacitor
\( V_x \)  Storage capacitor voltage
\( V_{DD} \)  Positive supply voltage
\(-V_{SS} \)  Negative supply voltage
\( f \)  Frequency
\( P_{avg} \)  Average power
\( C_{load} \)  CMOS inverter load capacitance
\( V_{OL} \)  CMOS inverter low output voltage maximum
\( V_{IH} \)  CMOS inverter high input voltage minimum
\( Q_n \)  N-type MOSFET
\( Q_p \)  P-type MOSFET
\( Q_F \)  Metal-ferroelectric-semiconductor field-effect transistor
\( t_{on} \)  Time spent "on" over the course of a single period
\( T \)  Period
\( D \)  Duty cycle
\( V_{Bias} \)  Voltage source used to bias the voltage-controlled oscillator
CHAPTER I

INTRODUCTION

In 1920, Joseph Valasek discovered ferroelectricity in Rochelle salt, first termed “piezoelectricity and allied phenomenon” [1]. Many more ferroelectric materials were discovered in the following decades. One of the most widely used ferroelectric materials, barium titanate (BaTiO₃), was discovered in 1941 [2]. Interest in barium titanate was spurred by World War II, which was still on-going. Since the new ferroelectric material was able to demonstrate high dielectric constants (approximately, \( \varepsilon_r = 1000 \)), it was soon incorporated into capacitors both during the war and after it ended [3]. Interest in lead zirconate titanate (PZT, PbZrₓTi₁₋ₓO₃) began in the 1950s stemming from previous work with lead titanate (PT, PbTiO₃) [4]. Early measurements noted high Curie temperature of PZT, which stemmed from the lead zirconate (PZ, PbZrO₃) addition [5, 6]. Later studies of the materials presented strong piezoelectric responses, especially at the 52/48 mole fraction (PbZr₀.₅₂Ti₀.₄₈O₃) [4]. These properties allowed PZT to see much use in transducers as well as capacitors since its discovery [3, 7].

With the successful fabrication of metal-oxide-semiconductor field-effect transistors (MOSFETs) beginning in the early 1960s, the ease of fabrication and use in integrated circuits spurred interest in the new devices [8]. Though ferroelectric materials saw use in devices such as capacitors, with PZT seeing research in the 1950s, it was Joe
Evans Jr., now at Radiant Technologies, Inc., who first incorporated PZT into the capacitor and later transistor designs [9]. Being among the early innovators in the field beginning even before 1984, Mr. Evans began successfully incorporating ferroelectric materials into devices through various fabrication methodologies [9]. Through his continued work in the field, he developed the first integrated PZT capacitor in 1984 while at his earlier company Krystalis [9]. The next year the first PZT capacitor showing a promising electrical response was first fabricated [9]. Following initial work with capacitors, in May of 1987 he went on to build the first ferroelectric random-access memory (FRAM or FeRAM) on complementary metal-oxide semiconductor (CMOS) [9]. Over the years, he has continued to refine and develop manufacturing techniques and is the sole supplier of ferroelectric field-effect transistors (FeFETs) used in support of this work.

Ferroelectrics continued to see use in devices such as capacitors. While transistors including a ferroelectric layer at the gate terminal, either in addition to or as a replacement for the oxide layer, are popular in literature extending the MOSFET to the FeFET or metal-ferroelectric-semiconductor field-effect transistor (MFSFET), empirical results of these devices as standalone devices are scarce when present at all [10, 11, 12, 13, 14, 15, 16, 17, 18]. Moreover, literature concerning FeFETs is generally limited to device characterization and does not explore uses of the unique transistors in other circuits or applications where further advantages may be realized [19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54].
The radiation hardened nature of these devices lends them to uses in space applications where ionizing radiation is seen to damage or upset electronics [55, 56, 57, 58, 59]. When confronted with the challenges of spacecraft design, most semiconductor devices are susceptible to damaging or performance degrading effects of radiation, the effects of which are observable even in low-earth orbit (LEO) [60, 61]. However, in devices containing lead-based ferroelectrics, including the devices of interest in this dissertation, lead ions help mitigate much of the incident radiation due to the high density and atomic number [62, 63]. Advantages resulting from the radiation hardened nature of these components have already been shown experimentally using the Fast, Affordable, Science and Technology SATellite (FASTSAT) microsatellite flown by NASA over a period of two years [58, 59, 64]. Despite the success experienced with the FASTSAT satellite, current commercial ferroelectric devices and manufacturing are often limited to FRAM, such as those available on Texas Instruments microcontrollers or manufactured by Fujitsu [65, 66]. Due to challenges faced in transistor manufacturing, most FRAM devices use ferroelectric capacitors, or capacitors with a ferroelectric layer in place of or in addition to the dielectric layer, as the ferroelectric devices in circuit designs and retain any transistors in the design. However, the ferroelectric transistor is able to find additional uses as a device, such as potentially being used as the next generation of transistors in the wake of ever decreasing circuit size and supply voltages [67].

Recently, as a result of the ever-decreasing size of integrated circuits other research focal areas are concerned with examining the possibility of ferroelectric transistors exhibiting subthreshold swings less than 60 mV/dec [67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77]. As outlined in recent work, three areas exhibit promising results to
circumvent this constraint, of which ferroelectric transistors are one [67]. Other areas, such as tunnel-FETs or impact ionization MOS (IMOS) transistors, work to excite larger changes in current stemming from adjusting the channel or transport mechanisms [67]. However, the ferroelectric transistor, which is included in the negative capacitance class of devices, works to impart more substantial variation in the channel resulting from the same gate voltage, much in a way similar to suspended gate FET (SG-FETs) [67]. It is for this reason – that ferroelectrics are a key component in what may be the next generation of semiconductor devices – in addition to the ability to operate in radiated environments that makes the ferroelectric transistor, which is the focus of this work, so important that ferroelectrics. Due to physical constraints when using the MOSFET structure, 65 mV/dec is the approximate limit for a varying gate voltage to affect a decade change (10×) in subthreshold current, or current observed below the threshold voltage [78]. By decreasing this value, smaller supply voltages can be used, which directly affect the power dissipation, heating, and speed of the device. To accomplish this extraordinary feat, the ferroelectric layer is viewed as a capacitor with negative capacitance since the polarization can be theorized to align in a way that serves to add to the applied gate voltage [69]. The ferroelectric layer can increase the effective gate voltage seen at the channel, and in this manner, a small gate voltage variation introduces a large change in drain current typically seen with larger gate voltages due to the increased effects at the channel [67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77]. Unfortunately, the possible benefits afforded by the ferroelectric layer through negative capacitance are only seen in the MOSFET configuration. Though not expected to be observable in the particular FeFETs used in this research, previous data has been
presented that shows what is thought to be a purely transient negative capacitive response due to the polarization switching.

Piezoelectric materials, of which ferroelectric materials are a part, are also a topic of interest for research in the field of energy harvesting. Using the material property of generating an electric charge under physical strain allows vibration or applied pressure to capture ambient or sensed energy. Low power devices are sometimes able to operate without an external power source, making piezoelectric materials crucial in distributed and wireless sensor layouts. Since ferroelectric materials also exhibit a piezoelectric response to physical stress and strain, devices incorporating these materials may be used to generate voltages in circuits. For transistors with a structure similar to that of the transistors manufactured by Radiant Technologies, Inc., the voltage across the ferroelectric layer often manifests as an additional voltage, of varying polarity and magnitude, applied at the gate. Commercially available integrated sensors have been created using ferroelectric capacitors by taking advantage of this phenomenon. However, transistors containing ferroelectric material have not yet been used in this field.

Given the use of ferroelectrics and the increasing interest in ferroelectric devices for a variety of applications, models of ferroelectric materials and devices including the materials are also increasing in importance. Earlier physically derived models of the ferroelectric transistor examined the polarization of the ferroelectric layer and even considered variation in polarization across the layer or channel along with the effects imparted on the semiconductor potential [16, 17, 40, 41, 53, 81, 82]. Due to the piezoelectric response of ferroelectrics, which is often used for energy harvesting, much research and modeling efforts examine the piezoelectric response of materials, or the
relationship between structural deformation and electrostatic potential [83, 84, 85, 86, 87, 88, 89].

Ferroelectric devices see use in many fields, ranging from energy storage, data storage, and energy capture, to operation in radiated environments. However, experimental data detailing the performance of ferroelectric devices, especially when operating in circuits, is still scarce when available at all [23, 27, 29, 30, 32, 35, 36, 39, 45]. The research contained in this dissertation provides experimental data demonstrating FeFET operation by examining the isolated device and the performance of the device in various circuits that show capabilities not seen with other devices. This was accomplished by first characterizing the transistor through measurements made using an isolated device and determining the unique, useful features afforded to the transistor by the addition of PZT. The FeFET was incorporated in existing circuit designs, and the designs modified where necessary to exemplify the unique features. To aid in ferroelectric device development beyond the FeFET as well as circuit design using the FeFET, a model of the transistor was created that uses the electrical response of the ferroelectric layer and its impact on the semiconductor channel to accurately compute the channel current. The polarization of the ferroelectric layer was calculated using the gate, drain, and source terminal voltages, and the polarization in turn used to determine the channel potential and semiconductor depletion region. With the channel potential and ferroelectric state known, the current over time is then calculated. Since ferroelectric materials are seen most in non-volatile applications such as memory devices, the model incorporates a time evolution of the polarization to show retention properties. Using the structure of the crystal, the potential computation in the unit cell considers spatial
constraints specific to each ion along with their interactions. Given the applied potential, the polarization state of the ferroelectric layer is found by way of determining ion displacements. Empirical data collected using the specific FeFETs of interest is also provided as a significant contribution to the field, which helps to influence circuit designs and modifications to accommodate the FeFETs better. Also useful are the current and polarization model of the transistors based on first principles as shown for the presented ferroelectric transistor model.

While the majority of transistors containing ferroelectric materials discussed in literature have a structure similar to a MOSFET, the FeFETs made available by Joe Evans at Radiant Technologies, Inc. have a unique configuration similar to that of a thin film transistor (TFT) or junction field-effect transistor (JFET) [90]. Currently there is no known commercial source of fabricated ferroelectric transistors using the MOSFET structure, and only Radiant Technologies, Inc. FeFETs using the TFT or JFET structure are available, though still especially rare due to manufacturing difficulties. Resulting from the lack of physical devices and testing, little empirical data exists in the field currently. Therefore, characterization and developing a source of referent data using these devices is the first part of this work. Next the design and implementation of new or modified concepts using these devices is explored, as it demonstrates device capabilities in never before considered areas where unrealized advantages of the devices may be uncovered. Lastly, a physics-based model of the devices is developed and shown to accurately demonstrate the FeFET operation as a standalone device and in circuits.
CHAPTER II

FEFET DEVICE PROPERTIES AND OPERATION

In this dissertation the devices of interest are the FeFETs fabricated and provided by Joe Evans, Jr. at Radiant Technologies, Inc. The particular FeFETs provided by Radiant Technologies, Inc. have platinum contacts at each of the three device terminals (source, drain, and gate). Within these transistors, a 350 nm ferroelectric layer of 20/80 lead zirconate titanate (PZT, PbZr\textsubscript{0.2}Ti\textsubscript{0.8}O\textsubscript{3}) is located between the gate contact and semiconducting channel, which is composed of a 20 to 40 nm film of indium oxide (InO\textsubscript{x}, In\textsubscript{2}O\textsubscript{3}). Similar to a JFET structure, both source and drain terminal contacts are positioned opposite the gate contact, extending to and enveloping the sides of the indium oxide channel as shown in Figure 2.1. Unlike typical MOSFET structures, the substrate is not electrically significant and instead only provides the surface on which the transistors were fabricated. As such, no electrical connection is made to the substrate, which was composed of glass. The width and length dimensions of the device vary for each device model, of which there are five available, as indicated in Table 2.1.
Due to how reactive PZT is with silicon, indium oxide is instead used as the semiconductor composing the channel. Additionally, in order to seal the device from the environment and discourage further reactions, a layer of dielectric material is placed around the entire transistor as shown in Figure 2.2. This particular structure, combined with the device packaging, though prolonging the lifespan of the devices and creating an overall more robust design incidentally precludes piezoelectric response measurements.

![Figure 2.1: FeFET general structure with all contacts constructed using platinum and glass used as the substrate (not electrically significant)](image)

Table 2.1: FeFET channel dimensions and gate area

<table>
<thead>
<tr>
<th>Model</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
<th>Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ND1</td>
<td>10</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>ND4</td>
<td>40</td>
<td>40</td>
<td>1600</td>
</tr>
<tr>
<td>ND7</td>
<td>400</td>
<td>4</td>
<td>1600</td>
</tr>
<tr>
<td>ND9</td>
<td>500</td>
<td>5</td>
<td>2500</td>
</tr>
<tr>
<td>ND10</td>
<td>2500</td>
<td>5</td>
<td>12500</td>
</tr>
</tbody>
</table>
When analyzing the ferroelectric transistor, device operation is separated into ferroelectric material and semiconductor operation. Separation of these two types of materials allows analysis and appreciation of ferroelectric material specific properties prior to introduction of the three terminal device physics. This division mirrors the approach taken regarding the device model, which incorporates both a ferroelectric and semiconductor model that interact with one another as discussed in detail in chapter III.

A. Ferroelectric Material

The unique properties of ferroelectric materials are what set FeFETs apart from other transistors that are commonly used, such as MOSFETs. By incorporating ferroelectric materials into transistors, these unique properties also allow FeFETs to have
advantages over other transistors that make the addition of FeFETs to some designs quite attractive. Notable recent interest in use of ferroelectric materials in transistors stems primarily from the possibility of creating transistors capable of switching more quickly than the MOSFET, which would be an important advantage in circuits [75, 77]. Key features of a ferroelectric material that are particularly enticing for modern electronics include electric polarizability, nonvolatile retention of the polarization state, piezoelectric response, and temperature dependence of both the polarization and retention. Of these aspects, electric polarization and non-volatile retention of the polarization state are the most widely used for electronic devices incorporating ferroelectrics, which are primarily seen in non-volatile memory devices. In this dissertation, each of these aspects of the ferroelectric material are considered for modeling and various applications to differing degrees.

(i) Structure

The structure and composition of ferroelectric materials are what provide the polarization that is often sought after. Since lead zirconate titanate is used in transistors of interest in this dissertation, the discussion of material structure is tailored to this material in particular. However, other perovskite materials, such as barium titanate or barium strontium titanate, are also popular and possess the same structure. For these similar materials, the ionic charge and bond lengths will change slightly but the overall performance remains constant. In PZT in particular, the crystal takes on the well-known perovskite structure, which has one of the simplest of the known ferroelectric unit cells, as indicated in Figure 2.3. The unit cell contains the complete composition of the material as it is a small repeatable block of the structure.
In Figure 2.3, the thermally averaged unit cell is shown, which results in a cubic structure. In the cubic phase, each side of the cube has length $a$ ($a = b = c$ with $90^\circ$ angles formed between each side for cubic structure), which is approximately 4 Å.

However, as the unit cell lowers in temperature, as indicated by Figure 2.4, a tetragonal phase is induced for the 80% PT composite material. At temperatures below the Curie temperature, the 20/80 PZT unit cell is tetragonal at room temperature, as indicated by both Figure 2.4 and Figure 2.5. In this state, the cations displace relative to the oxygen cage with displacements shown in Table 2.2 when an electric field is applied across the material [94, 95]. In this scenario, which will be the primary interest in this body of work as circuit operation will typically be conducted at room temperature, the angles between each side are maintained as right angles but the crystal distorts, elongating along the $c$ direction indicated in Figure 2.6. In this phase, the $c$ direction elongates to
approximately 4.135 Å while the $a$ and $b$ lattice parameters are both approximately 3.9135 Å.

Figure 2.4: Phase transition for varying PZT composition and temperature reprinted with permission

Figure 2.5: PZT lattice parameters for varying PZ and PT composition reprinted with permission
Table 2.2: Lead titanate (PbTiO₃) ion displacements along the c-axis expressed as a fraction of the total tetragonal lattice parameter c in Ångströms

<table>
<thead>
<tr>
<th>Ion</th>
<th>Relative to c parameter</th>
<th>Ion Displacement (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb²⁺</td>
<td>0.11</td>
<td>0.46</td>
</tr>
<tr>
<td>Ti⁴⁺</td>
<td>0.07</td>
<td>0.29</td>
</tr>
<tr>
<td>O²⁻</td>
<td>0.00</td>
<td>0.00</td>
</tr>
</tbody>
</table>

Figure 2.6: Crystal structure with arbitrary dimensions and angles

As shown in Figure 2.7, the lead ions, Pb²⁺, at each unit cell corner each contribute 1/8 of an ion to the unit cell, resulting in a single lead ion within the cell. Similarly, the oxygen ions, O²⁻, on each face each contribute half of an ion, resulting in three oxygen ions inside the unit cell. The central ion, either zirconium (Zr⁴⁺) or titanium (Ti⁴⁺), is wholly inside the unit cell. As a result, the formula for PZT is expressed as PbZr₀.₂Ti₀.₈O₃. In these samples, owing to the 20/80 description of the compound, 20% of the unit cells are PZ with the remaining 80% of unit cells consisting of PT. The composite material of PZT allows properties of PZ and PT to be observed to varying degrees based on the percent composition of each material.
Figure 2.7: Lead zirconate titanate unit cell showing only the fractions of each ion contributing to the unit cell composition. At each corner lies $\frac{1}{8}$ of a $\text{Pb}^{2+}$ ion, contributing an overall single ion per unit cell. Likewise, the central ion ($\text{Zr}^{4+}$ or $\text{Ti}^{4+}$) located at the center of the unit cell contributes a single ion per unit cell. Each unit cell face contains half of an $\text{O}^{2-}$ ion, resulting in three ions being present in a single unit cell.

In perovskites, displacement of the central, positively charged ion is the largest single contributor to the overall dipole moment of each unit cell. The resulting overall dipole moment of the unit cell due to ion displacements, which for PZT has contributions from each lead, oxygen, zirconium, and titanium ion, forms the electric polarization that is typically sought after when using ferroelectrics. The polarization, which is electric in nature and often abbreviated as simply the polarization, is induced with either an applied electric field, stress, or combination thereof.

Within the ferroelectric material, unit cells tend to polarize similarly in groups of adjacent cells called domains. Size of the domain is related to the direction and intensity of the electric field in addition to the polarization within the domain. Domain size tends
to grow for domains with polarization opposing the electric field as the intensity is increased. Conversely, domains orthogonal to the electric field direction tend to shrink as the electric field intensity increases. This trend is due to the fact that larger electric fields more strongly polarize the material, causing more unit cells to take on a common electric dipole moment. For large electric fields, which is dependent on material to prevent crystal damage, the polarization becomes saturated, that is the maximum allowed number of dipoles have switched to align with the applied electric field. At this point the size of the domains is greatest or the overall volume corresponding to a similarly polarized domain is at a maximum, owing to the fact that the maximum number of unit cells have displaced in a similar fashion. This trend is illustrated in Figure 2.8 for an electric field varying between 550, 705, and 980 V/cm. Of note here is the fact that the regions of common dipole alignment or direction are the ferroelectric equivalent of Weiss domains in ferromagnetic materials. Though originally discovered long ago, the domain structure was not well explained until 1928 when Heisenberg was able to describe the phenomenon using quantum mechanics [96, 97].

Figure 2.8: Ferroelectric domain size under increasing electric field intensity (increasing electric field intensity from left to right) reprinted with permission
(ii) Polarization

Electric polarization is produced by two principal methods for ferroelectric materials, a combination of applied electric field and mechanical stress on the material. Principally for applications in electric circuits to date, the polarization is set using an applied electric field, usually via a voltage determined by other circuits or circuit elements. However, since ferroelectric materials are also piezoelectric several applications harness the stress induced polarization for sensors or energy harvesting [80, 83, 84, 85, 86, 87, 88, 89, 98]. Polarization stimulated by an applied electric field is essentially governed by the electric susceptibility owing to the interatomic potentials, though here the susceptibility must be considered a nonlinear function with respect to applied electric field, much unlike an isotropic linear material. Similarly, the piezoelectric response of the material dictates the stress induced polarization.

(a) Electric Field Induced Polarization

The electrical response of the 20/80 PZT, and all ferroelectric materials, shows a history dependence on the applied electric field as demonstrated by the hysteresis in Figure 2.9. Alternatively stated, the polarization is not uniquely defined by the currently applied electric field. Instead, the previously applied electric fields determine the present state of the ferroelectric material and therefore the response to the applied electric field. It is this history dependence that has allowed ferroelectrics to see use in memory applications. Much of the early work surrounding incorporating ferroelectric materials in circuits did so as a memory device by using the hysteresis to store information [100, 101, 102].
Beginning at the origin \((O)\), the initial or virgin polarization curve defines the transition from the initial condition of the polarization, which is indicated to possess no appreciable polarization initially. As the applied electric field increases a transition to the positively poled state occurs. At this point the polarization is saturated, and the change of polarization with respect to applied electric field, \(dP/dE\), shifts. Polarization saturation occurs when the ferroelectric material is no longer capable of further ion displacements due to extent of the crystal distortions allowed. At this point, the polarization curve with respect to applied electric field is diminished and the material acts as a dielectric. Each hysteresis edge shows the transition between the two states of complete polarization, or maximum magnitude polarization given the intensities of the applied electric field. The direction of the transition is indicated by the arrows, revealing the history dependence of the polarization having different paths depending on the initial state. Smaller electric fields may not yield polarization saturation, which results in a hysteresis curve without the tapered edges shown in Figure 2.9. To determine accurately if a material is ferroelectric, measurements indicating polarization saturation are required. Depending
on the measurement frequency and material under test, it is possible to produce a hysteresis curve that never saturates and may be mistaken for ferroelectric materials [103, 104, 105].

The principal defining factor of the polarization in ferroelectric materials is the hysteresis showing remnant polarization and ideally polarization saturation, as shown in Figure 2.9. Similar to ferromagnetic materials, small electric fields applied across the ferroelectric material will result in a near-linear response. However, as the electric field strength is increased the non-linear response of the ferroelectric material is revealed. Of note is the parallel between the ferroelectric materials and ferromagnetic materials. If, for example, the electric field, $E$, is exchanged for the magnetic field, $H$, and polarization, $P$, changed to magnetization, $M$, in Figure 2.9, the result is the well-established ferromagnetic hysteresis loop [99, 106]. Properties for ferromagnetic materials analogous to ferroelectric materials can be observed from the general hysteresis. For example, the width of the hysteresis is formed as result of the polarization or magnetization requiring sufficient energy to reverse the current state. As a result, the shift in either induced quantity is gradual initially until the magnitude of the slope increases.

In general, for simple dielectric materials the dielectric displacement or simply displacement, $D$, is proportional to the electric field, $E$, as shown in Equation (2.1).

$$D = \varepsilon E \quad (2.1)$$

For these materials, the polarization is assumed to be directly proportional to the electric field, expanding the dielectric constant, $\varepsilon$, as shown in Equation (2.2).

$$D = (1 + 4\pi\chi_e)E \quad (2.2)$$
The electric susceptibility, $\chi_e$, term in the dielectric constant arises from the fact that the polarization is directly related to the electric field by this parameter. Values for the electric susceptibility depend on the arrangement of ions in the material where the local or internal electric field defines the electric field acting on a particular ion relative to other ions or molecules in the material.

In ferroelectric materials, however, the local field at each ion site is dependent on the surrounding ions and their specific dipole moments. For similar dipole moments, the local field can be assumed to take on a simple numeric scale factor to simplify the dielectric constant. An example of this is the often-used dielectric constant expression for $N_i$ ions having a combined electronic and ionic polarizability of $\alpha_i$, as shown in Equation (2.3).

$$\epsilon = \frac{1 + \frac{8\pi}{3} \sum N_i \alpha_i}{1 - \frac{4\pi}{3} \sum N_i \alpha_i} \quad (2.3)$$

The summations in the dielectric constant expression here arise from the Lorentz local field. Since each ion type will in general have a similar but not exact polarization, the polarization can instead be computed separately, in which case the expression for the dielectric displacement can instead be represented as shown in Equation (2.4).

$$D = E + 4\pi P \quad (2.4)$$

In this case, the polarization is simply calculated using the generalized form of polarization as given by Equation (2.5).

$$P = \sum N_i \langle p_i \rangle \quad (2.5)$$

In this generalized form shown in Equation (2.5), the average dipole moment, $\langle p_i \rangle$, is multiplied by the number of dipoles possessing the dipole moment, $N_i$. However, if instead each dipole is assumed to be independent, the summation is taken over each...
individual dipole, and the specific dipole moment replaces the average dipole moment of each ion. This generalization results in a considerably larger summation, dependent on the number of ions assessed, but yields an exact computation of the polarization in the material similar to averaging over all dipoles. In the ferroelectric material model presented in chapter III, the potential at each ion site is computed using the dipole moment of each neighboring ion. The idea of expanding or generalizing is shifted to the application of the polarization for a typically small cluster of unit cells to the entire material, which would typically have more than $10^{10}$ unit cells as seen for the case of having a $10 \mu m \times 10 \mu m \times 350 \text{ nm}$ crystal ($250,000 \times 250,000 \times 875$ unit cells, or approximately $5.5 \times 10^{11}$ unit cells).

(b) Stress Induced Polarization

Owing to the piezoelectric response of ferroelectric materials, an alternate method for inducing polarization lies in applying stress to the material. Once the ferroelectric material is polarized, ion displacements cause the unit cell dimensions to alter slightly, distorting the overall crystal. Although these displacements are small, PZT is known to have some of the largest ion displacements allowing it to have a maximum polarization larger than many other materials. Applied stress to the material promotes distortion in the crystal and polarization. This useful characteristic of ferroelectrics has led to their use in sensors and energy harvesting applications [80, 83, 84, 85, 86, 87, 88, 89, 98].

Given a force, $F$, the Young’s modulus, $E$, is a function of the area over which the force is applied, $A$, and the ratio of the deformation to the original size, $\epsilon$, as given by Equation (2.6).

$$E = \frac{F}{A \epsilon}$$

(2.6)
Many ferroelectric modeling efforts centering on the piezoelectric response attempt to compute the Young’s modulus as the principal measure of the model accuracy. Typical values for piezoelectric materials, such as PZT, vary with composition but experimental values of approximately 30.3 GPa for some macro fiber composites (MFC) and 43 to 44 GPa for PZT have been observed [108, 109, 110]. Since the primary effort of this dissertation is aimed at accurately modeling the ion displacements and time dependency of the displacement, the Young’s modulus will be incorporated from literature. Applications utilizing the piezoelectric response are examined in chapter IV, wherein the polarization is measured as an indication of the applied force. In this manner, the polarization of the FeFET can be measured by such means as current measurement to determine environmental factors such as air pressure.

(c) Theory

The polarization, or polarization density, arising from the displacement of each ion in the ferroelectric crystal is obtained by Equation (2.7).

\[ P = \frac{\sum p_i}{V} \]  

Equation (2.7)

In the form of Equation (2.7), the polarization is expressed as the dipole moment per unit volume or, for \( i > 1 \), the summation of dipole moments over the volume of interest, \( V \). Since the volume of interest is the entirety of the crystal, the volume, \( V \), in Equation (2.7) is simply evaluated over the whole crystal and therefore has units of cm\(^3\). The dipole moment for each ion is easily computed directly from the charge of the ion, \( q_i \), – shown in Equation (2.8) as what would be the net charge of the ion – multiplied by the displacement, \( d \).

\[ p = q \cdot d \]  

Equation (2.8)
In reality the ion would have a charge distribution based on the potential arising from neighboring ions and any external fields or forces. To accommodate this, the electron cloud is sometimes assumed to be a spherical shell that would displace relative to the nucleus. This approximation allows a simplified charge distribution, which is related to the ionic polarizability of each ion. Using this assumption, Equation (2.8) instead is expanded to account for both nuclear (core), \( q_c \), and electronic (shell), \( q_s \), charges, resulting in the form expressed in Equation (2.9).

\[
p = q_c \cdot d_c + q_s \cdot (d_c + d_s)
\]  

(2.9)

Here the shell displacement is taken to be relative to the core, which will be expanded upon in chapter III.

As typical for a crystal lattice, the displacement is assumed to be in any direction, resulting in the displacement and dipole moment both being vectors in three-dimensional space \( \mathbb{R}^3 \). Owing to the symmetry of the unit cell, a Cartesian coordinate system is used throughout this dissertation. Within the unit cell, examination of the potential due to neighboring ions readily gives rise to the principal displacements of the ions. Looking first at the central ion of PZT as depicted in Figure 2.3, the lead ions at each corner are similarly (positively) charged while the oxygen ions at each face are oppositely (negatively) charged. With this in mind, it is not surprising that the principal displacements, for a coordinate system centered at the central ion position with basis vectors extending normal to the cube faces, are along the basis vectors. The electrostatic potential arising from neighboring ions reveals this idea directly as shown in Figure 2.10. In this case, only the electrostatic potential is shown, which for oppositely charged ions is expected to have singularities when evaluated for coincident pairs. For the considered
coordinate system examining the central ion in the PZT unit cell, a singularity is observed for displacements equal to a half lattice constant in any direction owing to the electrostatic potential having the form of Equation (2.10).

\[ U_{ij} = \frac{q_i q_j}{|x_i - x_j|} \]  

(2.10)

Figure 2.10: Potential evaluated for a central ion (Ti\(^{4+}\)) within the PZT unit cell having a weak electric field applied along the \(x\)-axis. Potential shown for the \(z = 0\) plane with the crystal having a tetragonal arrangement with the \(c\) extent along the \(x\)-axis.

As to be expected as a result of observed stability in crystals, an additional potential term works to counteract singularities due solely to electrostatic potential terms. Arising from the Pauli exclusion principle, a repulsion term exists that serves to ensure ions do not collocate in space. This repulsion term is proportional to distance raised to a power greater than one, thereby ensuring the potential would diverge in the positive direction more quickly than terms that may diverge in the negative direction. Several approximations of the potential exist and vary with the type or types of ions included in
the pair. The Lennard-Jones potential, often referred to as simply the L-J potential, shown in Equation (2.11) is a simple and computationally efficient approximation of potential that can be tuned to well represent experimental data.

\[ U(r) = \frac{A}{r^{12}} - \frac{B}{r^6} \]  

(2.11)

Similarly, the Buckingham model in Equation (2.12) has proved to also well represent experimental data by using an exponential term as the repulsive component of the potential [111, 112].

\[ U(r) = A e^{-Br} - \frac{C}{r^6} \]  

(2.12)

For this dissertation, and expanded upon in chapter III, the Lennard-Jones potential form is used. The primary advantage observed here is the removal of the singularity introduced with the electrostatic potential term. When evaluating the potential at an arbitrary point, the need to determine a priori the volume over which the potential term is valid can be removed.

Within the ferroelectric material, the electric field may decomposed into four components which define the local electric field, \( E_{loc} \), as shown in Equation (2.13).

\[ E_{loc} = E_0 + E_1 + E_2 + E_3 \]  

(2.13)

The first component of the local field is the external field, \( E_0 \), which arises from the applied electric field or more generally simply from charges external to the system. Here, the applied electric field can be found directly by considering the applied gate voltage relative to the channel or, more generally, semiconductor potential. Secondly, the depolarization field, \( E_1 \), arises from the displacement of charges (considered to be ions in this work) due to the electric field. The depolarization field takes on a value equal to the product of the depolarization factor (\( N \)) and the polarization of the material (\( P \)), where
the depolarization factor depends on the shape and orientation of the material. The remaining two terms, $E_2$ and $E_3$, are determined on a scale smaller still, dealing with the site specific to the ions. The Lorentz field, $E_2$, arises from the field produced by considering the (hypothetical) removal of a small cavity (often considered spherical) containing the reference site and nearby dipoles. With the cavity removed, charges that remain on the surface of the cavity produce another field, given by Equation (2.14) for a spherical cavity of radius $a$ in a uniformly polarized material.

$$
E_2 = \int_0^\pi a^{-2} (2\pi a \sin \theta)(a \, d\theta)(P \cos \theta)(\cos \theta) = 4\pi P / 3
$$

(2.14)

The Lorentz field is interestingly similar to the Weiss internal field, stemming from the Curie-Weiss law in ferromagnetic materials. One major difference between the two is that the coefficient, here $4\pi/3$, is often of the order of 1000. Lastly, the field inside the cavity resulting from the contained dipoles is given by Equation (2.15), which is simply the electric field from a dipole moment, $p$, at a distance, $r$, for each dipole.

$$
E_3 = \sum_i \frac{3(p(r) \cdot r_i - p_i) |r_i|^2}{|r_i|^5}
$$

(2.15)

The macroscopic electric field is given by the average field over the entire material, as given by Equation (2.16) where $e(r)$ is the microscopic electric field.

$$
E(r_0) = \frac{1}{V_{cav}} \int dV \, e(r)
$$

(2.16)

However, the electric field caused by a uniform polarization, $P$, is equal to the electric field produced by a surface charge density, $\sigma$, on either surface of the material. By treating each separate domain as a separate volume over which the electric field is averaged, the macroscopic field acting on the semiconductor can be obtained by considering the surface charge of the domain [5, 114].
(iii) Retention

Once set ion displacements are established in the ferroelectric crystal, polarization is retained for a length of time determined by the energy of the system. The energy is governed by the environment of the material, including the temperature. As energy is added to the system, the probability of ion displacements changing increases as the energy increases either beyond the potential barriers between potential wells or to the point that sufficient tunneling through the barrier is probable. An example of these potential wells is exhibited in Figure 2.10 along the $x = 0$ and $y = 0$ lines. The potential barrier, arising chiefly from the interaction with neighboring lead ions for the central ion, is most effective at restricting movement for central ion energies sufficiently below the barrier height. Consequently, the time expected for an ion to move across or tunnel through the barriers imposed by the potential arising from neighboring ions shortens as energy is added to the system, allowing the dipole moment to neutralize due to the depolarization field created by initial ion displacements.

By virtue of the perovskite structure detailed in Figure 2.3 and the net charges on each ion, the central ions are expected to displace principally toward one of the oxygen ions located on the unit cell face. Similarly, the lead ions tend to displace in a slightly skewed manner relative to a stable oxygen cage. In this work, the oxygen cores or nuclei are assumed to remain stationary to provide stable reference points against which the cation displacements can be measured. Two caveats to this assumption are the crystal distortion, which is allowed to move the oxygen ions, and the oxygen electron shell displacement, which generally takes on a non-zero value and follows the same stipulations governing cation shell displacements. As a result of this construct, the
relative motion of each ion – to include the core and shell motion as well – influences each other ion and thereby the time evolution or retention properties of the ferroelectric material.

The time evolution of each ion component, core and shell, is taken to be defined by the wave function for the respective component. Using the time dependent form of the Schrödinger equation gives the well-known expression given in Equation (2.17).

\[ i\hbar \frac{d}{dt} \Psi = \hat{H} \Psi \]  

(2.17)

This representation in Equation (2.17) shows the dependence of the time evolution on the potential as defined by the Hamiltonian operator for the system. Since the PZT unit cell lends itself to working in Cartesian coordinates, the Schrödinger equation can be written in the position basis as given in Equation (2.18).

\[ i\hbar \frac{\partial}{\partial t} \Psi = \left( \frac{-\hbar^2}{2m} \nabla^2 + V \right) \Psi \]  

(2.18)

Both the wave function, \( \Psi \), and the potential, \( V \), are taken to be a function of both time and position in Equation (2.18). The very directly coupled nature of the polarization is evident in this form as the potential is a function of neighboring ions, in addition to any external terms. Of particular interest here is the well-known idea that the time evolution of the system is quite simple in the quantum mechanical frame if the wavefunction is known at any point in time [115, 116].

(iv) Temperature

If the material reaches the Curie temperature (492 °C for PT and 233 °C for PZ), then ions have sufficient energy to travel over the potential barriers in the system unimpeded, and the polarization is no longer retained. At this temperature, the relative permittivity increases significantly as shown in Figure 2.11 for PT and Figure 2.12 for PZ.
for PZ. Above this temperature, however, the ferroelectric material acts as a purely dielectric.

Figure 2.11: Temperature variation of the dielectric constant in lead titanate. Reprinted with permission from G. Shirane, E. Sawaguchi, and Y. Takagi, *Physical Review*, 84, 476-481 1951. Copyright 1951 by the American Physical Society.
The primary consideration of temperature dependence in this work stems from the energy of the system. Energy of the system affects the retention properties of the ferroelectric layer. Additionally, the dielectric constant is expected to change with varying temperature and will be evaluated using the model. All experimental data were collected at room temperature, restricting available data for anchoring and model validation.

B. FeFET Operation

As mentioned previously, electric polarization of the ferroelectric material is the distinguishing factor that separates FeFET operation from that of commercially available field-effect transistors such as MOSFETs, JFETs, or TFTs. The polarizability of the ferroelectric layer creates a system in which the drain current depends not only on the gate voltage but also the polarization state, which has been shown to possess a history dependence. Polarization of the ferroelectric layer can effectively be shown to offset the gate voltage by a quantity dictated by the combination of current polarization and current gate voltage.

Earlier research remarked that this can, in the extreme and assuming sufficient polarization, effectively switch the FeFET between a depletion and enhancement mode transistor. That is to say, the threshold voltage for the transistor can be shifted so far as to be made negative, resulting in a depletion mode transistor that has appreciable current even with 0 V applied at the gate. For the n-channel devices considered in this dissertation, depletion mode operation stems from negatively polarizing the transistor, with the polarization carrying a descriptor similar to the voltage used to induce said polarization. Conversely, if a positive voltage is applied to the transistor gate, the
resulting positively polarized ferroelectric layer acts to restrict current in the device. In this state the FeFET acts as an enhancement mode transistor. One of the most intriguing applications of these transistors that has not yet been explored thoroughly to date is the idea of polarizing the transistor to adjust the threshold voltage of the transistor spontaneously. In doing so, the transistor characteristics can be altered significantly, resulting in differing biasing points and therefore gains in analog circuits or switching speeds for memory devices. Applications utilizing this attribute of the transistor will be explored in chapter IV. Additionally, the model developed in this dissertation can be used to compute the necessary gate voltages to change the threshold voltage of the transistor as well, aiding in future circuit design.

(i) Static Polarization

Polarization of the ferroelectric crystal in the particular FeFETs used here is not directly measurable due to the structure of the transistor, or more specifically the arrangement of the ferroelectric layer and channel contacts being opposite one another as indicated in Figure 2.1. As a result, when measuring the polarization under each of three channel terminal configurations, source and drain connected or only one of two channel terminals connected, the contribution to the polarization of each terminal of the device is revealed in addition to any polarization contribution by the ferroelectric layer. Therefore, the semiconductor material affects not only the measurement of the polarization but also the polarization itself. As shown by measurements of the channel potential over a range of applied gate voltages, the depletion region depth into the semiconductor increases under negative gate-to-channel terminal voltages, which in turn restricts the ability to polarize the material as effective under negative conditions. Of note is that in practice
when poling the transistor gate, the additional depletion region depth into the semiconductor results in longer poling times. This stems from the essentially reduced contact area for a significantly negative voltage in addition to the slightly increased thickness and resulting drop in electric field [118, 119]. In particular this operation is an artifact of the somewhat unique structure used, and not observed in most present-day literature.

The primary consideration for polarization with regards to the different source and drain connections results from the cutoff of the semiconductor in the vicinity of the contact. As a terminal voltage, connected to the n-type semiconductor, increases relative to the gate voltage, which is connected to the PZT layer acting as a p-type semiconductor, the depletion region near the interface increases. The effect reduces the area around the contact, making it more difficult to negatively polarize the FeFET ferroelectric layer. This idea is shown through the surface potential for varying gate voltage, which is not symmetric for both positive and negative voltages, as demonstrated in Figure 2.13. Also of note is the idea that the surface potential is defined by a hysteresis, with a range of possible values for a particular applied gate voltage. This is especially important for scenarios in which the gate voltage is negative, as the source and drain contact size in the semiconducting material is restricted as indicated by surface potential measurements of such devices [118, 119].
Figure 2.13: FeFET surface potential for varying applied gate voltage reprinted with permission (www.tandfonline.com)

Shown typically for maximum polarization with gate voltages sweeping from +5 to -5 V as in Figure 2.13, in practice the polarization and resulting surface potential is often not defined by the outer edge. Instead, the partial polarization, whereby the polarization takes on a value between the two extremes depicted in the polarization hysteresis, typically defines the polarization observed in during device operation [11, 17]. Partial polarization arises from the applied voltage being sufficiently large enough only to polarize a fraction of the PZT ions, changing the dipole moment of only some ions in the ferroelectric crystal to an appreciable degree. This can be shown from Figure 2.14 where the amplitude of the voltage across the ferroelectric layer is varied in a fashion to observe interior loops of the drain current hysteresis that results from varying the ferroelectric polarization. This concept forms the basis of the Preisach model developed to describe
ferromagnetic domain switching wherein smaller, individual hystereses contribute a portion to the overall polarization or magnetization and sum to form the complete response of the material [120, 121, 122].

Figure 2.14: Effects of partial polarization on the drain current of the FeFET as shown for seven interior loops of varying amplitudes after the initial curve establishes initial conditions following the gate voltage increasing to 6 V. The discontinuity in the measurements occurring between 2 V and 3 V results from measurement relay switching between sensitivity settings.

(ii) Drain Current

One of the primary characteristics of a modern, commercial transistor is the device drain current under specific conditions, such as terminal voltage and temperature. Similarly, as the FeFET replaces a transistor in most applications assessed for adoption of the device, the FeFET drain current is of particular importance. Owing to the hysteresis of the ferroelectric layer of the transistor, the drain current must be characterized with varying polarization states with the gate voltage similarly varied. Similarly, since the
FeFET is able to operate a depletion mode transistor for periods of time, the retention characteristics of the drain current is of particular importance for memory applications.

(a) Active Current

Active current of the FeFET is defined as the drain current observed with the presently applied, generally non-zero, gate voltage. In this operating mode, the transistor is viewed as a FeFET with essentially a threshold voltage modified by the polarization state. As shown in Figure 2.15, the point at which the transistor begins conducting significantly is adjustable through variations in the polarization state. Additionally, the slope of the current modifies slightly across the applied voltage range [32, 36, 39]. Variations in the derivative of the current arise from the non-linear switching of the polarization as the voltage is increased. A unique aspect of the FeFET is then revealed in that the transconductance, as given by Equation (2.19), can be altered simply by polarizing the ferroelectric layer differently.

\[
g_m = \frac{\partial i_{ds}}{\partial v_{gs}}
\]  

(2.19)

Changing the polarization state in turn alters the biasing or quiescent point (Q-point) of the FeFET. When coupled with adjustments of the gate voltage, adjustments in polarization state allow for differing transconductance while maintaining the same drain current, effectively altering only the transconductance of the device. The transconductance plays an important role in electronic circuit design as it factors into the gain of most amplifier circuits or the oscillation condition. This point in particular can result in interesting use cases for a FeFET over other devices such as a MOSFET in analog circuits. Using the same biasing current, the gain of the device is adjustable. This unique property allows for a variable gain of the circuit by simply adjusting the
polarization state of the transistor while all other elements are essentially constant owing to the consistent biasing current provided [32, 36, 39, 44, 45].

Figure 2.15: Active drain current hysteresis for FeFET models ND1, ND4, and ND7

The effects of polarization on the drain current can be viewed as essentially reversed relative to the gate voltage. An increased, positive gate voltage will decrease the depletion region existing between the PZT, which acts as p-type semiconductor, and the indium oxide semiconductor. Decreasing the depletion region will in turn increase the channel size and therefore the drain current of the transistor. This drain current trend is typical for n-type transistors, though the mechanism for widening the channel is similar to that of conduction for JFETs rather than MOSFETs. The opposing nature of these
two forces – the polarization and gate voltage – is most clear when comparing the active to remnant current hystereses.

(b) Remnant Current

As expected from the polarization, the FeFET is capable of conducting significant and varying current with 0 V applied at the gate. To define the current with 0 V at the gate as a function of polarization, the remnant current is defined as a function of the previously applied, non-zero gate voltage. This definition of remnant current results from the idea of the current remaining after the gate voltage is “removed,” wherein the gate is often then essentially grounded. A typical circuit used to measure remnant current is shown in Figure 2.16, where the switch is open for remnant current measurements, and the applied gate voltage with the switch closed is used to set the polarization state between measurements.

![Figure 2.16: Remnant current measurement circuit](image)

From the active current measurements, the trend of more negative gate voltages resulting in, effectively, a lessened threshold voltage carries over to remnant measurements as well. Remnant current similarly follows from this trend due to the fact that the polarization state, arising from application of a negative gate voltage, serves to
increase the semiconductor channel, increasing overall current. Channel depth increases as a result of the polarization of the PZT layer being arranged such that an essentially negative charge exists at the PZT-semiconductor interface. This charge distribution will then repel negatively charged electrons, encouraging a channel to form between the oppositely positioned source and drain contacts. For a positive gate voltage, the induced polarization is reversed, whereby the channel is instead discouraged by attracting additional electrons away from the channel formed between the source and drain contacts. In these devices, the semiconductor is an n-type material, meaning the channel formed to allow drain current is composed of negatively charged carriers (electrons).

The observation of having more negative gate voltages stimulate larger remnant current is in-line with the physics dictating the FeFET performance. As shown in Figure 2.17 for the ND1, Figure 2.18 for the ND4, and Figure 2.19 for the ND7 transistors, the remnant current has an almost mirrored effect relative to the active current. Also of note, the magnitude of the current is similar at the point of maximum conduction. This observation leads to the thought that polarization has an effect on the channel conduction that is similar in magnitude to the effect of the gate voltage. As noted from the active current and polarization hystereses, the remnant current hysteresis is defined by the previous polarization state at each point, which is determined by the maximum and minimum voltage applied in addition to the initial conditions of the ferroelectric material.
Figure 2.17: Active and remnant current hysteresis ND1 FeFET with 1 V drain-to-source voltage. The gate voltage was set to 0 V while collecting the remnant current measurements; the data are plotted against the last applied gate voltage.

Figure 2.18: Active and remnant current hysteresis ND4 FeFET with 1 V drain-to-source voltage. The gate voltage was set to 0 V while collecting the remnant current measurements; the data are plotted against the last applied gate voltage.
Figure 2.19: Active and remnant current hysteresis ND7 FeFET with 1 V drain-to-source voltage. The gate voltage was set to 0 V while collecting the remnant current measurements; the data are plotted against the last applied gate voltage.

Though the remnant current is tied to the remnant polarization, the effects of having a non-zero drain-to-source voltage influence the polarization and therefore the remnant current over time. Since the FeFET may be included in low-power and memory devices, characterization and understanding of the remnant current is especially important if using the device for long periods between gate poling. The drain-to-source voltage will destructively act on the ferroelectric layer polarization, resulting from the orientation of the channel contacts and proximity to the PZT layer. Principally, the dipole moments are oriented normal to the gate contact. However, the introduction of a significant drain voltage, with the source assumed grounded, acts to reverse – or at the least lessen – the polarization near the drain, the terminal typically having the largest voltage in this setting. Considering the remnant current configuration with the gate contact essentially grounded, a positive drain voltage will produce an electric field oriented from the drain to
the gate contact. Here, the effect of the drain voltage is similar to that of applying a negative gate voltage, which would serve to “overwrite” the PZT polarization state if in a positively poled state. On the other hand, if in the negatively poled state then the drain voltage will serve to help maintain the polarization state. This has been noted in memory circuit designs as the negatively poled state having a lessened dependence on the drain voltage, assuming a positive value with the gate grounded.

(iii) Gate Capacitance

Gate capacitance is one of the most examined features of transistors incorporating ferroelectric materials. Though most current research focuses on negative gate capacitance, the FeFETs of interest in this dissertation use a unique topology that is not conducive to the phenomenon. However, the capacitance of these FeFETs is still of particular interest for inclusion of the devices in radio frequency (RF) circuits as well as understanding and modeling the switching characteristics of the devices. Addition of ferroelectric devices in any circuit will require extensive knowledge of the device capacitive effects. Introducing a large capacitance severely decreases the switching speed of high-speed memory devices or inadvertently changes the operating frequency of radio-frequency circuits.

Owing partially to the polarization of the devices, the charge entering or exiting the source or drain contact is observed to be non-linear with respect to the applied voltage. As the polarization switching occurs, the gate capacitance increases more rapidly, falling back to a “nominal” level after the polarization is saturated. This coupling of the polarization, or charge, and the capacitance is shown in Figure 2.20
wherein the polarization dependence of the capacitance is highlighted by the dramatic differences in gate capacitance within a single loop.

![Figure 2.20: Experimental data of the FeFET gate-to-source capacitance for each of the ND1, ND4, and ND7 FeFET models](image)

Possibly the most interesting, and complicating for circuit design, is the voltage dependence of the gate capacitance. Where most capacitors are linear with respect to voltage, which is to say that the capacitance given by Equation (2.20) is constant, the FeFET gate-to-source capacitance, $C_{gs}$, is quite notably non-linear.

$$C_{gs} = \frac{\partial q_s}{\partial v_{gs}}$$ (2.20)

The capacitance must be evaluated at each point, using the definition, since charge is a non-linear function with respect to voltage. Both advantages and disadvantages exist to this complexity. First, the capacitance of the FeFET can be adjusted very easily for a given biasing point by simply changing the polarization state. This can lead to different
modes of operation available to circuits using the FeFET to minimize capacitance during specific regions of operation by poling the gate accordingly. However, since the polarization state is not static and instead varies with time, this can necessitate refreshing the polarization or poling the gate periodically, with a refresh rate dependent on the voltage levels used.

The switching speed of the device is also influenced by the gate capacitance. Large gate capacitances limit the operating frequency allowed for some circuits, such as the ring oscillator explored in chapter IV. While all FeFETs discussed in this dissertation have the same thickness, it is noted that the dimensions of the ferroelectric layer will determine many of the properties of the FeFET. For example, as thickness of the ferroelectric layer increases so does the time required to polarize the material. For the ring oscillator, this increased capacitance serves to decrease the operating frequency as the input capacitance of the inverting stage is increased, more heavily loading the driving inverting stage.

(iv) Retention Properties

Polarization retention of the ferroelectric layer in the FeFET is determined by several factors, many of which have already been mentioned. The most prominent factor driving polarization is the temperature, with the Curie temperature being the limiting case of having no retention properties. In this somewhat extreme case, the FeFET has sufficient energy to overcome the potential barriers and the memory or retention properties of the device are lost. However, even with temperatures below the Curie temperature retention properties degrade over time. As additional time passes since the polarization state is set, the probability density function of the ion shifts, resulting in
changing displacements over time. Effects of time on the polarization are noted to be logarithmic with respect to time [49, 123]. This trend is intuitive owing to the exponential used to define the wave function in the barrier with an energy level below the barrier height.

(a) Polarization Retention

By far the most widely used application for ferroelectrics in circuits is memory storage. As such, the polarization retention is of particular concern. Use of a FeFET in memory devices also exists on a smaller scale, but the ability to show the retention characteristics of the device will not only aid circuit design using these devices but also raise interest in the devices and aid in device design [37, 42, 43, 47, 48].

The polarization retention of the FeFET is key to the history dependence of the FeFET. When a circuit is powered down, the FeFET retains the current state owing to the non-volatile nature of the polarization. This has led to ferroelectrics use in memory applications. Similarly, the incorporation of a ferroelectric material at the gate of the FeFET allows polarization retention after being set or the gate being poled. Polarization retention affects not only the current, but instead the entire state of the FeFET. As mentioned earlier, the gate capacitance is dependent on the polarization state. This creates a crucial design factor when utilizing a ferroelectric device in a circuit that may turn on and off periodically or transition between powered and unpowered modes of operation, such as employed for low-power applications. As a result, particular care must be taken when polarizing the transistor and anticipating the state during powering.

Temperature and elapsed time are the two primary factors used when considering the expected retention of a device. However, especially true for the three-terminal
FeFET, different voltages applied at the terminals will have a detrimental or beneficial effect on the retention. Depending on the poled state, the voltage at the transistor terminals will either serve to encourage the set polarization in the event of a similar polarity voltage being applied across the terminal or have a destructive effect on the polarization state if an opposite polarity voltage is applied. In this context, a voltage encouraging the current present polarization state serves to increase, albeit perhaps only slightly, the potential barrier acting to keep ions in the current displaced positions. Conversely, a voltage working to destroy the polarization instead lowers the potential barrier, allowing ions to change displacement more freely.

In order to have an appreciable drain current in the device, often the drain voltage is significantly larger than the source and possibly the gate voltage, which can also arise from powering off only portions of the circuit. Additionally, circuits such as the 1T1C Dynamic Random Access Memory (DRAM) in chapter IV incorporate memory elements storing information in the polarization and voltage. In this setting despite the ability to power off the device, the charge on the capacitor can serve to counteract the polarization in the FeFET, thereby decreasing the effective retention time.

(b) Remnant Current

The easiest method to sample the polarization of the FeFET is through measurement of the current. Of the current, remnant current most easily defines the polarization state to include the retention properties. From the remnant current, several factors can be deduced depending on the available information. The current is a function of the applied voltage and the elapsed time, neglecting the effect of temperature by assuming the transistor remains at room temperature or well below the Curie temperature.
for PZT [49, 123]. Knowing the voltage that was applied, typically taking on one of only a few possible values, the time elapsed since the last poling can be estimated. If the poling voltage is unknown, such as may be the case with an analog circuit or sensor, drain current measurement at a particular time can instead lead to accurate estimation of the applied poling voltage or last state of the device or circuit. This does, however, assume the voltages were large enough to sufficiently polarize the ferroelectric layer and any partial polarization may obfuscate the particular voltages used.

Previous testing of the retention properties of the remnant current highlighted the current decay with time. Illustrating the deterioration of the gate polarization over time, even when faced with a minor drain voltage, the drain current decay with respect to time is shown in Figure 2.21. Alternatively, channel resistance measurements with the drain voltage turned off between measurements are shown in Figure 2.22 using the ND1, Figure 2.23 using the ND4, and Figure 2.24 using the ND7 FeFETs. In this case the gate polarization is established once again between each read out owing to the potentially destructive operation of applying a voltage to the FeFET drain. A resistive load inverter circuit was used to measure the channel resistance of each FeFET over time, which extended up to two weeks. Because of this configuration, the drain voltage is not always maintained at 5 V and instead decreases as the drain current increases, resulting in a larger voltage drop across the load resistance rather than the FeFET channel.
Figure 2.21: Remnant current decay for a previous generation ND7 model transistor with a constant 0.5 V applied at the FeFET drain terminal after having -8 V applied at the gate terminal.

Figure 2.22: Remnant channel resistance of the ND1 FeFET after applying a ±5 V write voltage to the gate terminal for at least 100 ms. A resistive load inverter was used as the FeFET measurement circuit, resulting in less than the total 5 V supply being dropped across the FeFET channel.
Figure 2.23: Remnant channel resistance of the ND4 FeFET after applying a ±5 V write voltage to the gate terminal for at least 100 ms. A resistive load inverter was used as the FeFET measurement circuit, resulting in less than the total 5 V supply being dropped across the FeFET channel.

Figure 2.24: Remnant channel resistance of the ND7 FeFET after applying a ±5 V write voltage to the gate terminal for at least 100 ms. A resistive load inverter was used as the FeFET measurement circuit, resulting in less than the total 5 V supply being dropped across the FeFET channel.
C. Conclusion

The FeFET device operation incorporates both semiconductor and ferroelectric material physics, making it a uniquely interesting device. Additionally, the device geometry of the particular FeFETs of interest in this work gives rise to device operation not extensively examined in literature. Aspects of the ferroelectric layer, here PZT, polarization and retention, which is the focus of this effort, encompass a wide array of device attributes and circuit specific considerations.
CHAPTER III

METAL-FERROELECTRIC-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR MODEL

The FeFET model in this dissertation deals primarily with electric polarization as discussed in chapter II. Although several methods have been used to model the ferroelectric crystals, the method of choice here is the shell model of an atom. In the shell model of atoms, which has been shown to reproduce experimental results, the nucleus is considered a point charge and the electron cloud a spherical shell attached by an anharmonic spring [111, 112, 126, 127]. However, due to the small scale and relatively quick movement of ions, time steps in simulations often must be on the order of femtoseconds ($10^{-15}$ seconds). For large crystals and considering complex potentials, simulations often are only able to be run for picoseconds ($10^{-12}$ seconds).

A model of the FeFET as a unified device is developed that incorporates unique properties such as polarization, remnant current, and current hysteresis, which should aid circuit and device design. The presented model embodies the physical laws and device properties primarily, with empirically defined constants being removed to the extent possible. Additionally, the presented model incorporates the transistor structure, similar to that of a thin film transistor or JFET, that has not been considered in any earlier literature or modeling attempts. As the distinguishing feature of the FeFET is the
ferroelectric layer, and more specifically the polarization, the model is focused primarily on accurately describing the ferroelectric layer polarization under various conditions and over time. As a consequence of having a detailed description of the polarization state, channel potential, charge, and current is found directly using semiconductor physics. A summary flow diagram of the model progression is given in Figure 3.1 for model startup (initialization), Figure 3.2 for time evolution in the ferroelectric material, and Figure 3.3 for the semiconductor model, thereby encompassing the operation of both ferroelectric and semiconductor components.
Figure 3.1: Flow diagram of the FeFET model startup, which is principally defined by determining the steady-state polarization state given the current applied terminal voltages.
Figure 3.2: Flow diagram of time advancement for the ferroelectric layer with the interior looping over all ion components (core and shell) prior to updating FeFET polarization
Figure 3.3: Flow diagram of the semiconductor model for which the primary objective is calculating the drain current by way of the depletion region depth. Shown as optional is the feedback component of the drain current affecting the ferroelectric layer potential.

A. Lead Zirconate Titanate

The ferroelectric material in the FeFETs of interest in this body of work is a 20/80 composite of lead zirconate and lead titanate (PbZr$_{0.2}$Ti$_{0.8}$O$_3$). Spontaneous electric polarization in the PZT layer is the defining difference between FeFETs and either JFETs or MOSFETs and therefore the focus of this model. The PZT layer resides between the gate contact and the semiconductor in the FeFET as shown in Figure 2.1, which results in
variations in gate capacitance and channel potential. Modeling of the FeFET polarization will begin at the PZT unit cell, which is shown in Figure 2.3. Given the potential and PZT layer dimensions, the most probable displacement of the central, positively charged ion will be calculated. Once the unit cell polarization is determined, the spatial contraction or expansion of the crystal will also be considered along each dimension. At this point, the neighboring interactions will become a factor due to slight physical strain in the lattice as well as neighboring central ion interactions. However, more than 8 trillion PZT unit cells (sized approximately 0.4 nm × 0.4 nm × 0.4 nm) exist in a 40 µm × 40 µm × 350 nm layer, which requires efficient calculation of the unit cell polarization and the assumption of applying ion displacements across neighboring unit cells to reduce required calculations. The electrostatic potential considerations in the semiconducting channel are then calculable given the ferroelectric polarization state, which ultimately satisfies the goal of accurate current calculations.

While the model parameters developed and used in this chapter are specific to the transistors provided by Joe Evans at Radiant Technologies, Inc., the model is generic and can in general be applied to any ferroelectric material or transistor geometry. Parameters that are transistor specific, such as the tuned parameters accounting for ion or shell displacement are noted throughout this chapter to provide a targeted approach to transitioning the model to another material. Additionally, the ferroelectric model may be extracted to model a ferroelectric capacitor, which is generally a capacitor using the ferroelectric material as a dielectric layer. As such, comparisons to ferroelectric modeling, including capacitors is discussed.
(i) Shell Model

At the heart of the ferroelectric model for this work lies the shell model of the ions in the ferroelectric material. The shell model is selected to represent the ferroelectric ion structure having both a positively charged nucleus, represented by the core, and a negative charged electron cloud, represented by the shell. The two components of the ion are independent, each having their own potential contributions and moving somewhat independently. The core and shell are, however, bound to one another; in this arrangement the shell is coupled to the core by an anharmonic spring with the potential energy arising from displacements taking the form shown in Equation (3.1).

\[ U_{\text{Binding}} = k_2x^2 + k_4x^4 \]  

(3.1)

In this form, the displacement, \( x \), is the total displacement of the electron shell as measured relative to the ion core. The remaining two parameters, \( k_2 \) and \( k_4 \), are spring constants that are used to shape the potential arising from the coupling of the electron cloud and ion core. Typically, the shell displacement is observed as very small relative to the displacement of the ion as a whole and is related to the ionic polarizability \([129, 130]\).

Ionic polarizability represents the ability to induce a dipole moment given an applied electric field. In centimeter-gram-second (CGS) units, the polarizability takes on the units of \( \text{cm}^3 \), and is represented by \( \alpha \) in Equation (3.2).

\[ \alpha = \frac{p}{E} \]  

(3.2)

One noteworthy simplification is that the polarizability is assumed to be equal in all directions, that is to say the ions are all assumed to be isotropic. This can be a significant simplification given the electron orbital orientation of each ion. If the model
is to be expanded upon to consider the orbital orientation and interaction or distortion, the polarizability is generalized to a $3 \times 3$ matrix given by Equation (3.3).

$$\alpha = \begin{bmatrix} \alpha_{xx} & \alpha_{xy} & \alpha_{xz} \\ \alpha_{yx} & \alpha_{yy} & \alpha_{yz} \\ \alpha_{zx} & \alpha_{zy} & \alpha_{zz} \end{bmatrix}$$  \hspace{1cm} (3.3)

However, for the purpose of polarization retention and integration of the ferroelectric model into a full transistor model, additional complexity by considering the electron orbitals will dramatically increase run time and reduce the duration feasible of simulation for retention measurements.

One further simple addition to the shell potential term beyond the anharmonic spring, which would most likely be necessary for more loosely bound shells (large polarizability) or to simply safeguard against unphysical results, is to disallow any shell displacements exceeding an expected maximum value. The purpose of this is not to limit the shell displacement exactly but instead to ensure the shell does not displace sufficiently far from the ion core to either indicate damage or non-physical displacements. The potential terms in Equation (3.1) should in general accomplish this as the large displacements will cause the potential to increase rapidly owing to the $x^4$ term. In this model the potential defining the shell and core interaction is defined exactly by Equation (3.1) with the addition of a hard constraint at approximately 130% of the maximum computed value for each ion as indicated in Table 3.1.
Table 3.1: Maximum allowed shell displacement relative to the ion core based on ion polarizabilities and empirical ferroelectric material polarization

<table>
<thead>
<tr>
<th>Ion</th>
<th>Maximum Allowed Shell Displacement (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb²⁺</td>
<td>4.55e-2</td>
</tr>
<tr>
<td>Zr⁴⁺</td>
<td>1.72e-3</td>
</tr>
<tr>
<td>Ti⁴⁺</td>
<td>8.82e-4</td>
</tr>
<tr>
<td>O²⁻</td>
<td>2.23e-2</td>
</tr>
</tbody>
</table>

The values of $k_2$ and $k_4$ vary for each ion type. Changing the ferroelectric material necessitates spring constant terms for the ions composing the ferroelectric layer. Additionally, the terms may need to be adjusted slightly to introduce expected shell displacements given the environment of the shell and core. In Table 3.2, the spring constants used to define the PZT potential are shown. However, due to the especially small polarizability of the central cations (Zr⁴⁺ and Ti⁴⁺), the spring constants were not used, instead a slight displacement of 0.25 – 0.5% of the core displacement was imparted on the electron shell. This resulted from the spatial grid required to determine such a displacement being too small to evaluate.

Table 3.2: Spring constants defining the PZT core-shell interaction (due to modeling constraints the Zr⁴⁺ and Ti⁴⁺ spring constants were not utilized)

<table>
<thead>
<tr>
<th>Ion</th>
<th>$k_2$ (erg/cm$^2$)</th>
<th>$k_4$ (erg/cm$^4$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb²⁺</td>
<td>2.50E+12</td>
<td>5E+24</td>
</tr>
<tr>
<td>Zr⁴⁺</td>
<td>5.00E+07</td>
<td>3E+25</td>
</tr>
<tr>
<td>Ti⁴⁺</td>
<td>2.00E+17</td>
<td>4E+28</td>
</tr>
<tr>
<td>O²⁻</td>
<td>5.00E+14</td>
<td>3E+30</td>
</tr>
</tbody>
</table>
The charge assigned to each component of the shell model, core and shell, is dependent on the net charge of the ion and valence electrons such that the net charge of the combined core and shell is equal to the net charge of the ion. This is a defining aspect of this model in particular as some shell models will in general ascribe a core and shell charge such that attributes of interest are satisfied [112, 131]. The end result then becomes an ion with a net charge not equal to the charge in reality, though through displacements of the core and shell exhibited forces may agree with experimental data. However, this is a usually minor departure from the reality of the ion composition as the delta is often with a fraction of an elementary charge.

(ii) Potential

For each core and shell of each ion, the potential is computed at each time step. In general, all ions are allowed to interact with all other ions in the crystal for potential calculations. The exception to this is a cutoff distance, or maximum allowed distance, for the nearest neighbor calculations. For example, when computing the electrostatic potential, rather than evaluating all ions in the crystal, instead only ions within a radial distance not exceeding $1.65 \times \lambda$ are evaluated, where $\lambda$ is the crystal lattice constant – approximately 4 Å for PZT. This maximum neighbor distance is an input parameter and will in general not influence the results of the model to an appreciable degree if increased beyond the currently chosen value. Neighbor distances of multiple lattice constants or more result in exceptionally small potential contributions owing to all potential terms being proportional to a power of the reciprocal radial distance. A notable advancement of this model is the evaluation of the entire potential. Often only the pair of minima which are along the axis normal to the gate contact and channel are considered due to ion
displacement typically being parallel to an applied field [49, 50, 51, 52, 53, 54, 82]. Ion
displacements coplanar with the gate contact and transistor channel (normal to the
applied field) have growing importance when modeling time varying polarization states
with neighboring ion interactions.

As suggested by other implementations of the shell model for ferroelectric
materials, all components interact with each other to varying degrees, including the core
and shell of the same ion [111, 112, 131, 132]. The Coulombic potential arising from the
core or shell is evaluated against each other component of all evaluated neighboring ions.
Similarly, the short-range potential is also computed for the shells of all evaluated
neighbor only. For the shells only, the potential arising from the coupling to the ion core
is computed as well. The final potential term stems from the applied electric field. Both
the Coulombic and electric field potential terms are proportional to the electric charge,
highlighting the importance of maintaining a physical basis for the net charge. An
outline of the coupling of different ions is shown in Figure 3.4.

![Figure 3.4: Ion-ion interaction outline](image)

The component of the potential arising from the Coulombic interaction between
ion components is derived from Coulomb’s law, resulting in the form given by
Equation (3.4).
\[ U_{\text{Coulomb}} = \frac{q_1 q_2}{r} \]  

(3.4)

However, the Coulombic interaction potential shown in Equation (3.4) is valid for stationary charges only. The contribution can instead be generalized to include the motion of the particles if they are moving quickly enough to longer allow the approximation of stationary particles. In such a case, the force is defined by the Lorentz force specified by Equation (3.5), which includes a velocity-dependent term.

\[ F = q(E + v \times B) \]  

(3.5)

Where now the electric field is defined by the charges and applied fields and the motion of charges results in a time-varying magnetic field, \( B \). For the problem of interest, the motion is sufficiently small and slow enough that the stationary charge approximation agrees well with reality. Nevertheless, the ion core and shell motion are obtainable from the corresponding wave function and may be used to solve for the potential exactly.

The short-range interaction between ion shells stems from the Pauli exclusion principle wherein two particles cannot occupy the same state to include position. As a result, the strong repulsion term between ion shells is able to overcome the attraction term for opposite charges that would otherwise be allowed to migrate until collocated as specified in Equation (3.4). If only the ion shells were to have the repulsive term, an interesting condition arises depending on the handling of the coupled potential between an ion’s core and shell. If the shell alone has a contribution from the short-range potential and the core-shell coupling is introduced merely as an anharmonic spring constant, then the core may be seen to in essence “drag” the shell with it owing to the continually lower potential. Instead, a stricter coupling of the shell potential must be used. In this model, the approach is to evaluate the contribution of the short-range
potential between shells and include it in the core potential computation. This approach assumes the core and shell displacement will not change appreciably over a time step, which is a valid assumption since the time steps of interest are taken to be on the order of femtoseconds ($10^{-15}$ seconds).

The form of the short-range potential ($U_{SR}$) is borrowed from an alternate though equivalent form of the Lennard-Jones potential shown in Equation (2.11), where the potential is strongly coupled to the inverse of the distance. By instead replacing the two independent coefficients by two, coupled coefficients, an equation of the form shown by Equation (3.6) is constructed where the minimum energy and radial distance corresponding to the minimum energy are precisely specified.

$$U_{SR} = \frac{A}{r^{12}} - \frac{B}{r^6} = \varepsilon \left( \left( \frac{r_m}{r} \right)^{12} - 2 \left( \frac{r_m}{r} \right)^6 \right) \quad (3.6)$$

In the $A - B$ form of the potential, the expression is easily shown to have each a strong repulsive ($A$) and weaker attractive ($B$) term. However, in the alternate form shown in Equation (3.6), the range at which the minimum occurs, $r_m$, and the energy at the minimum, $\varepsilon$, are easily specified. The alternate form quickly becomes more useful in tuning parameters to result in ionic displacements in line with experiment. For example, the ion displacement, which is principally composed of the core displacement (shell displacement measured relative to the core displacement), is expected to be roughly 0.5 Å for lead ions. Given the various interactions that exist for each ion, the parameters may be computed such that each ion, and each component of the ion, achieves the desired displacement. Similarly, the time dependence of the polarization, arising chiefly from the depth of the potential well and energy of the system, is used to compute the terms defining the potential well depth.
Since cation electron clouds (those of lead, zirconium, and titanium) are significantly smaller than those of the anions in the crystal (oxygen), the short-range interaction resulting from the shell-shell interaction is often assumed to be essentially zero [111, 112]. This means that only anion-anion or cation-anion (and equivalently anion-cation) shells interact according to the Lennard-Jones potential in this model. This simplification can be removed with the definition of non-zero coefficients for the ion interactions, which is a component of the overall potential. However, this simplification is often done in practice since the values of $A$ and $B$ result in a small contribution to the overall potential, making the additional computation largely unnecessary.

For PZT, the $A$ and $B$ coefficients are tuned to experimental data, reflecting a combination of the desired displacement for each ion core and additional relative displacement of the electron shell, as indicated in Table 3.3. Each coefficient is essentially scaled to accommodate the small distances of interest. With distances between ion neighbors taking on values of the order $10^{-8}$ cm, the numerators in Equation (3.6) must be scaled accordingly. Also of note is that the interaction between ions are symmetrical, which is to say that Pb$^{2+}$ interactions with O$^{2-}$ are computed precisely the same as those computed for O$^{2-}$ interacting with Pb$^{2+}$. All cation-cation interactions are listed in Table 3.3 for completeness but are simply assigned a zero to describe no appreciably interaction. Within the model, this simplification is taken advantage of by omitting the additional radial calculations. Since the distance between ion cores and shells are computed for Coulombic potential terms already, only the time otherwise spent on the computation of $R^6$ followed by $R^{12}$ is saved. The resulting potentials formed for each non-zero short-range interaction are shown for a single pair of
ions in Figure 3.5 for Pb\textsuperscript{2+}–O\textsuperscript{2−}, Figure 3.6 for Zr\textsuperscript{4+}–O\textsuperscript{2−} and Ti\textsuperscript{4+}–O\textsuperscript{2−}, and Figure 3.7 for O\textsuperscript{2−}–O\textsuperscript{2−}. While the minimum does not immediately fall at the prescribed dislocation for each ion, of note is that shown is only the interaction between a single ion pair rather than the entirety of the neighbors considered.

Table 3.3: PZT short-range potential coefficients for use in the Lennard-Jones potential

<table>
<thead>
<tr>
<th>Ion-Ion Interaction</th>
<th>A (erg·cm\textsuperscript{12})</th>
<th>B (erg·cm\textsuperscript{6})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb\textsuperscript{2+} – O\textsuperscript{2−}</td>
<td>7.3\times10\textsuperscript{-103}</td>
<td>7.64\times10\textsuperscript{-57}</td>
</tr>
<tr>
<td>Zr\textsuperscript{4+} – O\textsuperscript{2−}</td>
<td>1.21\times10\textsuperscript{-104}</td>
<td>1.39\times10\textsuperscript{-57}</td>
</tr>
<tr>
<td>Ti\textsuperscript{4+} – O\textsuperscript{2−}</td>
<td>1.21\times10\textsuperscript{-104}</td>
<td>1.39\times10\textsuperscript{-57}</td>
</tr>
<tr>
<td>O\textsuperscript{2−} – O\textsuperscript{2−}</td>
<td>2.425\times10\textsuperscript{-102}</td>
<td>1.986\times10\textsuperscript{-56}</td>
</tr>
<tr>
<td>Pb\textsuperscript{2+} – Zr\textsuperscript{4+}</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Pb\textsuperscript{2+} – Ti\textsuperscript{4+}</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Pb\textsuperscript{2+} – Pb\textsuperscript{2+}</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Zr\textsuperscript{4+} – Ti\textsuperscript{4+}</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Zr\textsuperscript{4+} – Zr\textsuperscript{4+}</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Ti\textsuperscript{4+} – Ti\textsuperscript{4+}</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Figure 3.5: Example short-range (blue) and Coulombic (orange) potential components determining the overall potential (grey) for Pb$^{2+}$ interacting with O$^{2-}$.

Figure 3.6: Example short-range (blue) and Coulombic (orange) potential components determining the overall potential (grey) for Zr$^{4+}$ or Ti$^{4+}$ interacting with O$^{2-}$. 
Figure 3.7: Example short-range (blue) and Coulombic (orange) potential components determining the overall potential (grey) for O\(^2-\) interacting with O\(^2-\).

Though the preceding potentials evaluates the potential given a single pair of ions, the primary point of interest is the potential in the wake of all considered nearest neighbors. In general, the crystal is allowed to distort prior to computing the potential, resulting in an elongation along the axis coinciding with direction of the applied electric field, if any. In refining the coefficients after the initial calculation, this elongation in addition to all nearest neighbor contributions are considered. A surface plot of the potential arising from the use of these coefficients to define the interaction of the ion core with neighboring ions is shown for a single slice of the unit cell (electric field varying in \(x\)-direction) in Figure 3.8 for Pb\(^{2+}\) and Figure 3.9 for Zr\(^{4+}\) or Ti\(^{4+}\).
Figure 3.8: Potential of the Pb$^{2+}$ ion core with an electric field applied along the positive $x$-axis. Distance is measured relative to the thermally averaged ion position, or the ion core having no displacement.

Figure 3.9: Potential of the Zr$^{4+}$ and Ti$^{4+}$ ion cores with an electric field applied along the positive $x$-axis. Distance is measured relative to the thermally averaged ion position, or the ion core having no displacement.
Coupling between the core and shell is achieved through an anharmonic spring potential. The $x^4$ term in Equation (3.1) is present largely to enforce the shell and core remaining together. The values of the spring constants used are related to the polarizabilities of the ions. Additionally, the potential observed at each site, often evaluated at the expected displaced ion location, is used in determining the coupling terms. An example of this is highlighted by the central ion, Zr$^{4+}$ or Ti$^{4+}$, which take on markedly different values of the spring constants to achieve the required displacement. This arises from the fact that the potential is unique for each ion type owing to the geometry of the unit cell and arrangement of ions about the cell.

The spring coupling term contributes to the potential calculation for the shell only. As mentioned earlier, additional coupling is brought about by considering the short-range potential in the core calculations, though evaluated for the shell position. The spring potential term is enforced only on the shell owing to the idea that the shell being considerably less massive will essentially be bound to the core, rather than the reverse. Consideration of the short-range potential in the core potential calculations alleviates concerns of non-physical displacements for oppositely charged ions.

To restrict the model to producing physical results given the long propagation times required for retention calculations, the oxygen cores are held at the thermally averaged location. This construct creates a framework in which the ions will never be allowed to continually migrate after advancing many time steps, eventually resulting in the ferroelectric crystal displacing as a whole. The shells of oxygen ions are allowed to displace about the cores as expected. Additionally, around the ferroelectric crystal, a layer of “padding” unit cells is constructed to remove the concern of the potential
evaluated at the edge of the crystal. The padding unit cells take on ionic displacements representative of the overall crystal and share the same spatial contractions and expansion exhibited by the bulk crystal. Typically, only two padding cells are necessary for the crystal since the nearest neighbor evaluations consider ions no further than two unit cells away. As the maximum nearest neighbor distance (MNND) is increased, the number of padding cells increases as well. Due to physical memory and run time constraints, the maximum nearest neighbor distance and padding cell thickness should be made no larger than necessary. For a ferroelectric crystal having $X \times Y \times Z$ unit cells, the number of constructed unit cells will instead be computed by Equation (3.7), which takes into account the requirement for doubling the unit cell padding to cover both surfaces of the crystal normal to the positive and negative directions of each axis.

$$CellCount = (X + 2 \text{round}(MNND) \cdot \text{pad}) \times (Y + 2 \text{round}(MNND) \cdot \text{pad}) \times (Z + 2 \text{round}(MNND) \cdot \text{pad})$$

(3.7)

Due to the perovskite structure of the PZT unit cell having ions located only at the central faces, corners, and center of the cell, the nearest neighbor consideration can simply be rounded as in Equation (3.7). In this manner considering nearest neighbors up to $2.5\lambda$ would require three padding cells in order to capture the oxygen and central cation considerations. Because of this formulation for the number of cells constructed and evaluated for nearest neighbor terms, the speed at which the number of cells can quickly grow has the great potential for resulting in excessive run times or the inability to assess retention characteristics.
(iii) Wave Function Calculation

For each ion component, core and shell, the representative wave function is calculated. The wave function can then be used to determine the expectation value of all observables related to the component by using the corresponding operator acting on the wave function. The idea of determining expectation values of observables will be expanded upon in the sections of chapter III discussing dipole moment and polarization computations. At a high level, with the potential calculated for the target ion component, the time independent Schrödinger equation, given by Equation (3.8), is solved for the spatial component, \( \psi \), of the total wave function, \( \Psi \), and is indicated as a function in \( \mathbb{R}^3 \).

\[
\frac{-\hbar^2}{2m} \nabla^2 \psi(x, y, z) + U \psi(x, y, z) = E \psi(x, y, z) \tag{3.8}
\]

In general, the wave function is a time varying quantity and time dependence will be taken into account in detail in the wave function solution time dependence section of chapter III. For conciseness, at this point the wave function time-dependence is not shown as a fourth dependent variable.

From Equation (3.8) the opportunity for different computations is immediately apparent arising from the Laplacian of the wave function, \( \nabla^2 \). Since the Schrödinger equation is solved numerically, different numerical derivative stencils can be employed to increase accuracy of the computation or simply the calculations. The selected stencil is a simple three-point second-order in each spatial direction as called for by the Laplacian operator, which expands to \( \left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \right) \). The three-point stencil for the second derivative is given by the approximation, shown for the \( x \)-direction, in Equation (3.9) and illustrated in Figure 3.10.
\[ \frac{\partial^2}{\partial x^2} \approx \frac{f(x_{-1}) - 2f(x_i) + f(x_{+1})}{(\Delta x)^2} \]  

Figure 3.10: Graphical depiction of the numerical differentiation stencil for neighboring points used to approximate the second derivative, shown referenced to the central grey point. Grid points highlighted in red indicate the two nearest neighbor grid points considered in computing the x-axis partial derivative. Similarly, grid points shown in green indicate the y-axis nearest neighbors, and grid points highlighted in blue indicate the z-axis nearest neighbors. Distances indicated are normalized to the grid point separation in each direction.

To represent the spatial partial derivatives on each point, a matrix corresponding to each partial derivative term is computed based on the arrangement of the potential vector in the computation. The general form is a matrix such that the main diagonal is assigned a value of \( \frac{-2}{(\Delta x)^2} \), with the “\( \Delta x \)” term substituted for the grid point spacing in the direction of interest. The remaining terms in the stencil, which correspond to the forward
(“$i + 1$”) and backward (“$i - 1$”) components of 29, are given by a block form having the value $\frac{1}{(\Delta x)^2}$ or zeros with the particular shape dictated by the ordering of the potential vector. Of note is the fact that all terms in the derivative stencil have the same “$\Delta x$” dependence. This aspect of the stencils plays an important role when considering crystal expansion and contraction along specific directions, which in turn elongates or shortens the spatial step taken. To correct for this, as expanded upon in the ferroelectric crystal distortion section in chapter III, each stencil is multiplied by the square inverse of the scale factor in the $i$-direction, $\gamma_i$, for that stencil’s direction, where the scale factor is defined by Equation (3.10).

$$\gamma_i = \frac{\text{Unit Cell Length in } i\text{-direction}}{\text{Lattice Constant (thermally averaged)}}$$

(3.10)

For each basis vector in the coordinate system defined in Figure 2.3, a scale factor representing the crystal expansion or contraction along that axis is computed. Therefore, for each of the numerical derivative matrices, of which there are three, a different scale factor is used to appropriately develop an approximation of the derivative along that axis. The scale factor presented in Equation (3.10) is squared prior to use in this case as the terms of the stencil take on units of cm$^{-2}$. Crystal distortion is measured relative to the thermally averaged cubic PZT lattice constant, 3.9135 Å.

The potential for higher order numerical stencils exists as well, which may be leveraged to increase the resolution of the model. Because in this implementation of the ion potential the stencil remains static with time, schemes with higher accuracy can be employed with marginal, if any, run time increase. A prime example of this lies in the estimation of the second derivative for each point within the grid, where the current method obtains an error of the order $h^2$, where $h$ is the step size. Additionally, the
symmetric difference approach used here can lead to undesirable roundoff errors as the steps are made very small, as is the case here for the small dimensions of interest.

With the potential, represented by a matrix with the potential along the diagonal, and the Laplacian specified, the spatial components of the time invariant, or stationary, wave function states and corresponding state energies are obtained by solving for the eigenvalues and eigenvectors of the resulting matrix. In the example of a twenty-five-point grid along each of the three spatial basis vectors, a $15,625 \times 15,625$ matrix results ($25^3 \times 25^3$). This matrix corresponds to 15,625 possible eigenstates, some of which may be degenerate – or having the same energy [115, 116]. An example of this is shown in Figure 3.11 for a lead ion core with the eigenvalues corresponding to the 15,625 energies. Close examinations of the computed energies show many degenerate states, with only 14,675 unique energies. Within this work, first any eigenstates having a complex energy with the imaginary component not equal to zero are removed. Next, only the ten lowest energy states are considered (an adjustable parameter). Though initially only the computed ground state, or lowest energy state, was used, the number of possible states was expanded slightly to accommodate higher energy states near the computed ground state. A comparison of the probability density function (PDF) between the computed ground state and the superposition of the first ten states is observed by comparing Figure 3.12 and Figure 3.13. Because the evaluated volume is small ($3.43 \times 10^{-25}$ cm$^3$), the PDF after normalization takes on values that would otherwise seem excessively large, often $10^{25}$ or larger for harmonics of small order.
Figure 3.11: Eigenstate energies assessed for a lead ion core using twenty-five grid points along each spatial basis vector.

Figure 3.12: Probability density function of the estimated ground state from the calculated eigenstates, shown for the \( z = 0 \) cm plane using twenty-five grid points along each spatial basis vector under a weak electric field along the positive \( x \)-axis with \( c \) lattice parameter of \( 4.135 \) Å.
Figure 3.13: Probability density function of the superposition of the first ten calculated eigenstates, shown for the $z = 0$ cm plane using twenty-five grid points along each spatial basis vector under a weak electric field along the positive $x$-axis with lattice parameter of 4.135 Å.

Since the sum over all possibilities must equal unity, wave functions are normalized to ensure this property is satisfied. The wave function $\Psi$, which is a probability amplitude, is related to the probability density function, $P$, by its complex conjugate, denoted by $\Psi^*$, through Equation (3.11).

$$P = \Psi^*\Psi$$  \hspace{1cm} (3.11)

The PDF is normalized such that here the integral over all space is unity, namely the integral of the product of the wave function complex conjugate and the wave function as shown in Equation (3.12).

$$\iiint dx \, dy \, dz \, \Psi^*\Psi = 1$$  \hspace{1cm} (3.12)

At this point the total wave function, $\Psi$, will be replaced with the spatial component, $\psi$, as Equation (3.11) and Equation (3.12) are solved initially considering only a time-
invariant system. Therefore, each possible, evaluated wave function (now denoted as \( \psi \)) is normalized individually over the volume of interest, and the superposition of states results from the normalized sum of each wave function. As this would typically result in having a superposition of states with PDF exceeding unity within the volume of interest, the composite wave function is itself normalized according to Equation (3.13).

\[
\psi = \frac{1}{\sqrt{n}} \sum_{i=1}^{n} \psi_i
\]  

(3.13)

This construction of the general wave function, \( \psi \), as a function of the possible states, \( \psi_i \), gives equal credence to all allowed wave functions. That is so say, each considered wave function receives equal weighting proportional to the number of states used to construct the overall wave function. More generally, the superposition will take on a form with each solution to the time invariant Schrödinger equation, \( \psi_i \), contributing a portion ascribed by a coefficient \( c_i \) as in Equation (3.14).

\[
\psi = \sum_{i=1}^{n} c_i \psi_i
\]  

(3.14)

As a result, evaluating the integral of the wave function in Equation (3.13) over all space as in Equation (3.12) yields unity. The reason for this relation is that each of the eigenvectors, \( \psi_i \), are orthogonal, meaning that the integral as indicated in Equation (3.15) is true for any two different wave functions.

\[
\iiint dx \; dy \; dz \; \psi_i^* \psi_j = 0, \quad \text{for all } i \neq j
\]  

(3.15)

\[\text{(iv) Dipole Moment Calculation}\]

The dipole moment evaluated for all ions in the PZT unit cell forms the basis for all polarization calculations. In order to determine the dipole moment, corresponding to the displacement of each ion and the substructure, all ions within the ferroelectric material begin at the thermally averaged locations (i.e., no displacement) with the unit
cell taking on a cubic structure. The potential applied across the PZT crystal, if any, combined with the potential arising from ion-ion interactions determines the movement and resulting displacement of each ion. Since no ion displacements exist initially but are expected, the potential computed is not expected to be accurate for the initial evaluation. This initial inaccuracy is due to the assumption of the initial condition of the state of the system, that is, that the system is in a cubic state with no displacement. As a result, there is some non-zero time for the modeled crystal to transition from a thermally averaged state to a steady-state solution given the applied potential, temperature, and ion locations. Therefore, to accommodate this abrupt change in the system, the wave function computed from the first pass is used in computing an approximation of each ion displacement, as given by Equation (3.16).

\[ \langle x \rangle = \iiint dx \, dy \, dz \, \psi^* \, x \, \psi \] (3.16)

In general, the expectation value of an observable, such as position, is given by Equation (3.17), where the operator, shown as \( \hat{A} \) though typically specified with the accent omitted, acts on the wave function and is multiplied by the complex conjugate of the wave function, integrated over all space.

\[ \langle A \rangle = \iiint dx \, dy \, dz \, \psi^* \, \hat{A} \, \psi \] (3.17)

The result of this calculation is the expectation value, \( \langle A \rangle \), that is the average of infinitely many measurements on systems having the same wave function. Though in general the wave function will not necessarily be integrated over a volume, such as the case for a wave function in a single spatial dimension, in this work the wave function is exclusively a function of the spatial coordinates and time. Since only a single observable, or observable quantity, may be assessed at a time, as shown for \( x \) in Equation (3.16),
complete displacement computation requires three separate calculations to arrive at the resulting position, \((x, y, z)\). This expected position does not, however, directly coincide with the displacement of the ion. If, for example, in a single dimension there exists equal probability to find an ion with some symmetric, non-zero displacement about \(x = 0\), the resulting expectation value of \(x\) will of course be zero. However, the expectation of the displacement, that is \(\langle |x| \rangle\), of said ion will be non-zero. When evaluating each ion or each ion component (core and shell), the coordinate system is centered at the thermally averaged location. This allows the computation to calculate the expectation of the position directly, which is then referenced to the thermally averaged position to compute an estimate of the displacement.

An iterative method is employed for the model start up resulting from the coupling between a large number of ions. With the ion locations updated from the first pass through the crystal, a second pass is performed, still at the initial time, \(t = 0\) s. Now all ions have an approximation of the displacement, and the resulting potential calculation is significantly more accurate. Again, the wave function is calculated for each ion and its components, with each core and shell taking on a new displacement owing to Equation (3.16). The polarization and ionic potentials adjust slightly after the second pass, making the polarization more accurate. This iterative procedure is repeated until the polarization change between iteration is deemed to be minor, here taken to be less than a 1-2 \(\mu\text{C/cm}^2\) change on any two successive iterations. Essentially, this is allowing the crystal to settle to a steady-state condition, but only at start-up. As this would be similar to evaluating the crystal after given an arbitrarily long amount of time passed so as to allow the transient response to settle, this is useful only in defining an initial
condition for the system. In the case of a time-varying environment, the ion positions update from a single calculation given the current electric field as detailed in the time-varying section of chapter III.

Similar to treatment of the ion shell displacement, the ion as a whole, primarily meaning the ion core displacement, is assumed not to leave the unit cell. This assumption means that the crystal is assumed to not be damaged as a result of applied electric fields. To accommodate this assumption, all displacements are limited to 0.7 Å in any particular direction. This equates to an overall maximum displacement of approximately 1.2 Å if maximally displaced in each of the three directions, which is far outside the expected maximum displacement of 0.5 Å albeit principally in a single direction only.

Having computed the expectation value for the displaced position, the resulting dipole moment is found directly. The electric dipole moment, \( p \) (esu \( \cdot \) cm), is given by the product of displaced charge and the displacement, as shown in Equation (2.8). Using the known charge of the ion and the displacement, the electric dipole moment is calculated for each ion in the ferroelectric crystal. The displacement vector of the ion shell includes the displacement of the ion core, as the ion shell displacement is internally computed relative to the expectation of the core position. Since the shell and core charges sum to the net ion charge, the independent location of the shell and core can lead to dipole moments larger – or smaller – than found with an assumed point charge of the net ion charge. This creates an interesting condition for the system, wherein a positive core displacement typically results in a shell displacement in the opposite direction increasing the contribution to the polarization of the overall ferroelectric layer.
It is at this point that motion of the ions may be allowed to influence the potential as well. As each ion carries with it a charge, the velocity of the ions, though small on average, can be used to influence the potential calculation. However, it is usually the momentum, rather than the velocity directly, that is considered. In this manner, the expectation value of the momentum of the ion core and shell can be computed from the respective wave functions as shown for the \( x \) direction in Equation (3.18).

\[
\langle p_x \rangle = \iiint dx \, dy \, dz \, \psi^* \left( \frac{\hbar}{i} \frac{\partial}{\partial x} \right) \psi \tag{3.18}
\]

With the wave function known (or approximated given the assumptions of the potential and calculation methods) and producing a non-zero expected velocity for each charge, the resulting vector potential, \( A \), can be calculated as shown by Equation (3.19) for the \( x \) component.

\[
A_x(x, y, z) = \frac{1}{c} \int dx' \, dy' \, d z' \frac{J_x(x', y', z')}{|(x, y, z) - (x', y', z')|} \tag{3.19}
\]

The vector potential, \( A \), and all non-constant terms defining it are functions of time, though the time dependence is omitted from Equation (3.19). As shown by the relationship given by Equation (3.19), the vector potential is related to the current density, \( J \), necessitating the computation of the velocity, by way of momentum, of each charge. Similarly, with the vector potential now defined the electric field may be written to include a time-varying term as a function of the vector potential, as given by Equation (3.20).

\[
E = -\nabla \phi - \frac{1}{c} \frac{\partial A}{\partial t} \tag{3.20}
\]

From Equation (3.20), the contribution to the potential is directly added using the time-varying nature of the vector potential. This additional computation may be used to
influence the potential and thereby the dipole moment as evaluated in the model when determining displacements and resulting dipole moment.

(v) Polarization Computation

With the electric dipole moment for each ion in the ferroelectric crystal determined, the electric polarization or polarization density, \( P \) (esu \( \cdot \) cm\(^{-2} \)), of the layer is found simply by dividing the total dipole moment by the total volume. Since a small subset of the unit cells in the entire ferroelectric layer are simulated in the model, the polarization density is computed equivalently as shown in Equation (3.21).

\[
P = \frac{1}{V_{\text{UnitCell} \cdot \text{CellCount}}} \left( \sum_{Pb} \delta + \sum_{Zr} \delta + \sum_{Ti} \delta \right).
\]

where \( \delta = (q_{\text{core}} \cdot d_{\text{core}} + q_{\text{shell}} \cdot (d_{\text{core}} + d_{\text{shell}})) \)  

Here the displacement vectors, \( d \), are measured relative to the thermally averaged location of the ion, with the shell displacement computed relative to the core displacement specifically. Additionally, the unit cell volume, \( V_{\text{UnitCell}} \), is the instantaneous volume measurement, to include the volumetric changes undergone by polarization induced crystal expansion or contraction along any dimension. The unit cell count, \( \text{CellCount} \), shown as an evaluation of the number of unit cells measured, does not include any of the padding cells, which are not included in any earlier summation terms either.

The polarization computation is assessed for each domain modeled in the ferroelectric crystal. Since the current implementation of the model does not enforce similar displacements for the ions across the group of unit cells referred to as the domain, the only shared attribute is the physical dimensions from the piezoelectric response of the crystal. However, the model can be expanded to assess an arbitrary number of adjacent
domains interacting with one another according to the potential terms defined by a combination of ion-ion interaction and/or potential arising from the neighboring domain polarization.

Polarization as computed in this chapter is used in the semiconductor model that determines the semiconductor potential, ultimately influencing the current observed in the FeFET. To accomplish this, the polarization is extrapolated to be uniform across the ferroelectric crystal with the polarization determined by Equation (3.21). Additionally, the potential of the ferroelectric material at the interface is assumed to be constant, or not varying at each point in the material spanning from the source to drain. This simplification may be seen in practice for device fabrication and modeling, at least preliminarily, by placing a thin conductor alongside the ferroelectric material thereby creating a constant potential while also serving to help isolate the PZT layer. Alternate fabrication methods necessitate the use of different materials and still attempt to isolate the reactive ferroelectric materials. This simplifying assumption alleviates any issues that may arise in early manufacturing stemming from the ferroelectric layer incorporation in the device, which can be an issue due to how reactive PZT is with silicon. Similarly, this assumption simplifies the potential terms for initial modeling of devices, allowing more rapid modeling of potential device designs.

(vi) Ferroelectric Crystal Distortion

In the presence of an applied electric field, the ferroelectric crystal distorts according to the piezoelectric response of the material. For PZT, the distortion is dictated by the composition of the material in addition to factors such as temperature. Using 20/80 PZT, shown in Figure 2.5 by the 80% PbTiO$_3$ vertical line, the unit cell is
tetragonal and has a significant difference between the $a$, $b$, and $c$ lattice parameters. In this model, this crystal distortion is determined by the polarization of the ferroelectric layer, which is determined by both the applied electric field, if any, and the past polarization for retention computations.

The expansion along a single direction from the thermally averaged lattice constant of approximately $a = b = c = 4 \, \text{Å}$ is given by a transition function, which is shown in Equation (3.22) for the case of the polarization lying principally in a single direction.

$$
\gamma_l = \frac{4.135 \, \text{Å}}{4.0 \, \text{Å}} = 1.03375
$$

The two remaining dimensions are assigned a lattice constant of 3.9135 Å, resulting in a scale factor of 0.978375. For retention computations or if the polarization reverses as may be expected over the course of a circuit simulation, the expansion is defined such that as the polarization rotates to align equally with multiple spatial basis vectors, the expansion along the now former principal dimension is reduced slightly as expansion along a different axis occurs. The end result is that the volume of the unit cell and therefore the overall ferroelectric crystal is nearly invariant as the polarization changes. This is not necessarily required, but having the polarization depend on the volume of the assessed unit cells, as shown in Equation (2.7), encourages a smooth transition with respect to volume so that abrupt changes are not induced while modeling this phenomenon. As such, the transition function is chosen to reduce the elongation in any particular direction according to the number of axes that have the maximum polarization. If the maximum component of the polarization as projected onto each of the three spatial
basis vectors is found to equal between any axis pair or triplet (referred to as the principal polarization axis), the scale factor is instead given by Equation (3.23).

\[
\gamma_i = 1 + \frac{4.135\text{Å} - 3.9135\text{Å}}{4.0\text{Å} \cdot \left(\text{Num. of Principal Polarization Axes}\right)}
\]  

(3.23)

A graph showing the unit cell volume as a function of the number of principal polarization axes is shown in Figure 3.14.

![Figure 3.14: PZT unit cell volume in Ångstroms as a function of number of principal polarization axes and resulting crystal structure (abscissa). Also shown are the volumes of a cubic structure taking on the lesser (a\(^3\)) and greater (c\(^3\)) of the two lattice parameters for a tetragonal PZT cell](image)

**(vii) Solution Time Dependence**

The time dependence of the ferroelectric crystal polarization is determined by assessing the time-dependent Schrödinger equation as given by Equation (3.24).

\[
H\Psi = i\hbar \frac{\partial \Psi}{\partial t},
\]

where  
\[
H = -\frac{\hbar^2}{2m} \nabla^2 + U
\]  

(3.24)
This methodology of first solving a time-invariant system, as specified earlier using Equation (3.8), and pivoting to use that solution for time propagation is often employed when solving for the wave function since systems for which the time-dependent Schrödinger equation may be solved directly are especially rare. If the wave function satisfying the (time-dependent) Schrödinger, given by Equation (3.24), is separable in time and space, then the wave function can be expressed as in Equation (3.25).

\[ \Psi = \psi(x, y, z) \cdot \varphi(t) \quad (3.25) \]

In this case, the wave function is decomposed into the product of two functions, one purely relating to spatial coordinates (\( \psi \)) and one relating only to time (\( \varphi \)). When Equation (3.25) is substituted back into Equation (3.24), the dependent variables are immediately seen to be separable. That is to say, all terms with a spatial dependence (\( x, y, \) and \( z \)) may be grouped together and all terms with a time dependence may be similarly grouped together. In this manner, the spatial and time components of the equation are equal to one another as in Equation (3.26).

\[ \left( -\frac{\hbar^2}{2m} \left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \right) + U(x, y, z) \right) \frac{\psi(x, y, z)}{\varphi(t)} = \frac{i\hbar \omega(\xi)}{c} \frac{\varphi(t)}{\varphi(t)} \quad (3.26) \]

Since each side varies depending only on a different variable (or set of variables), both sides of Equation (3.26) must be precisely equal to a constant. This constant term is taken as the energy, \( E \), which results from the fact that the Hamiltonian operator, \( H \), shows each measurement of the system’s energy results in a single value, \( E \), for the energy owing to the variance obtained from the operator acting on the wave function. Evaluation of the time-dependent Schrödinger equation from Equation (3.24) allows the computed wave function to propagate in time, thereby revealing the time evolution of the system. Similar to the consideration of the spatial derivatives specified
by the Hamiltonian operator, $H$, in Equation (3.24), the partial derivative with respect to
time requires a choice of numerical differentiation stencil. As is often performed when
generating an initial estimate, a first order approximation may be used to simply generate
the estimate of the wave function at $t = t + \Delta t$, corresponding to $\psi_{i+1}$, as shown in
Equation (3.27), which may then be used as the basis for higher order schemes.

\[
\frac{\partial}{\partial t} \approx \frac{\psi_{i+1} - \psi_i}{\Delta t}
\]  \hspace{1cm} (3.27)

Since the numerical differentiation scheme shown in Equation (3.27) is only a first order
in time scheme, more accurate schemes may need to be employed for higher accuracy.

Furthermore, as the derivative can be represented by a matrix that, assuming a constant
time step, will not change form over the course of the simulation, an arbitrary stencil can
be used. The more taxing operation of computing the matrix inverse need only be
performed during the model startup, rather than at each time step, owing to this fact. If a
variable time step is desired, a time step adjustment factor akin to the one shown for
spatial derivatives in Equation (3.10) can be used. Initially the time scale is kept small,
on the order of femtoseconds. Using a time step of this magnitude would result in
smaller errors, which are proportional to the time step used, however the resulting
simulation durations are considerably less useful. Additionally, errors from the spatial
derivatives specified in Equation (3.24) are also a factor in overall accuracy. Since the
spatial coordinates are a contributing factor due number of assessed ions as well as
computing resources, a balance must be struck between the different simulation settings.

Arising from small rounding errors, the wave function for each ion component is
normalized at each time step prior to computing the expectation of the position.

Normalization should be calculated prior to computing any of the observables from the
wave function, as a small error can ripple through the solution quickly. If this were allowed, first the position will be skewed owing to the relation given by Equation (3.28), wherein the not yet normalized wave function is represented by $\phi$ and shown to be integrated over $x$ alone.

$$\int dx \, \phi^* \phi = \xi \int dx \, \Psi^* \Psi$$

(3.28)

The resulting error factor, $\xi$, essentially acts as a scale factor on the wave function. In this case, the error may take on a value greater or less than unity, where the actual error factor acting on the single wave function is $\sqrt{\xi}$. This error influences any observable computed from the incorrect wave function, $\phi$, which then may be used in updating the position expectation. Quickly the position inaccuracy influences the potential of all neighboring ions in addition to the ion itself, leading to further inaccurate predictions of the ferroelectric material time evolution. The physical representation can be seen from this as well. If the wave function were allowed to take on a value such that the integral of the PDF, given by $\Psi^* \Psi$, over the evaluated volume does not equal unity, then the probability of finding the ion in the volume is either less than unity, which indicates crystal damage from ion dislocation, or exceeds unity, which is nonphysical.

As the wave function for each ion core and shell propagates in time, the expectation of the displacement is computed to ensure accurate potential computations on the following time step. Similarly, the polarization too updates which may necessitate an updated crystalline distortion via the scale factor along each dimension. At this point, for each time step the system is completely defined and updated to the current measurement time. The polarization found at each time step can then be used to compute the potential
of any neighboring materials, such as an adjacent semiconductor as is the case in the transistor model.

B. Transistor Model

The ferroelectric transistor model outlined in this section is capable of defining the operation and behavior of the transistor as either a standalone device or incorporated in circuits. In addition to the model of the ferroelectric material, the overall transistor model incorporates a semiconductor model to complete the device. In this manner, the influence of the ferroelectric material on the semiconductor is demonstrated. Ferroelectric material polarization influences the channel conductivity, which in turn influences the polarization. Polarization retention properties of the ferroelectric material are also influenced by the terminal voltages and current through the semiconductor.

The overarching model of the transistor is similar to that of a JFET, which incorporates the PN junction as the principal governing factor of current. PZT, taken to have a carrier concentration of approximately $4.4 \times 10^{20} \text{ cm}^{-3}$ based on empirical current measurements, acts as a p-type material in the transistor. Conversely, Indium Oxide (InOx, In$_2$O$_3$) acts as an n-type material having a carrier concentration of approximately $6.3 \times 10^{18} \text{ cm}^{-3}$. The interaction between the two materials at the interface results in a depletion region, largely devoid of charge. As the depletion region grows, such as with applied negative gate voltages, the channel in the semiconductor shrinks as shown in Figure 3.15. On the other hand, if the gate voltage is positive, the depletion region is made smaller [78, 136, 137]. Similarly, as the polarization in effect acts as an additional bias voltage to the junction, the effects of varying polarization state across for a constant
applied gate voltage are shown in Figure 3.16. This operation is expanded upon in detail in the semiconductor modeling section of this chapter.

Figure 3.15: Depletion region depth in the n-type semiconductor as the applied gate voltage varies from -5 V to 5 V for constant polarization states. The depletion region is only allowed to vary between 10 nm and 20 nm owing to the thickness of the semiconductor material.
Figure 3.16: Depletion region depth in the n-type semiconductor for varying polarization states. In the FeFET InOx acts as the n-type semiconductor, and PZT acts as the p-type semiconductor. Maximum depletion region depth is restricted to 20 nm owing to the thickness of the InOx semiconductor layer.

(i) **Use of Ferroelectric Model**

The ferroelectric material model outlined earlier in chapter III is the primary focus of the FeFET model as it is this feature that primarily distinguishes the FeFET from other transistors. Ferroelectric material polarization is initially set during the device or circuit startup. In this way, polarization of the ferroelectric material is well-defined. As mentioned previously, the modeled domain of the ferroelectric layer is expanded or extrapolated across the entirety of the semiconductor interface. Essentially this assumes the ferroelectric layer on average is represented by the smaller ferroelectric domain, which is required to enable longer simulations by shortening run time.

Additionally, no current is assumed to flow from the ferroelectric layer to the semiconductor. This assumption is similar to having a thin insulator between the PZT and semiconductor. However, were the insulator present then the interface characteristics would be altered, which is not modeled. Lastly, the polarization is considered largely uniform. This final assumption arises from the fact that the ferroelectric domain is extrapolated across the semiconductor. Small variations in electric polarization across the modeled domain are expected from ion-ion interactions, edge conditions, and potentially computation ordering.

(ii) **Semiconductor Channel**

Using the PZT polarization; applied gate voltage, if any; and both the source and drain terminal voltages, the potential in the semiconductor is found directly. As stated previously, the PZT and indium oxide (InOx, In₂O₃) layers form a PN junction, with PZT
acting as a p-type semiconductor due to the lead oxidation states and indium oxide serving as an n-type semiconductor. For indium oxide, the carrier density is assumed to be $6.3 \times 10^{18}$ cm$^{-3}$, and the carrier mobility is 5.8 cm$^2$/V·s. At the interface between the p-type and n-type materials, a depletion region forms, wherein carriers (electrons) from the indium oxide migrate toward the positively charged lead ions in the PZT layer. The depletion region depth modulates the size of the conducting channel and therefore the channel resistance of the transistor. The source and drain each have 100 nm-thick platinum contacts where the width and length vary with transistor dimensions, which affect the semiconductor potential as well.

Within the semiconductor, the primary point of interest is the depletion depth as it is the principal factor in determining the drain current. To compute the depletion region depth into the InOx channel, Poisson’s equation is used, as given by Equation (3.29) for a uniform charge distribution.

$$-\frac{d^2V}{dx^2} = \frac{dE_x}{dx} = \frac{\rho(x)}{\varepsilon}$$  \hspace{1cm} (3.29)

To simplify the modeled charge distribution, the “depletion approximation” (sometimes referred to as “full depletion approximation”) is used. Within the semiconductor material, this approximation assumes that the entirety of the depletion region is fully depleted of carriers, which is to say that the charge density in the region is equal to zero. Equivalently stated, within the depletion region the space charge used in Poisson’s equation is equal to the opposite of the carrier charge multiplied by the carrier concentration ($-qN_A$ or $qN_D$). This charge distribution is shown graphically in Figure 3.17 for both the depletion approximation and what would be realized without the assumption.
Figure 3.17: Space charge used in Poisson’s equation as considered in the full depletion approximation (solid line) and approximate distribution without the simplifying assumption (dashed line). The p-type material composes all points for $x < 0$ and the n-type material lies for all points $x > 0$.

From Equation (3.29), the resulting electric field is easily obtained via integration over the region of interest as shown to be $-x_p$ to $x_n$ in Figure 3.17. By using the depletion approximation, the electric field is then calculated to be simply linearly decreasing in the p-type material, having slope equal to the permittivity. At the interface, the electric field remains continuous and linearly increases, according to the material permittivity, to zero at the end of the depletion region in the n-type material as shown in Figure 3.18. The electric field at the interface, given Equation (3.30), is of particular interest as it yields one of the conditions used to derive the depletion region depth.

$$-E_{x,max} = -\frac{q N_a x_p}{\epsilon_a} = -\frac{q N_d x_n}{\epsilon_d}$$  \hspace{1cm} (3.30)

Owing to the permittivity differences of the materials, the notation of $\epsilon_a$ and $\epsilon_d$ is adopted to capture permittivity in the p-type (“acceptor-doped”) material and n-type
Integrating Equation (3.29) twice results in the second equation needed to solve for the built-in potential, $\phi_l$, and applied voltage, $V_a$, given by Equation (3.31).

$$\phi_l - V_a = \frac{q}{2} \left( \frac{N_d}{\epsilon d} x_n^2 + \frac{N_a}{\epsilon a} x_p^2 \right)$$

(3.31)

Substituting Equation (3.30) into Equation (3.31), gives the general form for the depletion depth into the n-type material as a function of the carrier concentrations, relative permittivity, and potential terms as shown by Equation (3.32).

$$x_n = \sqrt{\frac{2}{q} \frac{N_a \epsilon_a^2}{N_a N_d \epsilon_d + \epsilon_a N_d^2} \left( \phi_l - V_a \right)}$$

(3.32)

Figure 3.18: Electric field variation across the depletion region in the p-type ($x < 0$) and n-type ($x > 0$) materials as computed using the depletion approximation.

With the depletion region depth into the n-type semiconductor obtained from Equation (3.32), the current in the FeFET is found directly by Equation (3.33).

$$I = N_d e \mu V_{ds} \frac{W}{l} \left( T_s - x_n \right)$$

(3.33)

In this form, the current of the FeFET now looks similar to that of a resistor, controllable by the depletion region depth. This is form is due to the operation similar to that of a JFET wherein the depletion region depth dictates the current level by restricting current
flow to varying degrees. Each of the parameters, with the exception of the drain-to-source voltage, $V_{ds}$, and depletion region depth, $x_n$, are outlined in Table 3.4. Of note is the total semiconductor thickness, $T_s$, is 20 nm in the devices of interest in this work, which provides a theoretical maximum current were the depletion depth reduced completely.

Table 3.4: FeFET fabrication parameters used in current calculation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_d$</td>
<td>$6.3 \times 10^{18}$</td>
<td>InOx carrier concentration</td>
</tr>
<tr>
<td>$\mu$</td>
<td>5.8 cm$^2$/V s</td>
<td>InOx mobility</td>
</tr>
<tr>
<td>$W$</td>
<td>10, 40, 400 µm</td>
<td>Channel Width (ND1, ND4, ND7)</td>
</tr>
<tr>
<td>$L$</td>
<td>10, 40, 4 µm</td>
<td>Channel Length (ND1, ND4, ND7)</td>
</tr>
<tr>
<td>$T_s$</td>
<td>20 nm</td>
<td>Semiconductor thickness</td>
</tr>
</tbody>
</table>

An interesting parallel may be made by comparing the FeFET current equation with the resistance of a material of length $L$ and cross section area $W \cdot (T_s - x_n)$. Where the resistance of the channel is found via Ohm’s law, the resistivity of the channel, $\rho$, is similarly computed as a function of the fabrication parameters as given by Equation (3.34).

$$R = \frac{V_{ds}}{I} = \left( \frac{1}{N_d e \mu} \right) \frac{L}{W \cdot (T_s - x_n)} = \rho \frac{L}{W \cdot (T_s - x_n)} \quad (3.34)$$

This view of the FeFET current may be of particular help for circuit design or fabrication. Since FeFETs are used primarily in digital circuits, the channel resistance, which dictates
an “on” or “off” state of the device, may be of more use than the current. Conversely, for analog circuit design where current is often a focal point, the resistance may be decreased by adjusting any combination of channel width, channel length, or even carrier concentration and mobility via different fabrication techniques. The variability of the depletion depth, which the only post-fabrication controllable variable other than drain voltage, can also necessitate smaller semiconductor thickness. As the semiconductor thickness increases, the depletion depth must modulate more substantially in order to affect a significant on/off ratio for the device. As the on/off ratio for a FeFET decreases, the dependence on polarization state is in turn diminished, which may impact the effectiveness of the design.

An additional potential term dictating the depletion depth into the semiconductor arises from the ferroelectric layer polarization. To understand the origins of this potential term, $V_{pol}$, the charge arising from the polarization is assumed to contribute to the depletion region depth in the p-type material (PZT) way of the space charge contribution. In the event of a negative polarization, additional negative charge is added to the depletion region in the p-type material requiring less positive charge accumulation in the n-type material (InOx) by way of reduced negative charge migration. This reduced charge in the n-type material has the net effect of decreasing the depletion region depth, according to the relative permittivity and carrier concentration of each material. For the FeFET operation, this will serve to increase the drain current as the channel is less restricted. The opposite holds as well, wherein a positive charge accumulating in the p-type material will affect an increase in the n-type material depletion region again according to the material characteristics. An important assumption here is that the
polarization in the PZT layer is effectively able to add to or remove charge from the depletion region. The result is the polarization charge contributing to the electric field at the interface, determined by the charge deposited and permittivity of the PZT material as given by a modified variant of Equation (3.30) shown in Equation (3.35).

$$-E_{x,max,pot} = -\frac{q N_a x_p + P}{\epsilon_a} = -\frac{q N_d x_n}{\epsilon_d}$$  \hspace{1cm} (3.35)

In this configuration, the polarization, $P$, having units of charge per unit area is used to modify the charge in the PZT depletion region. Charge in the InOx semiconductor then must balance with the additional charge, thereby adjusting the depletion region depth into the semiconductor channel. Because the electric field in the InOx layer is assumed to increase linearly across the depletion region extent, the additional depth is therefore given by Equation (3.36).

$$\Delta x_{n,pot} = \frac{P \epsilon_d}{\epsilon_a q N_d}$$  \hspace{1cm} (3.36)

Of particular importance for the devices in question is the accuracy of the depletion approximation in the face of the thin semiconductor material, exacerbated by the assumption of the polarization effectively depositing additional charge in the depletion region. Applying the depletion approximation to empirical data yields varying results as shown in Table 3.5, which is expected due to manufacturing tolerances. While the channel is intended to be only 20 nm thick, manufacturing tolerances allow this to increase as high as 40 nm for some devices. As the channel turns off as a result of the depletion region encroaching on the channel to the extent allowed, a small minimum current is observed in all devices [90, 91]. It is this point that indicates a possible improvement of the semiconductor model in using a more accurate depiction of the space
charge in the semiconductor region where the depletion depth extends throughout the semiconductor but is not equal to the maximum value, \( qN_d \).

Table 3.5: Depletion region depth into the n-type semiconductor using the depletion approximation applied to collected experimental data

<table>
<thead>
<tr>
<th>FeFET</th>
<th>( x_{n,\text{on}} ) (cm)</th>
<th>( x_{n,\text{off}} ) (cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ND1</td>
<td>1.15E-06</td>
<td>1.95E-06</td>
</tr>
<tr>
<td>ND4</td>
<td>8.26E-07</td>
<td>1.93E-06</td>
</tr>
<tr>
<td>ND7</td>
<td>1.57E-06</td>
<td>1.98E-06</td>
</tr>
<tr>
<td>Average</td>
<td>1.18E-06</td>
<td>1.95E-06</td>
</tr>
</tbody>
</table>

Due to the variability between samples, the modeled parameters were created using an average across the representative samples. To this end, the effective carrier concentration of the PZT material and built-in potential of the junction are computed to align with the experimental data. This is done to fit an average of the samples evaluated for a known polarization state such that the additional potential term from the polarization may be evaluated in addition to the known applied gate voltage. Using these empirical data, the carrier concentration of PZT is determined to be \( 4.4 \times 10^{20} \) cm\(^{-3} \), which likely higher than the actual value. Likewise, the built-in potential is determined to be 4.5 V. This selected value for built-in potential can create some issues for large gate voltages. Though not used often out of concerns for damaging the FeFETs, large gate voltages can cause the depletion depth to take on an imaginary value if simply computed directly. This is accounted for in the semiconductor model by simply having a minimum depletion depth, computed from the experimental currents with the FeFET channel completely turned on. To institute a soft transition as observed in the experimental data, exponential functions by way of the hyperbolic tangent function are used to develop a
tapered yet mathematically smooth drain current under varying gate voltages. Though not easily physically realizable, this can be seen by holding the polarization state steady while varying the gate voltage as shown in Figure 3.19. Similarly to examine the effects of the polarization on the drain current, drain current modeled for varying polarization states with a constant gate voltage is shown in Figure 3.20, such as may be the case for a FeFET being controlled primarily by the ferroelectric layer piezoelectric response.

Figure 3.19: Modeled FeFET drain current for constant polarization states ranging from -100 μC/cm² to 100 μC/cm² with 4 V applied at the drain
Figure 3.20: Modeled FeFET drain current with varying ferroelectric layer polarization for an applied drain voltage of 4 V

Within the model, retention is treated simply as a subset of the general semiconductor potential configuration, having the gate voltage set to 0 V. In this case, if the voltages applied at both the source and drain contacts are also zero, the zero-bias depletion region forms. A voltage at either the source or drain contact will alter the depletion region in precisely the same manner as an applied gate voltage. In this case, however, the depletion region will have a spatial dependence, transitioning from the depletion region induced at the source-side of the transistor \((y = 0)\) that is based on the gate and source voltages to the depletion region formed at the drain-side of the transistor \((y = L)\) that is based on the gate and drain voltages. Here the coordinate system of the FeFET is introduced as shown in Figure 3.21. Since the \(z\)-dimension lies along the transistor width direction, the potential and resulting current do not have a \(z\)-dependence.
Although not employed in the model currently, the potential for a feedback loop between the semiconductor and ferroelectric models exists. When a non-zero current is present in the semiconductor, a small magnetic induction, $B$, forms as given by the Biot and Savart law from magnetostatics as shown in Equation (3.37), which uses the current density conveniently computed earlier.

$$B(x) = \frac{1}{c} \mathbf{\nabla} \times \int d^3 x' \frac{f(x')}{|x-x'|}$$ (3.37)

Since the vector potential, $A$, is of primary interest here, it is convenient to instead compute the vector potential directly making use of a gauge transformation – the Coulomb gauge. In this case, the vector potential may be computed given the current density as shown by Equation (3.38).

$$A = \frac{1}{c} \int d^3 x' \frac{f(x')}{|x-x'|}$$ (3.38)

The electric field is defined as shown in Equation (3.39), where the magnetic vector potential, $A$, is considered.

$$E = -\mathbf{\nabla} \Phi - \frac{1}{c} \frac{\partial A}{\partial t}$$ (3.39)
The resulting current calculations are able to make use of the electric field as defined by giving consideration to the magnetic vector field and help determine the movement of electrons from the source to drain. This same small magnetic field in the channel, adjacent to the PZT layer, alters the polarization over time owing to the magnetic field influence as shown in Equation (3.5).

(iii) Gate Capacitance

The capacitance associated with the FeFET gate is influenced by three effects primarily: the polarization state and switching, the PZT and InOx layers acting as dielectrics between the gate contact and source and/or drain contacts, and the depletion region existing at the PZT-indium oxide interface. Switching of the PZT polarization generally occurs on a long timescale, corresponding to lower frequencies. Ion movement to align against other neighboring ions and the applied field is readily observable from polarization differences at varying frequencies as seen in Figure 3.22. Time dependence of the PZT polarization is directly calculable from the ferroelectric model taking into consideration the potential and propagating the solution forward in time.
Figure 3.22: ND1 FeFET gate polarization (with charge collected from the source terminal) with gate voltage frequencies ranging from 0.1 Hz to 10 kHz

At higher frequencies the contribution of PZT to the gate capacitance follows from the dielectric properties of the material, acting similar to a dielectric material. Within the FeFET, the PZT dielectric constant varies with applied frequency, as expected, and polarization state, which is unique to the ferroelectric material. The dielectric properties of PZT result in a dielectric response such that the dielectric constant is taken to be a function of the applied voltage in conjunction with the present polarization state.

The final characteristic that varies to contribute to the gate capacitance is the depletion region depth. As the voltage across the PZT-semiconductor stack changes, the depth of the depletion region modulates accordingly. Additionally, the size of the source and drain contacts changes as well, creating a compounding effect on the capacitance. As the gate voltage, or the voltage applied at the contact atop the PZT layer, decreases, the depletion region increases to the point of restricting the area of the source and drain contacts. This exact phenomenon is observed from polarization and channel potential measurements wherein the ferroelectric layer is unable to saturate as strongly in the negative direction. As the voltage across the PZT-indium oxide stack decreases, the junction is reverse biased, and the depletion region widens. This scenario is illustrated in Figure 2.13.

Capacitance of the FeFET is not modeled directly, instead the various contributions to the capacitance are modeled as a result of modeling the materials and the interactions between materials. As a result, the capacitance, a function of both voltage and polarization state, is instead computed using the definition given by Equation (3.40).
\[ C(V, P) = \frac{dq}{dv} \]  

In this manner, charge entering the source contact given a change in voltage determines the capacitance. The amount of charge entering or exiting the source is dependent on factors such as the polarization state, which results in a history dependence of the capacitance and creates a capacitance hysteresis. Additionally, the frequency at which the voltage changes influences the capacitance to a large degree. This frequency dependence demonstrates the different modes of the capacitance. At the switching points of the polarization hysteresis, the capacitance is expected to peak as shown in data collected for ferroelectric capacitors. This same principle can be expanded to the drain contact, rather than the source, to compute the gate-to-drain capacitance, \( C_{gd} \).

(iv) Remnant Current

Once the voltage applied at the gate is removed, the ferroelectric layer retains the last polarization state, which forms the basis for the widespread use of ferroelectrics in memory devices. Modification of the semiconductor potential from the remaining polarization, or partial polarization if sufficient time elapsed, allows significant current similar to a depletion mode transistor in the negatively polarized state. The time evolution of the polarization state determines the current in the device given the applied source and drain voltages, if any. In this case, the current calculation is precisely the same as the active current, with the gate voltage set to 0 V. If the source and drain voltages are also 0 V, then no steady state current exists. For memory, power to the entire circuit may be disconnected or turned off, which leads to no steady state currents being present in the circuit. In any event, current and time in the model advance as
normally with the terminal voltages fixed as dictated by the nodal voltages in the circuit. While of particular importance for the FeFET, the model operation is unchanged.

C. Comparison to Experimental Data

Verification of the model performance is conducted by comparing data produced by the model and experimental collected data for the standalone device. Principal importance is placed on accurately characterizing the transistor as a standalone device since accurate modeling of the device will then translate to any circuit in which the device is used. The main characteristic of interest is the drain current, both in active and remnant operation. To arrive at the current calculation, agreement of the model with experimental data for polarization is also required. Retention of the polarization is also demonstrated through a comparison with experimental remnant current retention.

Additionally, the 1T1C memory cell is simulated with the model to depict an accurate representation of the transistor performance in both a retention and active setting. The model is also used to simulate the ring oscillator circuit. Here, the transistor switching characteristics are highlighted, which demonstrates agreement of the capacitance of the FeFET model with experimental data.

(i) Polarization

In order to accurately characterize the ferroelectric layer performance in the transistors under test, polarization measurements are taken in both static (“single-sided”) and switching (“double-sided”) configurations. The two settings are characterized chiefly by the number of channel connections made. In the static configuration, only the source or drain is connected while the remaining channel connection is left open. In the switching configuration, both channel contacts are connected, with the drain having a
positive voltage applied. Evaluation of the transistors under both conditions is needed in order to determine responses of the devices under test in an environment similar to what would be used in both digital and radio frequency circuits as well as isolating different aspects of the semiconductor response. Though digital circuit performance includes abrupt transitions in applied voltages, long periods of essentially constant voltages lead to a nearly static operation for a fraction of the cycle determined by the frequency of operation and transient characteristics of the circuit. Radio frequency or analog circuits in general have voltages that essentially always vary, as opposed to the nearly piecewise-continuous nature of the digital circuits. This results in RF circuits having a performance more closely defined by the “dynamic” operation of the FeFET.

First, static polarization measurements are collected by keeping all terminal voltages constant over the duration of each measurement using a discretized waveform produced by the Precision Premier II ferroelectric tester from Radiant Technologies, Inc. in a configuration similar to that shown in Figure 3.23. Due to symmetry of the transistors, either the source or drain contact can be connected to the tester “Return” terminal. A notional triangle waveform is shown in Figure 3.24, where the line segments of constant voltage indicate the portion of the waveform during which measurements are collected. This polarization data demonstrates the fundamental ferroelectric layer operation and indicates parameters such as polarization saturation as shown in Figure 3.25. As the waveform frequency increases, a time dependence is revealed through the time required to polarize the transistor. This time is related to the electric field applied across the ferroelectric layer, as seen in capacitors. Whereas when dealing with capacitors the electric field is simply determined by the ferroelectric layer thickness.
and applied voltage, in the FeFET the semiconductor potentials also influences the electric field.

Figure 3.23: Single-sided polarization measurement configuration using the Precision Premier II ferroelectric tester

Figure 3.24: Arbitrary discretized triangle waveform produced by the Precision Premier II ferroelectric tester
Figure 3.25: Polarization of the ND7 FeFET having the source grounded and drain disconnected with a 1 Hz gate voltage with 4 V amplitude

In the “singled-sided” configuration, or only having a single source or drain contact connected to ground, the modeled and empirical voltage dependent polarization data for each of the three transistor types are shown in Figure 3.26, Figure 3.27, and Figure 3.28 for the ND1, ND4, and ND7 transistors respectively. Visual comparison of the modeled data shows good agreement with the experimental data in general. In each of the experimental datasets, the FeFET gate voltage varies between ±4 V using the discretized triangle waveform discussed previously. Abrupt transitions in the input waveform can lead to disagreement between the modeled and experimental polarization curves as the triangle wave first derivative is discontinuous. Aspects of the polarization on which particular emphasis is placed are the restriction of the source contact area due to the encroaching depletion layer and polarization saturation, which is the true indicator of ferroelectric behavior. Both of these aspects are observed in the modeled polarization curves as well as the empirical data.
Figure 3.26: Comparison of the modeled and empirical polarization of the ND1 transistor collected using a 2 Hz triangle wave input signal

Figure 3.27: Comparison of the modeled and empirical polarization of the ND4 transistor collected using a 2 Hz triangle wave input signal
Figure 3.28: Comparison of the modeled and empirical polarization of the ND7 transistor collected using a 2 Hz triangle wave input signal

Though visual inspection of the modeled polarization curve shows poor agreement in general with any of the FeFETs, this is not necessarily unexpected. Since the modeled polarization was essentially a steady-state condition at each measurement point, the polarization is expected to be larger than that of the empirical data. Despite using a fairly benign frequency such as 2 Hz, the differences between the modeled assumptions and the empirical data are significant.

(ii) Drain Current Hysteresis

Quite possibly the single most iconic measurement of a ferroelectric transistor is the drain current hysteresis arising from the gate voltage dependence of the current. This was shown previously to a degree with the switching polarization measurement. However, whereas polarization measurements are concerned with the charge exiting or entering the source or drain of the transistor, the current measurements deal with the rate at which the charge exits or enters the source or drain, which is a small distinction.
Within the drain current hysteresis measurement again two families of measurements exist that are equally important: the active and remnant currents. Active current is defined as the drain current observed while having a gate voltage applied that is non-zero gate or has a non-zero derivative with respect to time, i.e., the gate voltage is simply passing through 0 V rather than remaining at that voltage. Conversely, the remnant current is defined as the drain current observed when the gate voltage is set to 0 V and has no appreciable change with respect to time. In the remnant current configuration, the current is defined solely by the polarization state, and the FeFET is allowed to operate as either an enhancement mode or depletion mode transistor.

Examining the active current of the FeFET, a setup similar to that shown in Figure 3.23 is used but with the drain connection established to a positive voltage. Within this setup, two current measurements highlighting the FeFET current dependence on terminal voltages are considered. First, the FeFET drain-to-source current, $i_{DS}$, dependence on the gate voltage, $v_{GS}$, is evaluated. The typical MOSFET voltage notation is used here, relating the gate voltage to the source. Of note, however, is that the source is grounded at the “Return” terminal of the ferroelectric tester and so $v_{GS}$ is interchangeable with $v_G$. Prior to measuring the drain current, the gate terminal is poled, which is to say a voltage sufficiently large so as to polarize the ferroelectric layer is applied to the FeFET gate while the source and drain are grounded. This poling establishes the tests’ initial conditions to remove the virgin or initial current hysteresis curve, which is of no value without having a knowledge of the polarization state.

The resulting empirical current curve shows not only a dependence on the gate voltage but also on the polarization state. As the gate voltage increases, so does the
current after reaching the threshold voltage. Initially the current increases rapidly with respect to the gate voltage, similar to the saturation region of the MOSFET whereby the current increases proportional to the modified gate voltage (gate voltage less the threshold voltage). The drain current then saturates, increasing to a much lesser degree with increasing gate voltage; this region is similar to the linear or triode region of the MOSFET. To demonstrate the agreement of the modeled with empirical data, the current versus gate voltage hysteresis is shown for each FeFET size in Figure 3.29, Figure 3.30, and Figure 3.31. On each current hysteresis, the threshold voltage is indicated to demonstrate the agreement between modeled and empirically measured data. The threshold voltages are collected in Table 3.6 to illustrate the modeled and empirical values more precisely.

![Diagram](image)

Figure 3.29: Current hysteresis arising from gate voltage dependence for the ND1 for both modeled and measured currents
Figure 3.30: Current hysteresis arising from gate voltage dependence for the ND4 for both modeled and measured currents

Figure 3.31: Current hysteresis arising from gate voltage dependence for the ND7 for both modeled and measured currents

Table 3.6: Approximate FeFET threshold voltage from both empirical and modeled data
<table>
<thead>
<tr>
<th>FeFET Model</th>
<th>Threshold Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Negative Polarization</td>
</tr>
<tr>
<td>ND1</td>
<td>-1.0</td>
</tr>
<tr>
<td>ND4</td>
<td>-2.0</td>
</tr>
<tr>
<td>ND7</td>
<td>-1.5</td>
</tr>
<tr>
<td>Model</td>
<td>-1.0</td>
</tr>
</tbody>
</table>

Though general agreement is observed between the modeled and measured drain current for each FeFET, the preferred approach to assess the accuracy of the model polarization is found by way of the percent error. The error is defined as the deviation from the empirical, or truth, data as indicated by Equation (3.41).

\[
\text{Percent Error} = \frac{P_{\text{Model}} - P_{\text{Experimental}}}{P_{\text{Experimental}}} \cdot 100\% \quad (3.41)
\]

Similarly, the mean percent error is given by taking the mean of the percent error evaluated at each data point across an entire period of the input waveform. A voltage dependent percent error plot of the modeled drain current is shown for each of the ND1, ND4, and ND7 FeFETs in Figure 3.32, Figure 3.33, and Figure 3.34, respectively. Overall, the FeFET polarization model is within family of the experimental results, with large divergences for small currents that manifest as large percent error or for slight shifting owing to differences in polarization.
Figure 3.32: Percent error of the FeFET model drain current hysteresis measured against the ND1 FeFET with gate voltages ranging from -4 to 4 V

Figure 3.33: Percent error of the FeFET model drain current hysteresis measured against the ND4 FeFET with gate voltages ranging from -4 to 4 V
Figure 3.34: Percent error of the FeFET model drain current hysteresis measured against the ND7 FeFET with gate voltages ranging from -4 to 4 V

(iii) Gate Capacitance

The primary method of measuring capacitance of the FeFET, specifically the gate capacitance, consists of taking the numerical derivative of the charge collected during a polarization measurement with respect to the applied gate voltage. This method seeks to approximate the derivative of charge with respect to voltage by measuring a small change in charge during the time period where the gate voltage is held constant at the new voltage step. The actual voltage waveform is precisely the same as that shown in Figure 3.24 where non-varying portions of the gate voltage indicate the measurement periods. To this end, the capacitance is then estimated at each measurement point using the definition of the capacitance as shown in Equation (3.42).

$$C = \frac{\partial Q}{\partial V} \approx \frac{\Delta Q}{\Delta V} \quad (3.42)$$
In this arrangement the only non-zero voltage is the gate voltage, resulting in measurement of the gate-to-source capacitance, $c_{GS}$, by changing the gate-to-source voltage, $v_{GS}$. Measurement of the gate-to-drain capacitance, $c_{GD}$, is unnecessary since the transistor channel is symmetric and results in the same measurement if configured similarly. However, the voltage ranges across the gate-to-source and gate-to-drain terminals may be different depending on the circuit and application. In this case both $c_{GD}$ and $c_{GS}$ are governed by the same curves arising from the same phenomenon but operate in different regions of the capacitance hysteresis.

Owing to the modeling assumptions, different input waveforms, and granularity of the polarization-based measurements, agreement to the extent expected is observed between the three datasets for each of the three FeFET sizes, specifically increasing gate voltage for both ND1 and ND7 transistors. As seen previously, the discrepancies in polarization again manifest in the capacitance, though lessened as the modeled polarization derivative tends to be closer to the experimental data than the polarization itself. However, if the polarization is in agreement – to include the derivative of the curve – then the capacitance should also agree between modeled and empirical data. Capacitance of the FeFET model as compared to the empirical data for each FeFET is shown in Figure 3.35, Figure 3.36, and Figure 3.37.
Figure 3.35: Capacitance of the ND1 FeFET computed using empirical measurements (collected using a 2 Hz signal) and FeFET model having gate contact area of 100 $\mu$m$^2$

Figure 3.36: Capacitance of the ND4 FeFET computed using empirical measurements (collected using a 2 Hz signal) and FeFET model having gate contact area of 1600 $\mu$m$^2$
Figure 3.37: Capacitance of the ND7 FeFET computed using empirical measurements (collected using a 2 Hz signal) and FeFET model having gate contact area of 1600 μm$^2$

Quite possibly the most important aspect of the gate capacitance that represents a major departure from typical ceramic capacitors is the voltage dependence of the capacitance. While capacitance is represented as a single value for linear capacitors since the change in charge is linearly related to the applied voltage up to dielectric breakdown, for the FeFET and ferroelectric capacitors in general the capacitance is a non-linear function. As a result, great care must be used when designing a circuit using ferroelectrics, lest the circuit operate in unexpected modes as a result of a varying polarization state. Two principal methods exist to bypass or address the issue easily: operating in a small voltage range or periodic setting of the polarization state. As power supplies, especially in low-power electronics, are often small enough to operate in a region that does not perturb the polarization state significantly, applying only small voltages is a viable option. The intersection of the two ideas is also of interest wherein the small applied voltages do not disturb the polarization state, but larger voltages can be
applied to set the polarization and thereby the capacitance of the device. In this manner ferroelectric capacitors or transistors can be used as a variable capacitor similar to that of a varactor for MOS devices.

(iv) Remnant Polarization and Current

In order to measure the retention over time, the transistor gate has either a negative or positive voltage applied. Initially, the applied voltage is large in order to set the polarization state for the test. As with the active drain current measurements, the polarization state must be known, again making the virgin or initial remnant currents not useful. Additionally, the voltage is applied for sufficiently long so as to polarize or write to the polarization completely. For the remnant measurement, the gate voltage is removed, replacing it with ground, as shown in Figure 2.16 having the switch open. The gate voltage is adjusted prior to closing the switch, helping to alleviate additional effects that would adversely affect the polarization. After the write time elapses, the switch moves to the open position allowing measurement of the remnant current. The drain voltage, set by the external supply, actually serves to destroy the polarization set by positive states and not allow the full extent of the voltage to be felt by the ferroelectric layer at the drain end. For this reason, the drain voltage is set to a small value in order to minimize the detrimental effects.

With the polarization in the PZT layer arranging to oppose the applied electric field in the active configuration (switch closed), in the remnant measurement configuration (switch open) the polarization serves to incite a current similar to the active current observed using the negative of the writing gate voltage. Interestingly, this causes the remnant current for a given voltage $v_{GS}$ to be proportional to the active current
observed using \(-v_{GS}\), or equivalently \(v_{SG}\). The reversal of the voltage polarity under remnant conditions is similar to switching between an NMOS and p-channel metal-oxide-semiconductor (PMOS) transistor. This unique feature can result in very interesting characteristics, limited primarily by the decay rate of the polarization and the need to set the polarization for each “remnant gate voltage” evaluated. However, in digital applications this may become useful as the voltages are constant during much of the circuit operation and the polarization may be set or written to during the transitions.

Due to the extended run time of the model per time step in addition to the small time steps required for the model execution, a limited current sample over a very brief time period is provided in Figure 3.38. Accuracy of the polarization retention of the FeFET model is unable to be verified against the empirical data owing to the severe differences in the time scales of interest. However, the potential barriers defined by the short-range potential terms can be scaled up or down via the energy depth term, \(\epsilon\), as shown in Equation (3.6).

![Graph showing remnant polarization of the FeFET model](image-url)

Figure 3.38: Remnant polarization of the FeFET model
In the remnant model simulations, a time step of 1 femtosecond is used to increase the accuracy of the results. Examining the polarization over time, however, severe swings in polarization occur in the first 20 fs of the simulation, initially dropping further as the ferroelectric crystal attempts to reach steady-state conditions after being poled with -5 V and abruptly reducing the electric field to 0 V/m after \( t = 0 \) s. The polarization then increases, decreasing in magnitude, until settling at approximately -40 \( \mu \text{C/cm}^2 \) for the duration. Small perturbations occur in the polarization extending until simulation stop. However, the rapid nature of the changes initially indicates the potential barriers may be insufficient to capture and retain ions in the polarized state for sufficient time or the spatial and time scales of interest are not adequately represented by the grids chosen. Taking a slightly different view of the retention, as is the typical viewpoint for retention testing and circuit design, the retention current is shown in Figure 3.39. Of note is that the remnant polarization effects on the drain current for the measured data is on the same order as the active current. This shows the charge of the polarization being smaller still creates an appreciable electric field in the semiconductor owing to the proximity of the charge and thin semiconductor layer (only 20 nm).

![Figure 3.39: Modeled remnant drain current of the FeFET over limited time scale](image)

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D. Model Timing Analysis

Simulated times are restricted greatly due to the efficiency of the model along with the number of computations required. Of particular interest is simply the time required to advance the model by a single time step, which is actually independent of the chosen time step size (17.65 s on average for the simulation settings used in this work). The principal driver in run time here is the computation of the potential terms for each ion core and shell. Because the potential is a function of time, changing with both the applied electric field (generally assumed to be time varying) and ion positions, the potential much be calculated for each grid point at each time step for each ion component. This results in calculating the potential at 3,375 points (15^3 grid points) for each of the ions lying within the domain of interest. For the example of the 2\times2\times2 unit cell block used here, 8 central ions are contained. However, there exists 27 lead ions and worse still 36 oxygen ions. With a nearest neighbor distance of 1.65\times the lattice constant, the result is that ion will calculate the potential contribution from each neighbor at each grid point, with the number of ions as described in Table 3.7. One further approximation may be to only update part of the potential on a given time step. Reasoning for this would be, depending on the time step chosen, the electric field often does not vary considerably on a femtosecond scale (depending on the frequency of interest). Similarly, the ion cores being much more massive than the electron shells, displace at a much slower rate. A simplification could then be chosen to update potential terms based on neighboring electron shells only on some time steps, neighboring ion cores on some time steps, and finally the electric field potential on occasional time steps as well. The potential duration between computations would be determined by the frequency of the
applied electric field and the energy of the system overall, which dictates the ion movement.

Table 3.7: Nearest neighbor count by ion type, considering only ions within 1.65 lattice constants

<table>
<thead>
<tr>
<th>Ion Type</th>
<th>Number of Neighbors</th>
<th>Pb²⁺</th>
<th>O²⁻</th>
<th>Central</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb²⁺</td>
<td>18</td>
<td>60</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>O²⁻</td>
<td>20</td>
<td>58</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Central (Zr⁴⁺ or Ti⁴⁺)</td>
<td>8</td>
<td>60</td>
<td>18</td>
<td></td>
</tr>
</tbody>
</table>

Another factor contributing to the time required to run the model is the matrix size, which is especially prevalent during the initialization or steady-state condition computations. In this case, solving for the eigenvalues and eigenvectors of the system for a matrix of size, for the settings in this work, 3,375 × 3,375 is considerable and by far the largest time sink. This is exacerbated by the need to solve for the conditions iteratively where the expectation of the displacement is obtained and potentially going back to calculate a new displacement for each ion, as shown in the flow diagram of Figure 3.1. While this time is variable depending on conditions such as initialized ion displacements, the average time for a single data point is approximately 5000 s. For the initialization, a pie chart of the time spent in each portion of the code is provided in Figure 3.40.
E. Comparison to Other Models

Since the PZT FeFET model is at its core truly a ferroelectric model interacting with a semiconductor, comparisons may be drawn between the ferroelectric model employed in this work and those pertaining to ferroelectric capacitors as well as transistors. When comparing to other ferroelectric capacitor models, the overall behavior of the device may differ slightly resulting from the introduction of a semiconductor channel. For example, the idea of a terminal connection essentially “cutting off” when a significant, negative gate-to-terminal voltage is present differs from the often-used capacitor structure in literature and other models.

Comparing against work pertaining to the FeFET as a transistor is significantly more difficult. The unique structure of the FeFETs used in the body of this work result in trends departing significantly from those observed in literature, most prominently the current hysteresis direction. Despite the rarity of literature on the transistors of interest,
several models do exist, often showing good agreement with the experimental results though at the expense of additional empirically defined tuning factors.

(i) Ferroelectric Capacitor Models

One model developed for ferroelectric ultracapacitors showed very good agreement with a range of different ferroelectric material compositions. During the course of electrical characterization of the devices, of which there were 32, the important discovery of leakage current was made. While this has since spawned other research topics using these same devices, a simple polarization hysteresis was nearly unobtainable for all but high frequencies, generally 1 kHz or higher. As a result, the overall model of the devices incorporated series resistance measurements to aid in determining the response of each capacitor. First order modeling of the devices assumed a leakage resistance in parallel with a capacitance as shown in Figure 3.41, where the capacitance and resistance are both a function of the polarization state.

![Figure 3.41: Preliminary ferroelectric capacitance modeling approach](image)

Fortunately, the FeFETs of interest do not possess similar leakage, which would be tremendously disadvantageous for a transistor representing significant gate current. Interestingly, however, separation of the polarization charge and charge due to leakage current was able to yield promising results. Among the results is the fact that the
hysteresis was found to be much narrower. Since PZT, which is used in the FeFETs of this work, is noted to have large spontaneous electric polarization even among ferroelectrics, the idea that the hysteresis would be smaller in general is supported.

Another model created for the same set of ferroelectric ultracapacitors was again focused on assessing the leakage current out of necessity. In order to model the ferroelectric response of the samples, first the leakage current or resistive part of the device response was first removed, allowing modeling to differentiate between the charge arising from ferroelectric polarization and that arising from leakage current. The first-order approximation of the device has proved to represent the device characteristics well, which has removed what was once thought to be negative capacitance from the experimental data.

For the ferroelectric ultracapacitors in particular, the significant, and at times overwhelming, leakage current results in a negative change in charge given a change in voltage, $\frac{\Delta Q}{\Delta V}$, which occurs as the change in charge is directly tied to both a the parallel resistance and the parallel capacitance. Often observed at lower frequencies, the charge, $\Delta Q$, may be positive even as the voltage is reduced. This issue presents itself from the fact that the resistance continues conducting and continues delivering a net positive charge delta to the measurement device even when the capacitive response trends similarly to that of purely dielectric capacitors.

Another important finding of earlier work with ferroelectric capacitors was the severe humidity dependence of the devices. By measuring the polarization hysteresis at varying relative humidity (RH), differences in the response of the ferroelectric capacitors as a function of humidity were observed. The humidity tended to increase the leakage
current through the capacitors, lowering the effective resistance. In fact, for some compositions the current was made so large that the Precision Premier II tester from Radiant Technologies, Inc. was unable to measure the magnitude of charge. This has actually led to use of these particular ultracapacitor samples as humidity sensors as the change in device properties is so great given a small change in humidity.

As with the leakage measurements, the FeFETs of interest do not exhibit a humidity dependence and as such this is not included in the model. Whereas the ferroelectric ultracapacitors evaluated in earlier research were exposed to ambient humidity, the FeFETs packaged by Radiant Technologies, Inc. are essentially sealed from external humidity owing to the casing of each individual transistor. Similar to the integrated sensors outlined in chapter IV, an exposed or partially exposed FeFET gate may be able to find use as a humidity sensor as well.

Both of the ferroelectric capacitor models discussed here had very strong agreement with experimental results, however that is expected as both are empirically derived models. One of the benefits of a physically derived model, such as the one presented here, is that given information on the material of interest, device performance may be assessed prior to fabrication. Therefore, while the agreement between modeled and experimental data may be less so than seen with the capacitor models of earlier work, the great advantage lies in the ability to characterize any ferroelectric material and simply allow the physics of the device to dictate the performance.

(ii) Ferroelectric Transistor Models

Along the lines of earlier work, one of the few FeFET models constructed for the particular FeFETs used here was heavily empirically derived, similar to the earlier
capacitor models. Among the advantages of the empirically derived model was great agreement with experimental results, quick runtime, and a variety of tuning parameters to allow agreement to a range of materials of interest. However, with this versatility and pseudo-accuracy came the drastic need for referent data. The model was unable to anticipate device performance outside of what was already observed, essentially being trained to a particular set of data. That said, the model was capable of success in evaluations of several analog circuits [38, 46, 49].

Whereas the current model is able to assess new materials, or even structures, without the need for updated referent data, perhaps its most significant departure is in the consideration of retention characteristics. Ferroelectric polarization over time is by far the most used application of ferroelectric materials, allowing non-volatile retention for memory applications. However, memory is not the only application that benefits from the polarization time history. As elaborated on in chapter IV, the polarization characteristics can actually benefit several analog or radio-frequency circuits, and the retention characteristics make for a much more complex and perhaps rewarding use for the transistors.

The only earlier physically derived model of the particular FeFETs of interest examined the incorporation of PZT into the transistor. This resulted in a non-quasi static model of the transistor that has enjoyed agreement with empirical results [40, 41, 53]. A similarity between the earlier model and the one presented in this work is the partitioned ferroelectric layer which allows for varying polarization or ferroelectric potential across the channel. This allows destructive drain or even source voltages to play a role in the current-voltage relationship over time. As the earlier model was concerned with analog
circuit operation, namely common-drain, common-gate, and common-source amplifiers, the time evolution of the polarization after voltages are turned off or removed is the principal difference between the two models.

F. Conclusion

The FeFET model is developed using the transistor geometry and materials in agreement with the device manufacturer specifications. The principal purpose of the model lies in the PZT ferroelectric model, which dictates the polarization state having an overarching influence on transistor behavior. In general, the progression of the model is shown to start at the ion level, incorporating the shell model to determine ionic displacements that lead to the polarization of the PZT unit cells and extend to the layer as a whole. Estimation of the wave function for each ion results in the ability to propagate the solution forward in time, thereby capturing the time evolution of the system. Notably, this model leads to calculation of the polarization retention.

Semiconductor modeling begins using the thin film transistor structure of the indium oxide channel. Interactions between the semiconductor and ferroelectric layers determine the transistor current, which is the most notable aspect of the FeFET in general. Additionally, the capacitance of the transistor is found arising from the polarization model and impacts on semiconductor contacts.

Agreement with empirical data is also shown, ranging from ferroelectric polarization to FeFET drain current in various conditions and ultimately culminating in polarization retention. Model performance in each area is benchmarked to the empirical data to determine accuracy and provide confidence in the model for various applications. The primary area of model usage will likely be retention testing as empirical
measurements, especially using different transistor sizes and measurement conditions, can be exceedingly cumbersome.
CHAPTER IV

FEFET APPLICATIONS

Unique properties of the FeFET make it an attractive addition to several circuits, opening the door to new operation or different methods of achieving similar operation. To date, the primary area of focus for ferroelectrics in general is memory applications, taking advantage of the non-volatile operation. By writing to the polarization of the ferroelectric layer, data are stored for long periods even in the event of power disruption. Use of the polarization as a non-volatile storage element is not the only application of ferroelectric materials, however. Another principal area where ferroelectric devices are used is in radiated environments. Due to the inherent radiation hardening of the FeFETs owing to the addition of the PZT layer at the gate, space applications such as satellites can benefit from these ferroelectric devices [58, 59].

However, non-volatile operation is beneficial not only for memory applications but also for device tuning in analog or RF circuits. Non-volatile polarization of PZT allows for device tuning such as to alter FeFET threshold voltage or gate capacitance. Interestingly device tuning based on polarization state can then reveal various modes of operation depending on the applied poling voltage. It is this varying mode of operation that is employed for both digital and RF circuits, exemplified by the 1-Transistor, 1-Capacitor (1T1C) DRAM and ring oscillator circuits, respectively.
A. 1Transistor-1Capacitor Dynamic Random-Access Memory

Currently, the widest application of ferroelectric devices exists in the field of digital circuits, and more specifically memory circuits. Due to the non-volatile properties of ferroelectric layer polarization, ferroelectric devices have the unique ability to store a state in the device polarization quickly while also withstanding many write cycles. In fact, the devices from Radiant Technologies, Inc. are suggested not to imprint or have fatigue. Resulting from the non-volatile storage capability, ferroelectric capacitors see use in long-term memory storage applications. However, devices incorporating a ferroelectric layer in a transistor are rarely incorporated in memory circuits. In this section, examination of the 1T1C memory cell using the FeFET shows great potential for use in several applications, giving either new modes of operation or enhanced capability.

Although present non-volatile storage research using ferroelectric devices primarily looks at ferroelectric capacitors, non-volatile storage afforded by the FeFET has not been the focus of extensive research to date. In 1974, the idea of incorporating ferroelectric material in a transistor for memory storage was first introduced. Using the new device, a DRAM design that utilized a ferroelectric gate transistor was proposed by several researchers [143, 145, 146, 147]. New capacitor-less DRAM designs were then able to harness the polarization of the transistor as a storage mechanism resulting from the new device. While a ferroelectric gate transistor would be more challenging to fabricate, resulting from the different processing required opposed to typical silicon on insulator (SOI) devices, the capacitor-less design transformed the MOSFET 1T1C memory cell shown in Figure 4.1 into a single transistor. Of widely used memory designs, the memory cell with the smallest footprint today is the 1T1C DRAM cell and is
typically seen as one of the simplest designs available. As a result, the ability to reduce the number of devices to half when using a FeFET is especially attractive.

![Diagram of 1T1C circuit](image)

Figure 4.1: 1T1C circuit diagram

Using the FeFETs provided by Radiant Technologies, tests using a 1T1C memory cell design shows non-volatile retention of the stored value as anticipated with these ferroelectric gate transistors [42, 43]. Furthermore, with precisely the same 1T1C design a memory cell that stores two data bits is possible. By retaining the capacitor previously removed in the capacitor-less approach (instead having a layout the same as Figure 4.1), storage in the capacitor combined with non-volatile storage in the polarization results in two independent bits. However, this new mode of operation is not required to be used; that is to say, the MOSFET-like 1T1C operation is valid even when using the FeFET.

(i) 1T1C DRAM MOSFET Operation

In the classical or MOSFET operation of the 1T1C circuit remains even after the FeFET, though additional capabilities now reside in the circuit. The overview of operation consists of setting the “bitline” to the appropriate value to be stored as the voltage across the storage capacitor, $C_{\text{Store}}$. The “wordline” is then set to “high” value, allowing the transistor to conduct as the switch is closed. The capacitor $C_{\text{Store}}$ then charges or discharges until either the switch opens, “wordline” transitions to “low,” or the
capacitor is unable to charge or discharge any further. Opening the switch or setting “wordline” to “low” stops the write process, as dictated by the timing of the circuit. In the absence of halting the writing process early, the voltage stored on the capacitor is the lesser of the “bitline” voltage and the “wordline” voltage, less the transistor threshold voltage.

Reading the stored value occurs via the sense capacitor, wherein the “bitline” node is charged to a preset voltage, typically half of the supply voltage, $V_{dd}$, and the switch closed with the “wordline” set to a “high” voltage. Deviations in the voltage of the sense capacitor, either increasing or decreasing, resulting from the connection to the storage capacitor reveal the stored value. In this process, the act of reading the stored voltage on the capacitance destroys the stored information, which results from altering the voltage across the capacitor significantly as a result of making an electrical connection with the sense capacitor.

Since the storage mechanism in this design involves maintaining a voltage across a capacitor, the single largest drawback of the 1T1C design is capacitor discharge over time. Discharge arises as a result of parasitic resistances, causing any stored charge to slowly leak, which eventually leads to data loss. To compensate for the capacitor discharge, DRAM designs adopt a refresh cycle approach wherein the stored value is read and again written to the memory cell. The refresh cycle repeats indefinitely with a period defined by the memory device fabrication, resulting from an estimation of the discharge times in order to ensure data integrity. However, resulting from the small size and simplicity of the design, refresh cycles occur tens to thousands of times per second. It is
this constant need to refresh the stored data that results in non-volatile storage mechanisms appearing especially attractive if power or long-term storage are of concern.

The MOSFET 1T1C topology is characterized by the ability to write to the storage capacitor, maintain the capacitor voltage above a threshold for a specified amount of time, at which point a refresh cycle must occur, and read the bit from the memory cell via the access transistor. Empirical data of the FeFET 1T1C circuit demonstrates the MOSFET operation by positively polarizing the transistor and using voltages small enough not to influence the polarization state of the device. This operation mode arises from the FeFET performing similarly to an enhancement mode transistor in the positively poled state.

To maintain MOSFET-like operation of the memory cell, the FeFET must remain in a non-negatively poled state, which is to say it must not operate as a depletion mode transistor. If, for example, the gate voltage by comparison to the source or drain of the transistor is negative, then the ferroelectric gate performs as though it is negatively poled, albeit often only slightly. This imposes restrictions of the voltages stored on the capacitor since the ferroelectric gate voltage is grounded during the retention period. Acting as a depletion mode transistor does not invalidate the MOSFET-like operation of the FeFET memory cell, however. Instead, the depletion mode operation is essentially increasing the leakage current or parasitic resistances observed by the capacitor. This in turn quickens the discharge rate of the capacitor necessitating a more frequency refresh cycle. Between the extremes of operating similar to either a depletion mode (negatively poled) or enhancement mode (positively poled) transistor, a modified threshold voltage operation exists. This has the effect of increasing the leakage current similar to the
depletion mode operation, but the refresh cycle time is now dictated to the extent that the gate is negatively poled. Therefore, when designing and timing a 1T1C DRAM cell using a FeFET, the refresh time must account for the components used in addition to the supply voltage effects on the leakage current of the FeFET.

Empirical data measuring the FeFET 1T1C operation shows correct MOSFET-like operation of the circuit. Using the FeFET, the storage capacitor retains the written voltage until either the read cycle senses the charge residing on the capacitor or the charge dissipates through the parasitic resistances in the circuit. Here, the leakage current through the FeFET is considered a parasitic resistance in the context of unwanted current through otherwise unavailable paths. As shown in Figure 4.2 for storing a high voltage, the FeFET allows current to flow to the storage capacitor during the write operation, thereby applying the necessary voltage across the storage device. The storage capacitor voltage decays for a period of time during the retaining or storing portion of the circuit operation, which is worse in the empirical data compared to a practical circuit owing to the additional instrumentation added to the circuit for reading node voltages – including a probe directly on the storage element. Finally, during the read operation the voltage at the capacitor dissipates quickly as the FeFET connects the bitline to the storage capacitor. Variation in the sense voltage indicate the stored value to be a “high” voltage, or logical “1”. As shown with the storage capacitor voltage, the sense voltage too is worsened by the added instrumentation relative to what would be observed practically.
Figure 4.2: Four possible read cycle results of the two-bit 1T1C DRAM cell using the ND1 FeFET and a 5 V supply voltage. The first two configurations have a “low” value previously written to the storage capacitor, and the last two outputs have a “high” value previously written to the storage capacitor. The first and third configurations use a negative poling voltage whereas the second and fourth configurations use a positive poling voltage, which allows the FeFET 1T1C MOSFET-like operation with data bit storage in the storage capacitor voltage.

The case of storing a “low” value, which results in simply discharging the storage capacitor to the extent possible during the write cycle, is not as exciting as storing a “high” value since retention time is infinite for this scenario. However, the varying polarization state of the FeFET leads to the interesting feature of varying threshold voltages under different conditions. Notable, the transistor drain will be at the read voltage, typically half of the power supply voltage, during the read operation. The transistor source on the other hand is either 0 V (storing a “low” value) or the decayed state of the once “high” voltage. Therefore, the gate voltage at which the transistor conducts changes with the voltages of the circuit, as expected with the MOSFET.
However, the current and previous storage capacitor voltages also affect the polarization state of the transistor, which varies the voltage at which the FeFET begins conducting. In general, this has limited impact on the operation of the circuit unless the supply voltage is small enough to the point of not turning on the FeFET.

(ii) 1T1C DRAM Non-Volatile Operation

The DRAM memory cell already protects against short power supply interruptions since the voltage across the storage capacitor is unaffected by power supply interruptions short enough to not miss a refresh cycle. However, in the event of a prolonged power loss the stored information is lost completely, that is unless the bit is also stored in the polarization of the FeFET as a safeguard or redundancy mechanism. Due to the radiation-hardened nature of the FeFET and gate polarization, the redundancy mode of operation may be especially useful for space applications or other uses in radiation-rich environments. The need for redundancy mechanisms within the circuit vary between applications, but the idea of a truly non-volatile storage mechanism can benefit many other more general applications by writing to the polarization state of the FeFET.

During operation solely utilizing the polarization of the FeFET for non-volatile storage, both write and read operations utilize the bitline. Interestingly, the FeFET 1T1C memory cell benefits from writing a low value to the storage capacitor in order to more strongly polarize the ferroelectric layer as outlined in Figure 4.3. The different write operation stems from a desire to polarize the ferroelectric material more or less completely at the expense of longer, more complex or shorter, simpler write cycles, respectively. If, for example, the ferroelectric gate is to be positively poled, the largest
voltage able to be applied across the ferroelectric material results from having both the storage capacitor voltage, $V_x$, and the bitline grounded while the wordline is equal to the maximum available voltage, often the supply voltage. Initially the discharging of the storage capacitor may be viewed as an additional process required for the polarization write cycle. However, the capacitor discharge can occur naturally as a result of turning on the FeFET with the bitline grounded. The extent to which the capacitor is discharged depends on the polarization state, voltages, and write cycle duration. Longer write cycles or larger supply voltages work to minimize $V_x$, which is beneficial as small, residual voltages on the storage capacitor lessen the extent of the polarization. Additionally, the residual voltage works to destroy the polarization over time, albeit typically very minimally. The second potential write cycle stems from the desire to maximize the polarization extent, typically within the context of shorter write cycles or smaller supply voltages. The wordline first transitions to a minimum while the bitline is at the maximum voltage, thereby negatively poling the FeFET gate. While this is the opposite of the desired polarization state, the FeFET has a minimized threshold voltage that allows quicker discharge of the storage capacitor at lower voltages. The bitline and wordline then reverse to mimic the first write cycle, in effect creating a pre-write cycle that can be applied depending on the configuration of the memory cell.
On the other hand, if applying a negative poling voltage to write a “low” value, then a negative gate-to-source or gate-to-drain voltage is needed in order to polarize the transistor gate. In the event of not using a negative supply voltage, the necessary gate voltage arises from raising the bitline voltage while minimizing the wordline. In this instance, three different write cycles exist depending on the time and complexity allowed, which is often dictated by the supply voltages available. The simplest write cycle consists simply of maximizing the bitline (raising it to the supply voltage) while minimizing the wordline. Similar to the positive poling pre-write cycle, to further polarize the FeFET the storage capacitor can be charged prior to initiating the polarization write thereby establishing the greatest magnitude, negative gate-to-source voltage possible. Charging the storage capacitor prior to the polarization write cycle in effect creates the first potential pre-write cycle. However, the storage capacitor voltage is restricted by the threshold voltage of the FeFET, charging only to the bitline voltage less
the FeFET threshold voltage at best. To further help set the polarization, a second pre-write cycle can be used to first initiate a negatively poled state, thereby minimizing the threshold voltage of the FeFET. By minimizing the FeFET threshold voltage, the storage capacitor charges to a maximum, which will then produce the largest magnitude gate-to-source voltage possible and serve to write to the polarization to the extent allowable. The write cycle alongside the possible pre-write cycle shown in Figure 4.4 create the desired voltages to polarize the FeFET gate, assuming sufficiently large supply voltages.

![Figure 4.4: Method for writing a negative value to the FeFET polarization for non-volatile operation with pre-write cycle and the base write cycle](image)

With the polarization set to the desired state, the read operation is similar to that used for the MOSFET operation with the caveat that the storage capacitor voltage – and therefore the source voltage of the FeFET – is unknown along with the polarization state. If the time since writing to the FeFET is sufficiently long, then the voltage at the FeFET source, $V_x$, is minimal due to the parasitic resistances discharging any voltage that would otherwise be present on the storage capacitor. In this instance, the polarization state
modifies the allowed current according to the current hysteresis as shown in Figure 2.15 for the ND1, ND4, and ND7 transistors. Polarization retention determines the proximity of the current to either the positively or negatively poled curves. In general, the polarization is taken to modify the threshold voltage and therefore the magnitude of the current can be used to determine whether the FeFET is operating in the positively poled (smaller current) or negatively poled (larger current) mode. Therefore, with the sense capacitor connected to the charged bitline, the rate of discharge of the sense capacitor reveals the polarization state. That is, given a known drain and gate voltage for the FeFET and assumed grounded source, the polarization state is the only remaining term governing the current through the transistor. During the read cycle, the gate voltage increases slightly to the point of conducting for a negatively poled state and minimally conducting if in the positively poled state. The magnitude of the read cycle gate voltage remains below a voltage that would otherwise severely disrupt the polarization. Similarly, the bitline pre-charge is restricted to non-immediately destructive voltages. If the gate voltage migrates too high during a read operation, the voltage across the source-side of the ferroelectric layer becomes sufficiently large so as to polarize the material, at least partially, which may lead to ambiguous or incorrect read results. This is shown in Figure 4.2 for the case of $V_2$ storing a “low” value (assumed grounded as with non-volatile operation).

However, in the general case the storage capacitor voltage is unknown, especially if writing to the polarization in such a way that the capacitor charges during the pre-write cycles. To alleviate this concern and construct a generalized read cycle, two methods of reading the polarization are formed. In the first method, the source voltage is bled off
with the gate voltage increased slightly and the bitline grounded. The extent to which this portion of the cycle occurs depends on the gate voltage used, which controls the drain current. For the worst case of a positively poled FeFET gate (measured in terms of the drain current), lowering the drain voltage to ground requires the gate voltage be set to the positively poled threshold voltage in order to establish significant conduction between the source and drain. As the source voltage lowers during the discharge portion of the read cycle, the drain current reduces over time owing to the decreasing drain-to-source voltage. The source voltage need only decrease to the point of being unambiguous as compared to the threshold voltage in either the positively or negatively polarized state, which is dependent on the FeFET physical characteristics – namely to include the ferroelectric material – in addition to the resolution or accuracy of the sense circuitry. With the source voltage reduced to an acceptable level, the gate voltage (wordline) then transitions low to allow the bitline charging of the sense capacitor. At this point, the gate voltage again increases to the nominal read level while the read cycle executes precisely as it would for the case with the source voltage assumed to negligible. This in turn establishes a pre-read cycle, as shown in Figure 4.5, similar to the possible pre-write cycles available for this non-volatile storage configuration.
Figure 4.5: Non-volatile 1T1C read cycle with source voltage discharge pre-read cycle execution

Ferroelectric transistors are used in some 1T memory cell circuits that simplify the design by removing the capacitor [143, 146, 148]. Without the addition of the capacitor, the circuit is left to only using the non-volatile and radiation hardened polarization storage mechanism, though benefiting from the simplified read cycle as well. A disadvantage of this is found when considering the extent to which the polarization can be set as the source connection of the transistor is always grounded without the possibility of further widening the gate-to-source voltage disparity through a pre-write cycle. Additionally, use of the 1T1C DRAM cell solely for non-volatile storage can be especially useful for applications calling for radiation hardened memory. This storage method, which initially seems more involved, benefits from the radiation hardened nature of the ferroelectric layer polarization. By using the same memory cell for applications in not only radiation rich environments but also radiation scarce environments, the overall
design gains widespread appeal where strengths of the circuit can appeal to specific aspects of each application.

(iii) 1T1C DRAM Two-Bit Operation

While the 1T1C memory cell represents one of the smallest and simplest memory devices available, using a FeFET as the transistor allows two bits to be stored in each cell, doubling the amount of memory storage possible in a specific circuit. The unique storage mechanism of the FeFET combined with the transistor operation allows writing of one bit to the polarization while also maintaining the classically stored bit in the voltage of the storage capacitor. The read operation is more complex as a result, simultaneously requiring determination of the voltage and the channel resistance or slope of the bitline voltage when reading. Similarly, the write operation is slightly more protracted as the cycle completes writing to both the storage capacitor voltage and the FeFET polarization state.

The write cycle for two-bit operation actually mimics that of the non-volatile operation combined with the MOSFET-like operation. First, the optional pre-write pulse may be executed, again according to the timing constraints of the circuit. This is shown in Figure 4.6 labeled as a “pre-pulse” cycle. During this portion of the write cycle, the gate voltage transitions to a minimum, here allowed to extend to -5 V approximately to establish a negatively poled gate. Where earlier the source and drain of the FeFET were shown to be at a maximum to better influence the polarization state, here they remain essentially grounded. The reason for this being that the gate-to-terminal voltage is still bounded by the limits of the FeFET devices; if a negative supply is used, effectively having twice the supply voltage applied across the ferroelectric layer could cause gate
punch through. If instead a supply voltage of 3 V is used, then the source and drain voltages can be modified to exacerbate the effects of the gate voltage. The goal of the pre-pulse is, simply put, to negatively pole the FeFET gate in order to minimize the threshold voltage. In so doing, the storage capacitor is charged to the maximum allowed value, in the event of writing a high value to the capacitor, or discharged as quickly as possible, in the event of charge residing on the capacitor when writing a low.

Next, the write cycle applies the appropriate voltage to the storage capacitor, similar to the MOSFET-like operation write cycle. This portion of the waveform is familiar to the MOSFET write operation wherein the gate voltage on the transistor is raised and the drain voltage set to the desired capacitor voltage level (“high” or “low”). After the predetermined write time to the capacitor elapses, which is defined as a function of the voltage supplies, capacitance, and FeFET characteristics, the gate voltage transitions to the desired poling setting while maintaining the drain voltage as during the capacitor write phase. This portion differs from the single-bit non-volatile polarization write in that the drain voltage is held at the capacitor write value. In this storage method, the idea of positively poling the gate will act as a second “capacitor write” phase due to the high gate voltage required. As a result, if the drain voltage is altered corresponding to the poling voltage then potential for overwriting the previously defined capacitor voltage exists. Unfortunately, this inability to maximize the polarization extent can impact the storage ability of the FeFET depending on the voltage levels used. However, it is noteworthy that it is the difference in polarization states rather than the absolute polarization state that is measured during the read cycle. That is, if a chosen configuration is capable of polarizing the FeFET only partially in the positive direction
that will be considered when defining the polarization states for determination in the read cycle.

Figure 4.6: Two-bit operation of the 1T1C DRAM cell showing write cycles for both the FeFET polarization and storage capacitor voltage

Perhaps most interesting for this storage configuration is the read cycle. As with the MOSFET-like or the non-volatile storage configurations, the read cycle executes almost exactly the same, without the need of a pre-read cycle. Initially, the bitline along with the sense capacitor are set to a nominal voltage that will not disrupt the polarization state of the FeFET, often taken to be $V_{DD}/2$ as is typical in 1T1C DRAM cells. Next, the FeFET gate voltage increases to a nominal voltage that would slightly turn on the transistor, depending on the polarization state and source voltage. In the event of a “high” source voltage, the sense capacitor voltage should increase as current flows from the source to the drain in an attempt to equalize the voltages to the extent allowed by the transistor. Conversely, if the source voltage is “low”, then the sense capacitor voltage
instead decreases as current flows from the drain to the source. These sense capacitor voltage trends hold in general, with specific expected deviations in the voltage determined by the as-built circuit parameters. FeFET polarization is found by examining the rate at which the sense capacitor voltage changes. If the polarization is in a negatively poled state, then the sense capacitor voltage changes more quickly as compared to the positively poled state. This difference is of course due to the additional presence of carriers in the semiconductor in the negatively poled state as a result of the ferroelectric polarization as discussed in chapter II. From a device-level analysis, this manifests as a change in threshold voltage, which in turn alters the current through the transistor and allows more or less charge to move through the channel. Rather than requiring the actual slope of the voltage be measured during the read cycle, the end result of the read cycle can be examined. Knowing the length of time the read cycle is active along with the various characteristics of the potential output yields four distinct states, resulting from the four possibilities of two bits ($2^2$ states) as shown in Figure 4.2. In the first two output waveforms shown, a low value is written to the storage capacitor during the write cycle. This results in a decidedly lower drain voltage regardless of the polarization state. However, the first configuration, representing a “negative” poling voltage, has a decidedly lower drain voltage still. This greater separation between initial and final voltage results from the lowered threshold voltage of the FeFET combined with the small source voltage, both working to maximize drain current. In the last two output waveforms, corresponding to a “high” value written to the storage capacitor, only the negatively poled state actually achieves an appreciable deviation in sense capacitor voltage. This results from the final configuration of a “high” sense capacitor state and
positively poled gate essentially turning off the FeFET drain. In this configuration the threshold voltage is maximized in conjunction with the source voltage of the FeFET, thereby restricting the drain current maximally. The trend observed is that a positively poled gate results in the sense capacitor staying closer to the preset voltage whereas the negatively poled gate encourages the sense capacitor to transition closer to the storage capacitor voltage due to the increased current. Therefore, the final value of the sense capacitor dictates the storage capacitor value whereas the deviation from the pre-charge voltage reveals the polarization state. Each of the four potential states is easily determined by comparing to the expected value.

Though the additional write operation slows the operating frequency of the memory cell, due to the now doubled operations occurring during the reading and writing cycles, the speed of the device is still competitive at least for some applications. As with other designs, the operating frequency depends on the fabrication of all devices comprising the circuit, but the correlation with transistor dimensions here is especially important. A balance must be struck when sizing the FeFET as progressively wider and shorter channel dimensions increase current and thereby decrease the time required to write to the capacitor. However, shorter channels can also make the difference between the polarization states less significant and increase the destructive nature of applied drain-to-source voltages. Additionally, wider FeFET channels increase drain current to include the leakage current. As the leakage current increases, additional emphasis shifts to the on/off resistance ratio of the channel. Therefore, the write and read cycles may occur more quickly than they would otherwise but must occur more frequently as a result.
B. Ring Oscillator

Oscillators are among the most important RF circuits. As a result, application of the FeFET to an oscillator topology such as the ring oscillator is particularly intriguing. The primary advantage of the FeFET-based oscillator lies in the tuning capability of the polarization. By tuning an additional property of the transistor relative to the MOSFET, the potential for a further adjusted operating frequency range exists. Principally, an oscillator’s operating frequency is a function of the delay of each stage in the design. For this reason, fewer stages are often advantageous as it provides fewer delays and yields an overall higher frequency. When using ferroelectric transistors in oscillator designs, however, additional stages allow for different topologies that are capable of polarizing the ferroelectric gate to varying degrees.

The generalized ring oscillator design, as shown in Figure 4.7, is one of the simplest oscillator designs, and as such allows significant modifications depending on the frequency range of interest and design constraints. Overall, the design of the ring oscillator is such that the input to the first stage is simply the output of the last stage, where the design contains 2N+1 stages. The requirement to have an odd number of stages is derived from the fact that the circuit must be astable, or not stable in either output state (the output of a single inverting stage being either “high” or “low”). This astable nature results in a continual switching of the output states for each inverting stage. However, loading at each stage output causes a delay in the transition time for the output to rise or fall accordingly. For an oscillator with similar stages, or delay cells, the operating frequency is readily defined as given by Equation (4.1), where the average
single stage delay is represented by $\tau_{\text{Stage, Delay}}$ and the oscillator is composed of $2N + 1$ stages.

$$f = (2N + 1)\tau_{\text{Stage, Delay}}$$  \hspace{1cm} (4.1)

Omitted from this function are the independent variables that determine the delay of each stage. As the inverting stages often take the form of a CMOS inverter or even resistive load inverter, several key factors driving the operating frequency are supply voltage and temperature. Of course, stage loading also plays a tremendous role, but for a given hardware arrangement, supply voltages, and operating temperature the load is completely determined. For this reason, ring oscillators of this type see use in temperature sensors and manufacturing quality control.

![General ring oscillator structure](image)

**Figure 4.7:** General ring oscillator structure, with each stage denoted as an inverter having an output resistance and load capacitance characterized as shown by the discrete elements

As the ring oscillator belongs to the class of voltage-controlled oscillators (VCOs), a primary function is the ability to change the oscillation frequency using an input voltage. The tuning voltage typically adjusts a resistance or capacitance in or biasing of the circuit. In more complex designs, the tuning voltage may connect different stages, bypassing some delay stages to increase the oscillating frequency significantly. Implementations using a MOSFET therefore are limited by the extent to which the operating frequency can be adjusted as the control voltage changes the biasing point of
the stages and in turn delay of the stages to change the frequency. It is in this area that ferroelectric devices – specifically the ferroelectric transistor – are able to offer additional appeal by adjusting multiple device parameters.

(i) Ferroelectric Stage Delay

In general, an inverting stage using a ferroelectric transistor has not only the biasing point changed simply by adjusting the control voltage but also the polarization state, which may arise from changes in the control voltage as well as basic circuit operation. Compounding the effects of the polarization on the device characteristics, the gate capacitance also changes according to the polarization state, which directly influences the loading experienced by the preceding stage. By having substantially different operating characteristics for each ferroelectric device, the circuit achieves operation that depends heavily on both the particular control voltage and polarization state. In this manner, the delay of a ferroelectric stage is adjusted. With the tuning range of the circuit determined by the delay of each stage, the total tuning range is defined by the maximum and minimum delays of the circuit.

Often the ideal tuning range for an oscillator is exceptionally wide, that is to say for a single circuit design the operating frequency is variable across a large range. Having the frequency variation vary gradually across the range as tuned by the control voltage allows selection of any particular frequency between the extremes. As mentioned previously, more sophisticated designs are able to add or remove delay stages depending on the control voltage by bypassing different circuitry in the design. In this work, the principal concern is simply the extent to which the delay of the ferroelectric stage can be
Manipulated as in general any number of stages may be converted to using ferroelectric transistors, including stages in more sophisticated designs.

For design and testing of the ring oscillator, the FeFET inverting stage is constructed as a resistive load inverter, as shown in Figure 4.8. This design decision results from the differing channel resistance between the n-channel FeFETs supplied by Radiant Technologies, Inc. and commercially available p-channel MOSFETs, making the CMOS inverting circuit more difficult to construct. Typically, inverting stages use both n-channel and p-channel transistors to construct a CMOS inverter as shown in Figure 4.9.

![Resistive load inverter configuration](image)

Figure 4.8: Resistive load inverter configuration used for inverting stages in the ring oscillator, where either a MOSFET or FeFET may be used as the n-channel transistor.
The primary advantage of the CMOS inverter over a resistive load inverter lies in the static power dissipation. For the resistive load inverter, a static power draw is present in the circuit whenever the input voltage is above the transistor threshold voltage. On the other hand, only one of the transistors of the CMOS inverter is on at a single time for either input state, thereby restricting power consumption to only the switching power dissipation or dynamic power draw through the circuit. Due to the placement of the PMOS transistor, only during the input voltage transition do both transistors turn on simultaneously, allowing current flow through the transistor pair. Otherwise, current flows from the power source to the load through the PMOS circuit only during the transition, assuming a capacitive load. Because of the intermittent power draw, the power consumption of the CMOS stage is found by Equation (4.2), which is dependent upon the load, frequency and supply voltage used.

\[ P_{avg} = C_{load} V_D^2 f \]  \hspace{1cm} (4.2)
Maintaining a small amplitude in the CMOS inverting stage is particularly important for low power designs since the power consumption of a switching CMOS inverter varies with the square of the supply voltage.

Polarization modulation in the FeFET principally alters the drain current as well as gate capacitance. Examining first the drain current, if the transistor becomes positively poled, then the drain current decreases due to the semiconductor channel reducing as a result of the dipole moment in the ferroelectric material increasing the depletion region as outlined in chapter II. The smaller current has the effect of increasing the transition time or slowing down the inverting stage by restricting the current flow and not allowing the capacitive load to discharge quickly. Conversely, when the transistor gate is negatively poled the drain current increases, which allows the output voltage swing to transition more quickly than in the positively poled state. Therefore, the negatively poled state decreases the transition time or reduces the delay of the inverting stage. In both states the output voltage swing from low to high is largely unaffected by the polarization state as this transition time is largely driven by the load resistance selected for the transistor. Given a high input voltage, the output voltage varies with polarization state. The degree to which the output voltage varies depends on the load resistance selected; since the FeFET operates similar to a resistor corresponding to the channel resistance of the current polarization state, the modulation in channel resistance alters the output voltage. This configuration essentially produces a voltage divider where modulation of the FeFET channel resistance by way of the polarization can raise or lower the output voltage. The primary design consideration here is that the output voltage when
a high input voltage is applied, $V_{OL}$, be sufficiently low as to be considered a low input to the successive stage, at or below $V_{th}$ of the following stage.

Using only the modulation of the FeFET inverting stage transition time driven by the polarization state, the oscillator operating frequency is variable between the minimum observed using a positively poled state and the maximum with a negatively poled state. Between the two extremes, a partial polarization state allows for any operating frequency between the two. Variation thus far is achieved only through the use of the ferroelectric material polarization. However, to observe a steady-state difference between the two polarization states, the poling voltage must be larger than the supply voltage applied to the FeFET gate for a “high” voltage level. Otherwise, the hysteresis point for both states is coincident as seen from the current hysteresis in Figure 2.15 where, at the maximum applied voltage, both the positively and negatively poled states (current states) are identical. Therefore, ideally the poling voltages used are beyond the range experienced at the gate during normal operation, and in this manner ensuring a degeneracy of the current at either input voltage depending on the polarization state.

Methods for polarizing the FeFET gate using a voltage outside of the range that would normally be applied can be implemented in several ways. The first, and probably the most straightforward, method is found by simply inserting an adder circuit directly in front of the FeFET gate, being fed by the output of the earlier inverting stage as shown in Figure 4.10. The general concept is that the final inverting stage passes through some amplifier or attenuator, indicated as the gain block “a”, prior to entering the summing junction which contains the desired poling offset voltage. The addition of a gain block allows the voltage applied to the FeFET gate to never deviate so far as to damage the
ferroelectric layer, for which ferroelectric breakdown is a serious concern similar to gate breakdown in a MOSFET. If the combination of the inverter output voltage and poling offset voltage exceeds the limits of the FeFET gate, then the inverter output voltage can be attenuated to reduce the magnitude of the voltages applied to the FeFET gate (|α| < 1). Also, depending on the magnitude of the poling offset voltage, the oscillator may not continue operating during poling. If the offset voltage used is large enough and the continued operation of the oscillator is required, the gain block may need to amplify the signal coming from the final inverting stage (|α| > 1). One advantage of this method is that after the initial poling of the FeFET, the offset voltage can be reduced greatly and used as a minor offset voltage for fine tuning in the neighborhood of the poling state. Another advantage of this configuration is that the adder and amplifier can be added to a ring oscillator with any odd number of stages without worry of each non-ferroelectric stage operating as intended. The principal drawback is the additional circuitry or devices required for the poling method in combination with the requirement that both be capable of operating reasonably well throughout the frequency range of the oscillator, which given the desired operating frequency of the oscillator may not be a minor requirement.

Figure 4.10: Adder method for FeFET ring oscillator poling, shown for a three-stage ring oscillator

A second method used to pole the FeFET gate involves gradually stepping down the voltage range used by successive CMOS inverting stages as illustrated in Figure 4.11.
In this configuration, the ferroelectric inverter and first CMOS inverter operate using the unaltered positive supply voltage, $V_{DD}$, and negative supply voltage, taken as ground in this example. However, each of the successive CMOS inverters use modified negative supply voltages feeding the n-channel transistors, $Q_{n2}$ through $Q_{n4}$. This configuration allows the voltage applied at the FeFET gate to be more negative than otherwise allowed and negatively poles the FeFET during a portion of the cycle. Since the positive voltage is unchanged, the effects of the negative poling are seen in only a portion of the waveform, provided the positive supply voltage is sufficiently large to positively pole the gate. Even for small supply voltages, the astable state of having a high input to the FeFET gate will be a destructive operation as the polarization is reversed to an extent.

Despite the shortcomings of this design, the configuration being discussed has the inherent benefit of simplicity. Not introducing additional circuity allows the oscillator to operate at higher frequencies by not introducing further delays or encumbering the design with the frequency response of the amplifier and summer circuits shown in Figure 4.10. The single-sided stepping method as discussed here allows the operation to highlight the polarization switching during and after the output transitions and the effects on the gate capacitance as switching potentially occurs every cycle. The primary drawback to this configuration is the continual widening of the output voltage ranges for later inverting stages. A larger transition window increases the power consumption of the oscillator as indicated by Equation (4.2), where the term $V_{DD}$ is more generally replaced with the total voltage transition, here equal to $V_{DD} + |V_{SS}|$. Of note is the idea that the implementation of constructing the necessary negative supply voltages shown in Figure 4.11 is notional.
In general, a more sophisticated design to allow for loading during transitions is required to have reasonable performance.

![Single-sided poling method for the FeFET ring oscillator](image)

**Figure 4.11**: Single-sided poling method for the FeFET ring oscillator, shown as applied to a five-stage ring oscillator

Lastly, an extension on the single-sided poling method modifies both positive and negative supplies in concert with one another. The tuning voltage appears in series with the supply voltages such that the overall voltage swing for each inverter is constant. This addition allows the power consumption of the oscillator to remain comparable to that of the original ring oscillator design. One such implementation shown in Figure 4.12 defines the p-channel transistor source voltage relative to the n-channel source voltage. By keeping the difference in source voltages constant (all DC supply voltages being equal to \( V_{DD} \) in this example), the power consumption is reduced relative to the single-sided ring oscillator poling method. The second supply voltage, the tuning voltage \( -V_{SS} \), may be positive or negative to induce the needed poling voltage at the FeFET gate. To a greater extent than seen with the single-sided poling circuitry, the tuning voltage can only deviate far enough to ensure the output voltage of the resistive load inverter still satisfies the input requirements of the first CMOS inverting pair. As the ferroelectric transistor current is typically the stricter requirement on tuning voltages, the continued operation of
the first CMOS pair is often the primary concern. However, if the tuning voltage magnitude is allowed to increase too far, then the second and successive CMOS pairs will no longer switch. The limits of the tuning voltage depend on the threshold voltages of the transistors used, including the ferroelectric transistor, along with the supply voltage. If oscillator operation is not needed during poling, these conditions may be neglected. Typically, especially small supply voltages, relative to the voltages needed to pole the FeFET gate, result in the most confining of tuning voltage ranges.

![Figure 4.12: Double-sided FeFET ring oscillator poling method, shown as applied to a five-stage ring oscillator](image)

For each poling method discussed, the overall ring oscillator was modified in some fashion, which will affect the operating frequency as the tuning voltage varies. This arises as a result of not only changing the ferroelectric transistor polarization state but in so doing also adjusting the biasing of the CMOS inverters. The exception to this is the adder method, though further restriction on the operating range may be imposed. Also of note is the fact that the duty cycle adjusts over the tuning range. This results from the change in the voltages applied at the transistor gates causing the transitions to occur sooner or later, depending on the tuning voltage used. Additionally, the gate
capacitance of the FeFET varies with the polarization state, substantially so at the
transition points. With this in mind, for optimal performance tuning the circuit for lower
frequency operation may aim to either continually switch polarization or attempt to
operate in this region for long periods of time using smaller supply voltages. Conversely,
for higher frequency operation the gate capacitance should be minimized, causing
constant polarization switching to be sub-optimal in many respects. Through careful
consideration of each of these design aspects, the FeFET may be used in the ring
oscillator – as well as other circuits – as a widely varying tuning element, capable of
altering device parameters to an extent greater than observed when using the MOSFET or
similar transistors.

(ii) Three-Stage Topology

A three-stage ring oscillator uses precisely the same configuration as shown in
Figure 4.7, but consists of only three inverting stages connected together. In general,
advantages of a three-stage design include reducing the number of devices and delay
stages, higher operating frequencies, and increased dependence on the delay of each
stage. The greater dependence of the operating frequency on each stage results from each
stage contributing on average one-third of the overall delay, assuming equal contributions
for each stage. With this in mind, FeFET tuning excels in three-stage designs when
harnessing the full capability of the transistor.

The limiting factor for three-stage implementations, however, is often the
operating frequency relative to the polarization time scale. As the operating frequency
increases and the time spent poling the FeFET gate decreases, the effects of the
polarization diminish as the polarization is not completely set or written to prior to the

next cycle or transition depending on the method employed. Attempts to slow the circuit operation counteract the intended benefit of three-stage topologies generally operating at higher frequencies. This limitation can be mitigated through different FeFET manufacturing, namely reducing the thickness of the ferroelectric as the time to polarize the material is proportional to the thickness of the layer.

For the FeFETs supplied by Radiant Technologies, Inc., data are first collected using the single-sided poling technique show very limited results. Due to the few stages, the tuning voltage can only be adjusted over a reduced range. The limiting factor in this configuration is the threshold voltage of the MOSFETs used to construct the CMOS inverters. The inverter directly following the FeFET inverter is similar to a rectifying circuit, as it adjusts the output voltage to be between $V_{DD}$ and, in this case, ground while also inverting the signal. As the tuning voltage decreases, the n-channel MOSFET in the second CMOS inverter turns on regardless of the output state of the rectifying inverter. For this configuration the limit on the tuning voltage is approximately $-V_{th}$ of the n-channel MOSFET, which greatly restricts tuning to approximately 0 to -1 V only.

As expected, for the three-stage ring oscillator a circuit similar to the adder-style poling setup must be used for wider tuning ranges. Using the adder poling circuitry at the FeFET gate, a tuning voltage extending down to -4 V or even -5 V may be used. Of particular interest is the duty cycle of the ring oscillator, which generally lies in the range of 10-20% as measured at the FeFET gate. Duty cycle measurements, which represent the fraction of the total period ($T$) that the waveform is in the “high” state ($t_{ON}$) as given by Equation (4.3), indicate that the FeFET is typically attempting not to conduct during a substantial fraction of the waveform.
\[ D = \frac{t_{ON}}{T} \]

Having a very low duty cycle at the FeFET gate indicates that the circuit favors the FeFET inverter output being in the “high” state, or rather that the time to propagate through the remaining two inverters is longer in this state. To explain this, the output state of the FeFET inverter is examined. In the “low” gate voltage state defined by the tuning voltage, the FeFET drain voltage reaches a maximum determined by the load resistor, FeFET in use, and polarization state. As the FeFET gate voltage reaches the minimum and the polarization switching occurs, reducing the threshold voltage of the FeFET, a channel and drain current remain in the semiconductor. As a result, the “low” gate voltage does not completely turn off the FeFET as may be expected. Instead, the FeFET continues conducting current, at a severely reduced amount, and the FeFET drain voltage does not reach the positive supply voltage, \( V_{DD} \). The negatively poled state (relatively) is therefore seen as acting to counteract the gate voltage in the low state to a small degree, causing the rectifying CMOS inverter not to transition as quickly as observed with a “high” input at the FeFET gate.

Interestingly and intuitively, as the tuning voltage decreases further, the duty cycle of the signal applied to the FeFET gate increases, reaching a maximum of approximately 20% for the ND1 FeFET as shown in Table 4.1. As the tuning voltage, and therefore the (negative) voltage applied to the FeFET gate, decreases then the FeFET drain current reduces despite having a negatively poled gate. This results from the negative gate voltage being able to overcome the increased carrier concentration incited by the polarization state, with the end result being that the duty cycle continues to increase as the “high” and “low” input states approach each other.
Table 4.1: Three-stage ring oscillator operating frequency and duty cycle measurements made using the ND1 FeFET

<table>
<thead>
<tr>
<th>$V_{Bias}$ (V)</th>
<th>Frequency (kHz)</th>
<th>Duty Cycle (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>63.6</td>
<td>11.1</td>
</tr>
<tr>
<td>1.0</td>
<td>64.1</td>
<td>12.9</td>
</tr>
<tr>
<td>0.5</td>
<td>66.2</td>
<td>14.2</td>
</tr>
<tr>
<td>0.0</td>
<td>65.7</td>
<td>14.0</td>
</tr>
<tr>
<td>-0.5</td>
<td>66.4</td>
<td>13.8</td>
</tr>
<tr>
<td>-1.0</td>
<td>68.4</td>
<td>14.4</td>
</tr>
<tr>
<td>-1.5</td>
<td>69.6</td>
<td>14.3</td>
</tr>
<tr>
<td>-2.0</td>
<td>70.0</td>
<td>14.2</td>
</tr>
<tr>
<td>-2.5</td>
<td>71.4</td>
<td>16.1</td>
</tr>
<tr>
<td>-3.0</td>
<td>71.3</td>
<td>16.5</td>
</tr>
<tr>
<td>-3.5</td>
<td>70.8</td>
<td>18.4</td>
</tr>
<tr>
<td>-4.0</td>
<td>70.4</td>
<td>21.3</td>
</tr>
</tbody>
</table>

(iii) Five-Stage Topology

In the five-stage ring oscillator topology, two additional stages are added to the three-stage design, which is shown to possess limited negative poling options due to the limited number of stages. Having introduced two additional stages, the two additional methods for introducing the negative poling operation of the circuit are achievable in the single- and double-sided stepping methods. Whereas in the three-stage topology the idea of gradually stepping down the source voltages of the CMOS inverters could not be performed due to the threshold voltages of the MOSFETs used, spreading out the transition over the course of a total of three CMOS inverter pairs allows for adequate voltage stepping at each stage. For the n-channel MOSFETs used here, the threshold voltage lies between 0.8 and 3.0 V, typically close to 1.5 or 2.0 V. Similarly, the p-
channel MOSFETs used in empirical data collection have threshold voltages ranging from 1.5 to 3.5 V, again typically close to approximately 2.0 V. Over the course of three stages, the voltage is therefore adjustable down to approximately -5 V, the minimum voltage evaluated for the tuning voltage. This minimum is maintained regardless of the number of stages for this style of topology owing to the drain voltage of the FeFET. In the limiting case of applying -5 V at the FeFET gate, the drain voltage will be some value less than the positive supply voltage, which was taken to be +5 V, depending on the leakage current of the FeFET. This will in general result in a gate-to-drain voltage having a magnitude less than 10 V, which is beyond the 8 V limit typically imposed on these transistors.

First, the single-sided stepping configuration is considered as this is the simplest of all evaluated poling methodologies. Using a tuning voltage, shown as \(-V_{SS}\) in Figure 4.11, between 0 and -5 V allows each stage to have no more than 1.7 V difference in n-channel MOSFET source voltage, which allows each stage’s continuing to invert as the tuning voltage varies. Based upon the preceding discussion surrounding the effects of decreasing the n-channel MOSFET source voltage, the frequency is often expected to increase with increasingly large, negative tuning voltages. Indeed, the ring oscillator implemented using the ND4 FeFET shows this vary trend as illustrated in Figure 4.13. As the non-positive tuning voltage magnitude increases, the operating frequency increases along with the duty cycle. With the addition of the two additional stages, the load resistance is able to be selected such that the duty cycle is near 50% throughout the range of tuning voltages, which is in contrast to the three-stage oscillator which had a considerably tenuous tuning voltage range as the duty cycle increases to toward 50%. Of
note is the fact that the operating frequency is substantially lower than typical oscillator circuits. This results firstly from the number of stages and devices used and also from the delay elements, introduced as external load resistors and capacitors as indicated in Figure 4.7. By slowing the operating frequency, the FeFET ferroelectric gate is provided additional time to completely polarize, which is necessary for the 350 nm PZT layer to have sufficient time to switch polarization states. Also of note is the fact that as the tuning voltage magnitude increases, the output swing of each CMOS inverter increases, which introduces an increased delay. Similarly, the subsequent CMOS inverter does not complete switching until the voltage drops to an even lower value, determined by the threshold voltage of the n-channel MOSFET relative to the source voltage. These two effects serve to decrease the operating frequency of the oscillator in general, and in this case the FeFET is able to overcome both aspects of the circuit and in addition to increasing the operating frequency. The trend of the duty cycle in this configuration is exactly the same as that of the three-stage topology examined earlier.
Figure 4.13: Empirical operating frequency (blue) and duty cycle (orange) measurements of a five-stage ring oscillator with an ND4 FeFET using a tuning voltage ranging from 0 V to -5 V

For the ND1 and ND7 FeFETs, the operating frequency does not monotonically increase with increasing tuning voltage magnitude as with the ND4. With the ND1 FeFET, the operating frequency instead initially remains constant as the tuning voltage drops. As the tuning voltage approaches -2 V, the operating frequency instead begins decreasing at a nearly linear rate as indicated in Figure 4.14. Due to the 16 times smaller gate contact area and one quarter of the channel length relative to the ND4 FeFET, the polarization is anticipated to have a lessened effect, as noted by the width of the current hysteresis.

![Graph showing operating frequency and duty cycle as a function of tuning voltage for ND1 FeFET.]

Figure 4.14: Empirical data of the five-stage ring oscillator operating using an ND1 FeFET showing operating frequency (blue) and duty cycle (orange) as a function of tuning voltage

On the other hand, the ND7 FeFET has the same gate contact area as the ND4 FeFET, with a much wider and shorter channel. As a result, empirical data collected with the ND7 FeFET show a trend akin to the merging of the two devices: initially the
operating frequency decreases, again at a near linear rate, as presented in Figure 4.15. However, at approximately -3.5 V, the operating frequency begins increasing as the tuning voltage approaches a magnitude sufficiently large enough to negatively pole the transistor gate during a fraction of the waveform and overcome the increased delays caused by the tuning voltage’s effects on the CMOS inverters in the circuit. As the tuning voltage is lowered further, the frequency eventually stabilizes, increasing slightly from the minimum. The load resistance is again selected to produce a duty cycle near 50% across the tuning voltage range. Here the duty cycle, measured at the FeFET gate, increases as the frequency decreases. Considering the channel resistance of the FeFET as the non-positive tuning voltage increases in magnitude, the FeFET is increasingly negatively poled, at least for a significant portion of the cycle. In this state, the channel resistance is smaller due to the increased carrier concentration and drain current larger than seen in the positively poled state exists. This in turn reduces the output voltage slightly from the maximum that would otherwise be seen and helps to increase the duty cycle, encouraging the circuit to remain in the state resulting in an active or “high” FeFET gate voltage for longer periods of time.
Figure 4.15: Empirical data of the five-stage ring oscillator operating using an ND7 FeFET showing operating frequency (blue) and duty cycle (orange) as a function of tuning voltage

C. Depletion Mode Operation

In many applications that would otherwise use a p-channel MOSFET, a depletion mode transistor accomplishes a similar function. By utilizing the polarization of the FeFET ferroelectric layer, the transistor operates as either an enhancement mode transistor or as a depletion mode transistor [49, 91]. This concept of using a FeFET in place of what would typically be a depletion mode MOSFET has advantages in both complexity of additional ion implantation and, potentially, cost. However, so-called pseudo-NMOS circuits, or circuits constructed using a PMOS transistor that is always on, have advantages in terms of noise margin and needing only a single power supply. Instead, all ferroelectric transistors can be manufactured similarly and simply use the polarization to adjust the threshold voltage as needed. If sufficiently negatively poled, the FeFET acts as a depletion mode transistor by forming a channel in the semiconductor. In this state, the polarization of the PZT layer repels the carriers from the ferroelectric-
semiconductor interface, stimulating an increased carrier concentration in the semiconductor channel that is positioned opposite the ferroelectric material.

Interestingly, the degree to which the channel forms is modulated by the extent of the polarization state. In the event that the PZT ferroelectric layer is only partially polarized, the threshold voltage is reduced but only slightly. This partial polarization then creates a scenario where the channel extent or conductivity is tunable based on the applied gate voltage waveform. The ferroelectric transistor is therefore able to accommodate a wide range of desired ion concentrations, which may vary depending on application and circuit, using a single device. Setting the desired polarization state is simple through the use of both positive and negative gate voltages, relative to the drain and source terminal voltages. As shown for the partial polarization current hystereses in chapter II, the zero-bias drain current, or drain current with 0 V applied at the gate relative to the source terminal, defines the extent of the polarization state.

Depending on the circuit used, the depletion mode ferroelectric transistor can also act as a variable load. Using one or more supply voltages, the polarization state may be set to construct an arbitrary load. A setup similar to that shown in Figure 4.16 accurately polarizes the transistor ferroelectric gate to ensure the necessary resistance. This particular circuit configuration uses a similar source and drain voltage to incite a near uniform polarization of the ferroelectric layer. The polarization decay, exacerbated by the destructive operating voltages, requires a refresh cycle with the period determined by the circuit conditions – namely relative gate voltage. By allowing a FeFET to switch between either depletion or enhancement mode spontaneously, different modes of circuit operation are obtained using a single design. As a result, use of FeFETs in a circuit can
allow for reconfigurable circuits such as logic gates or simply different operation in general. Owing to the non-volatile nature of the polarization retention, ferroelectric transistors may then be able to act similar to a field-programmable gate array (FPGA), which are built using many reconfigurable circuits for versatile and efficient operation.

![Ferroelectric transistor partial polarization circuit configuration for depletion mode operation](image)

Figure 4.16: Ferroelectric transistor partial polarization circuit configuration for depletion mode operation

D. Integrated Sensors

Using the properties of the ferroelectric layer allows the FeFET to act as an integrated sensor. The ability of the ferroelectric layer to sense external stimuli is the defining feature of the material that allows use as a sensor, where the sensing property is considered as the ability of the ferroelectric material to alter the electric polarization state resulting from changes in the environment. An applied force on the device, or more specifically the ferroelectric material, produces a stress on the device. Resulting from the stress and depending on the magnitude, the ferroelectric material deforms slightly. As the material deforms, an electric potential difference across the material develops. Principally, the slight displacement of the positively charged central ion forms the polarization shift observed with an applied force. However, as discussed in chapter II, in a reference frame defined by stationary oxygen anions, the lead cations also displace slightly and substantially contribute to the overall polarization.
For room temperature 20/80 PZT, the primary material of interest in this work, the material is in the tetragonal phase, as shown by Figure 2.4. In this region, the ferroelectric crystal tends to elongate along an axis normal to the applied force. That is to say, the lattice parameters $a$ and $b$ are equal initially and $a < c$ as referenced in Figure 2.5 for 80% mole fraction PT. A force on either the “$a - c$” or “$b - c$” side as shown in Figure 4.17 incites further polarization of the material, causing a slight furthered elongation of the crystal along the axis of polarization. In this scenario, the central ion ($Zr^{4+}$ or $Ti^{4+}$) continues to displace along the axis of original polarization, normal to the applied force. The additional expansion along the polarization axis alters the polarization state, increasing the magnitude of the polarization. As an essentially standalone device, the ferroelectric material can act as a sensor by generating charge on the material resulting from the dipole moment created as a result of the polarization state. Similar to a ferroelectric capacitor, the voltage across the material can be sampled and the state of the device determined. This extends to sensing, wherein the voltage across the capacitor indicates the experienced force on the material. If, however, the material is incorporated in a FET as with the FeFETs used here, the channel resistance, resulting from the voltage, is modulated owing to the polarization state. Here, sampling of channel resistance, or equivalently the drain current, obtains an estimation of the polarization state allowing sensing of applied forces. Therefore, the ferroelectric layer polarization state defined by initial conditions combined with an applied force then translates to conductivity changes in the semiconductor, which must be sampled to determine the force applied at any given point. Additionally, as with a ferroelectric material acting as a sensor in a capacitor, the state of the polarization must be continually sampled and
estimated as the polarization state has a time dependence after the force is removed or as the force varies with time, which influences the initial conditions for the next reading. In general, physical forces or vibrations occur on a much shorter scale than electronic measurements, allowing somewhat relaxed timing constraints on the sensor design.

Figure 4.17: Depiction of lateral applied force on the PZT crystal and evoked polarization and deformation as a result of the force with axis convention as indicated

The configuration depicted in Figure 4.17 shows a somewhat idealized case for using a ferroelectric material as a sensor which does not precisely translate to the case of application of a ferroelectric layer being used in a FeFET sensor. The primary issue here stems from the fact that the polarization vector must be normal to the plane formed at the semiconductor-ferroelectric interface in order to modulate the semiconductor carrier concentration most effectively. As a result, the force to be sensed should be applied laterally to add directly to the existing polarization vector; the axis convention shown in Figure 4.17, indicates a force must then be applied in the $Y-Z$ plane having no or negligible component in the $X$ direction. Of note is that this discussion assumes shear force may be neglected for the PZT layer. The essence of this assumption is that the force is applied on the PZT material directly rather than on the structure atop which the PZT layer resides.
If the direction of the force is parallel to the polarization vector, the polarization will still change, though in a different manner. In this case the force acts against the current polarization state, reducing or destroying the polarization as shown in Figure 4.18. This too can be measured precisely, however, with the initial polarization state known—perhaps resulting from being set between external stimuli—the effects of the stress on the PZT polarization is evident again through the careful consideration of the channel resistance and drain current. In this scenario the rate of change of the drain current with respect to time, \( \frac{\partial i_{ds}}{\partial t} \), is either positive if the polarization state was acting to reduce the carrier concentration or negative if the polarization state was initially acting to increase the carrier concentration. Alternatively stated, the force in this case works to reduce the polarization, returning the polarization state toward the unpolarized “midpoint” of the two drain current extremes.

Figure 4.18: Depiction of force applied parallel to the direction of the PZT crystal initial polarization and resulting deformation of the crystal

To construct an effective FeFET, the dimensions are often designed in order to satisfy drain current requirements while allowing both drain current variability with respect to polarization state and operation at the desired frequency. As discussed in
chapter II, the thickness (or extent of the material in the $X$ direction) results in slowed operation owing to the increased gate capacitance and time required to pole the material in addition to the need for larger voltages to produce the same electric field, which in turn stresses the slew rate of the circuit design. The thickness of the material must be balanced alongside the desire to have drain current variability with the polarization state, which benefits from added material in the $X$ direction to increase the effects of polarization on current. Typically, the $X$ extent of the material will be considerably smaller in comparison to the remaining two dimensions. The channel length and width describe the drain current observed owing to the distance across which the carriers move in conjunction with the number of carriers allowed (effectively controlling the area over which the current density is present). In the FeFETs used in this work, the width ($Z$) is at least as long as the length ($Y$), both of which are more than an order of magnitude larger than the PZT thickness as shown in Table 2.1.

(i) **Pressure Sensor**

Pressure, in the form of atmospheric pressure or more generally any force resulting from contact with a liquid or gas, is able to stimulate and alter the FeFET ferroelectric layer polarization provided the transistor has a structure allowing the pressure to apply a force on the ferroelectric layer. Resulting from the applied pressure, the ferroelectric layer exhibits an electric polarization proportional to the force, dependent on the direction and initial conditions. As discussed earlier, the response of the PZT polarization for the FeFETs of interest is directly dependent on the direction of the applied force. With this in mind and given the structure of the FeFETs, a largely “exposed” ferroelectric gate is used as the sensing mechanism. Although a platinum
contact is fixed atop the PZT layer at the gate, the pressure applied on the large surface area of the gate contact will in turn press upon the ferroelectric material as shown in Figure 4.19. The resulting force has contradictory terms in the context of the PZT polarization, but the relatively small thickness of the material circumvents this unfortunate byproduct of the structure. The component of the force acting parallel to the polarization vector, $F_X$, works to reduce the polarization vector, whereas the remaining orthogonal components, $F_Y$ and $F_Z$, counteract this effect by helping to grow the current polarization state.

![Figure 4.19: FeFET pressure sensor under measurement conditions with applied force acting on the FeFET ferroelectric gate](image)

For a pressure sensor experiencing an isotropic pressure or force, the net polarization state is overwhelmingly responsive to the component normal to the principal contact area. As shown in Table 4.2, the area upon which the pressure is applied to a surface tangential to the polarization vector is dwarfed by the area computed considering only those surfaces orthogonal to the polarization vector. This trend is again due to the relative thickness of the PZT layer as compared to the width and length dimensions. Because of this, the extent to which the pressure destroys the polarization state is easily
detectable via channel resistance or drain current measurements, which then provides an estimation on the experienced.

Table 4.2: Areas of the different FeFETs upon which the isotropic pressure acts

<table>
<thead>
<tr>
<th>FeFET</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
<th>Thickness (µm)</th>
<th>Tangential Area (µm²)</th>
<th>Orthogonal Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ND1</td>
<td>10</td>
<td>10</td>
<td>0.35</td>
<td>14</td>
<td>100</td>
</tr>
<tr>
<td>ND4</td>
<td>40</td>
<td>40</td>
<td>0.35</td>
<td>56</td>
<td>1600</td>
</tr>
<tr>
<td>ND7</td>
<td>400</td>
<td>4</td>
<td>0.35</td>
<td>282.8</td>
<td>1600</td>
</tr>
</tbody>
</table>

In designing the sensor, the dimensions of the devices in use are of particular importance. When considering an isotropic pressure application, the resulting effects of the polarization on the channel resistance must be amplified after a measurement to account for the decreased sensitivity in the material resulting from the exposure to additive and destructive components. Owing to the sensitivity in measurement and a priori knowledge of the device structure, an appropriate “gain” can be applied to the detection. The sensitivity of the measurement circuitry will then be dictated not only on the precision required of the sensor but also taking into account the slightly degraded sensitivity of the measurements.

(ii) Accelerometer Sensor

Using the ferroelectric polarization as the basis for the sensor, the FeFET is also useful when acting as an accelerometer. Similar to operation as a pressure sensor, the forces exerted on the ferroelectric material are now restricted to a single vector, \( F = F_X + F_Y + F_Z \). Using the same coordinate system as depicted in Figure 4.17, the force acting principally in the \( X \) direction serves to reduce the polarization whereas a force acting
along either or a combination of the two remaining principal axes enhances the polarization state. Immediately, an ambiguity arises in the design where a single FeFET is capable only of determining the direction of a force only if the force is normal parallel to the polarization vector.

In the limiting case of a force’s being restricted to a single Cartesian basis vector, only two FeFETs are required if oriented such that the polarization vector of each lies along a unique basis vector. In this contrived scenario, the alternating growth and decay of the polarization states in each FeFET or synchronized increase in polarization lends itself to a unique solution for the force as shown in Table 4.3. Although this situation initially appears very non-physical, this is in fact simply a reduction in the desired accuracy of the accelerometer. That is to say if the detection of a force need only determine the direction and very rough estimation of magnitude, then the two FeFET case is the minimum set in \( \mathbb{R}^3 \). As the demand for the sensor accuracy increases, so does the number of FeFETs needed. Extending to the opposite extreme of infinitely many FeFETs, only \( 2\pi \) need be sampled of the possible \( 4\pi \) angles owing to the directionality being detectable for a force oriented in an arbitrary direction or the reverse (negative) of that same direction.

Table 4.3: Polarization state change for a two FeFET accelerometer restricted to experiencing forces only along the coordinate basis vectors

<table>
<thead>
<tr>
<th>Principal Direction</th>
<th>FeFET #1 Polarization</th>
<th>FeFET #2 Polarization</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>Decrease</td>
<td>Increase</td>
</tr>
<tr>
<td>Y</td>
<td>Increase</td>
<td>Decrease</td>
</tr>
<tr>
<td>Z</td>
<td>Increase</td>
<td>Increase</td>
</tr>
</tbody>
</table>
As with any sensing device using a ferroelectric material, the FeFET accelerometer requires a known initial condition. This arises from the fact that the drain current hinges so strongly on the polarization state and minor changes or perturbations in the state may be mistaken for a large force if the previous state is not considered. Documentation on currently available sensors using piezoelectric devices note the ability to measure dynamic changes in the environment but struggle with steady state measurements due to the decay in the response over time [80, 156]. However, for the FeFET of interest here using PZT as the ferroelectric material, retention of the polarization state is exceedingly strong to the point of being classified as non-volatile for memory applications. While this strength of the PZT FeFETs produced by Radiant Technologies, Inc. results in more sophisticated memory cells, it also allows for better detection of conditions to include steady state stimuli. First, the polarization state must be set to a known position through a poling voltage, though care must be taken to ensure saturation over the region of operation will not be considered. From here, periodic measurements of the drain current yield the present polarization state, which given the initial condition completely describes the difference in the two states – or the effect of the force imparted on the device. Depending on the measurement frequency of the device, which is a function of the expected frequency of the forces, the polarization state may be reset, ensuring saturation levels are not encroached upon, or allowed to meander over time. The non-volatile nature of the polarization allows for less frequent measurements during periods with no or slowed forces as the polarization decay over time is well described from the time evolution of the system in the current state. A primary advantage of the FeFET sensor over that of a ferroelectric capacitor is that parasitic resistances in
the device or leakage current in the ferroelectric layer are not expected to reduce the channel resistance. This stems from the fact that the capacitor variant of the ferroelectric sensor relies on charge measurement across the capacitor, which necessitates more frequent measurements and reduces effectiveness for steady state applications.

E. Conclusion

The FeFET is one of the most versatile devices when the full capability of the ferroelectric material is realized. With ferroelectric materials seeing use in several memory applications, inclusion in a transistor opens many additional opportunities. Not only is the non-volatile nature of ferroelectrics capable of storing data, but the overall mode of operation – including both current and capacitance – is altered. Though further complexities in fabricating FeFETs are introduced, the additional effort expended may more than make up for the advantages introduced in the circuit.

As one of the primary uses of ferroelectrics is memory applications, the non-volatile storage afforded to the FeFET by way of the ferroelectric gate allows for additional storage in one of the simplest memory design, the 1T1C memory cell. By maintaining the same minimum number of devices in the memory cell and adjusting read circuitry, the ferroelectric polarization stores a bit in addition to the voltage across the storage capacitor, doubling the potential storage capacity. However, the usefulness of the FeFET in the 1T1C application does not stop here. Different modes of operation are introduced with the addition of the FeFET, which allow for toggled performance whether dealing with lower power applications or adjusting performance for prolonged waiting between refresh cycles or even maximizing the memory speed.
Until now, FeFET use in radio-frequency electronics has been non-existent. However, the FeFET shows promising results when included in the ring oscillator. Through the modulation of both drain current and gate capacitance with polarization state, tuning voltages have unique effects on the FeFET performance, introducing a wide range of observed stage delays. While most current oscillator designs have tuning ranges exceeding those shown in this chapter, the use of only the polarization to introduce such large changes in stage delay is promising and will carry over into more complex designs like those found in current oscillator literature.

Perhaps most unique of the FeFET attributes is the ability to act not only as an enhancement-mode FET but also as a depletion mode transistor. By merely varying the polarization state, the threshold voltage changes to allow operation similar to that typically reserved for more costly MOSFETs. In this manner, the FeFET is capable of finding a home in a variety of applications that would otherwise use a PMOS transistor or require additional ion implantation. Additionally, the variable threshold voltage is useful for reconfigurable circuits, where the mode of operation may change over time, such as use as a “nominally on” switch transitioning to a “nominally off” switch under specific conditions.

Ferroelectrics and piezoelectric materials are not new to the realm of sensors. However, implementation of the FeFET as the basis for performing the sensing has not yet been explored. By utilizing the piezoelectric response of the PZT layer at the FeFET gate, the transistor becomes an integrated sensor, not requiring a power source but instead periodic sampling of the polarization state. Under benign conditions these sensors can be
considered ultra-low power as the non-volatile polarization will retain the culmination of sensed phenomena for long periods of time.

The applications discussed in this chapter only begin to touch upon the benefits adding a ferroelectric layer to a transistor. Other FET structures similar to the MOSFET lend themselves to unique operation having a subthreshold swing lower than 60 mV/decade, which is the minimum for a non-ferroelectric device. Furthermore, the inherently radiation hardened nature of the device owing to the PZT addition makes the FeFET an ideal device for use in either radiated environments or simply any space application. Experiment results from the FeRAM aboard the FASTSAT show no errors during flight, demonstrating the durability of ferroelectrics in space [58, 59]. Additional functionality in a configuration such as a varactor, or simply harnessing the variability of the gate capacitance in general may yield further useful applications.
CHAPTER V

CONCLUSION

Devices containing ferroelectric materials are becoming increasingly important components in hardware designs for radiation-rich environments, low power applications, and most often memory devices. Ferroelectrics see use in a wide variety of applications due to the unique properties of the material. Though quintessentially used in memory applications to take advantage of the non-volatile storage, this class of devices is useful for most radiated environment applications resulting from the radiation-hardened nature of the material. These applications range from areas such as nuclear reactors to space, where devices incorporating ferroelectric materials have already seen use. A prime example of using ferroelectric devices for space applications is the FASTSAT experiment flown by NASA wherein no errors are observed from the results of the Ramtron ferroelectric memory circuit onboard. Promising uses in space applications is not to say the use of ferroelectrics in memory applications is diminishing. Instead, the non-volatile nature coupled with the low-power aspects of many designs makes these materials interesting for evaluation in many circuits, namely small-scale electronics or mobile applications.

While ferroelectrics have seen relatively extensive use in memory applications, the ferroelectric transistor is the topic of some research hoping to achieve subthreshold
swings larger than achievable with a MOSFET. These designs hope to harness what amounts to using the ferroelectric layer as a voltage amplifier to incite changes in drain current more rapidly than capable in MOSFETs. While the FeFETs that are the focus of this work do not have the structure used in such transistors, they still afford many interesting and useful capabilities. One of the most notable departures between the FeFETs in this work and other transistor designs is the reversal of the current hysteresis direction. Depending on the use case and circuit in which the device will operate, this has potential to be an advantage or provide different design approaches at the very least.

Historically, ferroelectrics see use in memory circuits owing to their non-volatile storage. As a result, the need for a model of the FeFET, complete with polarization retention, exists. The model presented in this work uses the structure of the FeFETs in question while capturing the time-varying nature of the ferroelectric layer polarization and, perhaps most importantly, the interaction between the polarization state and the semiconductor channel. The presented model provides a foundation for future, higher fidelity models that take into account farther reaching effects such as neighboring ion interactions, larger crystals, and finer grid resolution, all of which are adjustable. The ability to model the Radiant Technologies, Inc. developed FeFET in a circuit is also central to this work, which is shown through the accurate depiction of the transistor variations with regard to each of the three terminal voltages. Because of this, the FeFET model is used for modeling of such memory circuits as the 1T1C memory cell discussed in chapter IV or a ferroelectric non-volatile latch [47, 48, 123].

Additionally, these ferroelectric transistors have the important ability to operate at low power owing to the magnitude of the voltage required being related to the size of the
material, where the size of the material dictates the voltage needed to induce the required electric field. For this reason, ferroelectrics may be used for low power memory applications wherein a small voltage is needed to set a polarization state for a long period – spanning more 10 years or more. These FeFETs also open the gate to new operation of existing circuits such as the 1T1C memory cell or even allowing a simple 1T DRAM design. The least explored area with this family of device is radio frequency applications by far. Designs such as the ring oscillator provided in chapter IV indicate great potential for tuning the operating frequency of the circuit by way of the multiple parameters influenced by the polarization state. As a result, the ferroelectric transistor may be capable of furthering the tuning range of many current designs with minimal alteration.

The realm of integrated sensors is another area in which ferroelectric devices can shine. Though applications already use piezoelectric materials, of which ferroelectrics are a part, current circuits do not currently use ferroelectric transistors such as those discussed in this work. Compounding with the potential for low-power operation of the devices, FeFETs are a prime example of a device that can be easily used as an integrated sensor, requiring no ancillary power whatsoever.

Future work may extend in any of several directions. First, the model may be extended to new transistor structures or even different materials. Effort required for new materials is limited only to defining the physical parameters that dictate the ion interaction in the material. These parameters are typically empirically derived, as are those used in this work. Additionally, a more sophisticated ion interaction may be developed by adding the different orbital interactions between ions, which may allow calculation of parameters prior to experimental results. New structures may include
using the model to examine a structure similar to that of a MOSFET with a ferroelectric gate. This new structure would be of particular interest due to the potential for negative capacitance and therefore large subthreshold swings. Along the lines of new structures, ferroelectric capacitors may be modeled by utilizing the ferroelectric material model. This essentially represents a simplified version of the transistor where the semiconductor is replaced with a metal contact. For memory circuits, the primary future work stems from additional retention testing. Typically, retention experiments extend for long periods of time that preclude a large sample size for data points. Additionally, introducing more simplifications to the polarization model may allow retention simulations, which are valuable for memory circuit design using either ferroelectric transistors or capacitors. As new and differently sized FeFETs are fabricated by Radiant Technologies, Inc., additional retention testing and simply device characterization are needed to further validate the presented model operation against other sized transistors. The largest area for future research is radio frequency circuits. Use of the FeFET in other oscillators and designing the circuit to harness and utilize the tuning capability of the transistor is paramount to extending the device operation into this new field. Lastly, a field in which ferroelectrics are already used and may enjoy much continued usage is operating as a sensor. Piezoelectric sensors and energy harvesting see much use already, but the potential for using a FeFET as the integrated sensor, without a power source other than for sensing channel resistance, is great. As shown in this work, the FeFET possesses many interesting properties that are not widely used but can benefit a disparate array of applications.
**APPENDIX**

**MODEL PARAMETERS**

Table A.1: Model parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PZT Lattice Parameter ($\lambda$, thermal average)</td>
<td>4</td>
<td>Å</td>
</tr>
<tr>
<td>PZT Lattice Parameter (a,b)</td>
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<td>Å</td>
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<tr>
<td>PZT Lattice Parameter (c)</td>
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</tr>
<tr>
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<td>-</td>
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<td>Stencil Time Step ($\Delta t$)</td>
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<td>$\mu$C/cm$^2$</td>
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<td>g</td>
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<td>2.5E+12</td>
<td>erg/cm$^2$</td>
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<tr>
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<td>Titanium Shell Displacement Fraction</td>
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<td>erg/cm$^6$</td>
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<td>Zr-O/Ti-O $R^{12}$ Coefficient (A)</td>
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<td>1.39E-57</td>
<td>erg/cm$^6$</td>
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</table>
REFERENCES


[58] Rana Sayyah, Todd C. MacLeod, and Fat D. Ho, "Radiation-hardened electronics and ferroelectric memory for space flight systems", Ferroelectrics, vol. 413(01), pp. 170-175, 2011.


