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A physically-derived nonquasi-static model of the ferroelectric transistor for computer-aided device simulation and its application in analog circuits

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A PHYSICALLY-DERIVED NONQUASI-STATIC MODEL OF THE FERROELECTRIC TRANSISTOR FOR COMPUTER-AIDED DEVICE SIMULATION AND ITS APPLICATION IN ANALOG CIRCUITS

by

RANA M. SAYYAH

A DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
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ABSTRACT
The School of Graduate Studies
The University of Alabama in Huntsville

Degree Doctor of Philosophy College/Dept. Engineering/Electrical and Computer Engineering
Name of Candidate Rana Sayyah
Title A Physically-Derived Nonquasi-Static Model of the Ferroelectric Transistor for Computer-Aided Device Simulation and its Application in Analog Circuits

The characteristics of the ferroelectric-based common-drain, common-source, common-gate, and differential amplifiers are empirically measured and discussed. The effect of varying the input frequency and load resistance on the phase shift of the output signal, the output voltage, and the voltage gain are determined based on experimental results. Then, a physically-derived nonquasi-static model describing the behavior of the aforementioned ferroelectric amplifier configurations is presented. The model is based on the method of partitioned ferroelectric layer and is valid in accumulation, depletion, and the three inversion cases: weak, moderate, and strong. The equations of this model are based on the ferroelectric polarization equations and the standard MOSFET equations that have been modified to account for the inclusion of the ferroelectric layer. The model code is written in MATLAB® and outputs voltage plots with respect to time. For each amplifier configuration, the accuracy and effectiveness of the model are verified by a few test cases, where the modeled results are compared to empirically-derived oscilloscope plots. Lastly, the application of ferroelectric electronics in space flight systems is discussed.

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C'_F	Ferroelectric capacitance per unit area
E	Electric field
E_c	Coercive electric field
f	Frequency
I	Current
I_d	Phasor representation of drain current
I_D	Drain current
L	Channel length
N_A	Acceptor concentration
N_D	Donor concentration
P_d	Dipole polarization
P^+_d	Positive-going branch of dipole polarization loop
P^-_d	Negative-going branch of dipole polarization loop
P_{diss}	Power dissipated by the FeFET
P_r	Remnant polarization
P_s	Spontaneous polarization
P^+_{sat}	Positive-going branch of saturated polarization loop
P^-_{sat}	Negative-going branch of saturated polarization loop
q	Electronic charge
Q	Quiescent point

q'_C	Total channel charge per unit area
q'_F	Ferroelectric charge per unit area
R	Load resistance
RQ	Equivalent resistance
t	Time
t_f	Ferroelectric thickness
t_g	Gate thickness
V	Voltage
v_{bs}	Substrate-to-source voltage
V_{bs}	Phasor representation of substrate-to-source voltage
v_{cb}	Channel-to-substrate voltage
V_{cb}	Phasor representation of channel-to-substrate voltage
v_{db}	Drain-to-substrate voltage
V_{db}	Phasor representation of drain-to-substrate voltage
V_{DD}	Drain-to-ground voltage
v_{ds}	Drain-to-source voltage
V_{ds}	Phasor representation of drain-to-source voltage
V_{DS}	DC component of drain-to-source voltage
V_{FB}	Flat-band voltage
v_{gb}	Gate-to-substrate voltage
V_{gb}	Phasor representation of gate-to-substrate voltage
v_{gs}	Gate-to-source voltage
V_{gs}	Phasor representation of gate-to-source voltage

V_{GS}	DC component of gate-to-source voltage
V_p	Polarization voltage
$V_{p,neg}$	Negative polarization voltage
$V_{p,pos}$	Positive polarization voltage
v_{sb}	Source-to-substrate voltage
V_{sb}	Phasor representation of source-to-substrate voltage
V_{SB}	DC component of source-to-substrate voltage
V_T	Threshold voltage
W	Channel width
x	Channel position
γ	Body effect coefficient
ε_i	Permittivity of indium oxide
θ	Phase angle
μ	Surface mobility
ϕ_F	Fermi potential
ϕ_{MS}	Metal-semiconductor work function
ϕ_t	Thermal voltage
ψ_F	Ferroelectric potential
ψ_s	Surface potential
ψ_{s0}	Surface potential at the source
ψ_{sL}	Surface potential at the drain
ω	Angular frequency

CHAPTER I

INTRODUCTION AND BACKGROUND MATERIAL

For many years, the metal-oxide-semiconductor field-effect-transistor (MOSFET) has been the most extensively used electronic element in the design and fabrication of integrated circuits (ICs) [1]. However, the constantly growing field of space exploration has led to a high demand for electronics that perform properly and reliably in radiation environments. Due to the MOSFET's inconsistent and undependable functionality in these environments, the ferroelectric field-effect-transistor (FeFET) and its use in many aspects of electronics has garnered growing interest. Along with the properties of reversible, spontaneous polarization and nonlinearity, ferroelectric materials are also characterized by radiation tolerance. Thus, the inclusion of a ferroelectric layer in the MOSFET structure results in a radiation-hardened transistor with unique features. Besides space flight systems, the FeFET has the potential to be applied in analog and digital ICs; however, only the FeFET's use in memory elements has been extensively researched. In order to lay the groundwork for the different applications of the FeFET, this transistor's behavior in the basic analog circuits must first be studied. This dissertation examines the FeFET-based common-drain (CD), common-source (CS), common-gate (CG), and differential amplifier configurations and presents a physics-based model that simulates the behavior of these FeFET amplifiers. The model

developed in this work is based on the concept of partitioning the ferroelectric layer [2] and modifies the standard MOSFET equations [3] to account for the inclusion of the ferroelectric layer. The model has been found to be both physically and empirically accurate and valid in accumulation, depletion, and weak, moderate, and strong inversion. Lastly, a short discussion of the application of FeFET-based memory elements in space flight systems is presented.

A. Motivation for this Work

Although the FeFET has been known for many years, the physics underlying FeFET operation has not been extensively studied. In fact, most of the research conducted on the FeFET has been on its performance as a memory element [4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17]. This dissertation seeks to fill in the information gaps regarding the FeFET and its application in the basic analog circuit configurations. As part of the initial phase of this research, the results of which are presented in the author's thesis [18], a quasi-static mathematical model of the FeFET was developed. That model's drain current equations were based on the Fermi-Dirac equation in order to reproduce the proper hysteretic shape of the FeFET's drain current vs. gate-to-source voltage (I-V) characteristics. Although the modeled results were empirically accurate, the model's equations did not reflect the physics governing the FeFET's operation. Therefore, a physics-based, nonquasi-static (NQS) model was created to describe the FeFET and was then implemented in MATLAB® to facilitate computer-aided device simulations. This model was then used to simulate the FeFET-based CD, CS, CG, and differential amplifier circuits. It is of great importance to understand and model the behavior of the FeFET-based amplifier configurations since they lay the foundation for further study in the areas

of both analog and digital circuit design. Understanding the FeFET and the behavior of the fundamental analog circuits built using this transistor is the first step towards establishing the basic knowledge of the field of ferroelectric electronics. Furthermore, with an efficient, user-friendly, physically-derived NQS model available, numerous FeFET-based circuits can easily be designed, simulated, and accurately studied.

B. Applications of Ferroelectrics in Radiation-Hardened Electronics and Space Flight Systems

Over the past few years, there has been an increasing interest in the exploration of space beyond Low Earth orbit. Radiation is a major concern for Low Earth orbit space flight systems since the radiation environment in Low Earth orbit is much harsher than at Earth's surface. Thus, the need for radiation-hardened electronics is undeniable. These electronics need to be radiation tolerant, low power, and reliable. Therefore, the National Aeronautics and Space Administration (NASA) is carrying out the Advanced Avionics and Processor Systems (AAPS) project in order to develop high-tolerant, radiation-hardened electronics and processors. As part of the AAPS project, research is being carried out on the use of ferroelectric materials in the creation of radiation-tolerant electronics and memory elements. Ferroelectric materials are inherently radiation hardened and are thus a leading contender in the field of radiation-hardened memory devices, as well as analog and digital circuits. Memory devices in particular can benefit from the use of ferroelectric materials, as memory elements are highly susceptible to the damaging effects of radiation.

a. The Space Radiation Environment

A key distinguishing feature of the space environment is the existence of radiation. The space radiation environment is composed mainly of the Van Allen belts, which are divided into the trapped proton belt and the trapped electron belt, as shown in Figure 1.1. The proton belt is the inner radiation belt, while the electron belt is the outer radiation belt. Due to the non-alignment of the magnetic and rotational axes of the Earth, the magnetic field at the south magnetic pole is weaker than at the north magnetic pole. The weakness of the magnetic field enables the proton belt to come close to Earth's surface, and it is closest in the South Atlantic region known as the South Atlantic Anomaly (SAA) [19]. Satellites traveling in the SAA experience a flux of 3000 particles per square centimeter per second, which is hazardous to space flight systems [19].

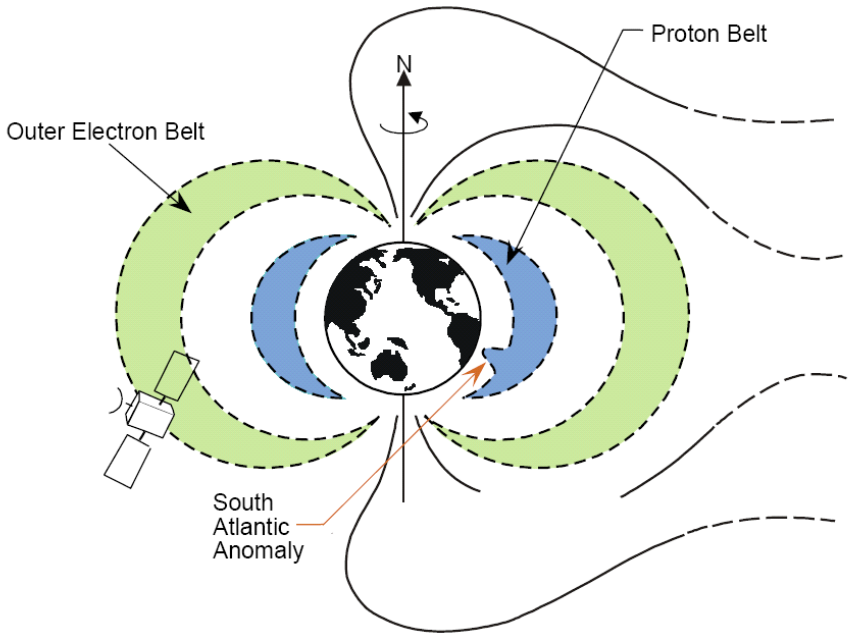

Figure 1.1 The Van Allen belts [20]

b. Effects of Radiation on Electronic Devices

High-energy trapped particles can have multiple adverse effects on electronic devices. One of the gradual damaging effects of exposure to radiation is an increase in the device's total ionizing dose (TID), which is the amount of energy in the device due to the ionization of protons and electrons [21]. An increased TID can cause leakage current, timing skews, and other electronic failures [21]. Moreover, radiation exposure can cause abrupt changes in the electronic devices. These damaging changes are collectively known as Single-Event Effects (SEEs) and occur when the trapped particles ionize with nearby atoms and generate charge. When a single ion interaction occurs, the state of memory or values of register bits can be changed, causing a Single-Even Upset (SEU). A Single-Event Latch-up (SEL) occurs when a high-energy particle forces a latched state, which can cause too much current to flow through the circuit and permanently damage the device. When a false signal propagates through the circuit due to charge generated by ionization, a Single-Event Transient (SET) occurs. In power MOSFETs, ionization can induce high current through the device if the breakdown voltage is exceeded. This damaging effect is known as a Single-Event Induced Burnout (SEB). Also, in power MOSFETs with a high gate voltage, if a heavy ion hits the gate, it can cause a short through the oxide and destroy the device. This event is the Single-Event Gate Rupture (SEGR) [22]. Clearly, high-energy particles in the radiation belts are a major concern for the safety and functionality of electronic devices in space.

When a semiconductor is exposed to radiation, electron-hole pairs can be generated in the oxide layer of the MOSFET. The electron-hole pairs are created when an electron is excited from the valence band to the conduction band, leaving behind a

hole in the valence band. However, only a small fraction of the free electrons and holes recombine immediately, while the majority of the electrons and holes drift and diffuse in the device. These free electrons and holes eventually recombine or are trapped. If an electric field is present in the depletion region of the transistor, electron-hole pairs that are created in the oxide layer are quickly separated by the field. Due to the electrons' higher mobility, the electrons quickly drift away, but the slow holes are trapped in the crystalline flaws of the oxide. These trapped oxide holes, shown in Figure 1.2, are a source of trapped positive charge in the oxide layer, which produces a negative shift in the threshold voltage of the MOSFET. Threshold voltage shifts adversely affect the device's speed and power consumption [23]. It is apparent that radiation-hardened electronics are necessary for proper and efficient electronic operation in radiation environments.

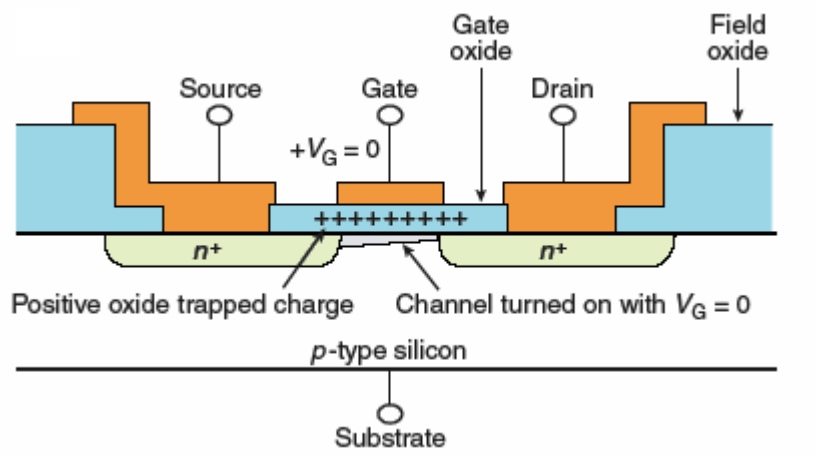

Figure 1.2 Effect of radiation on a MOSFET [23]

Besides digital and analog circuits, memory elements are also easily damaged by radiation. Indeed, memory cells are much more vulnerable to radiation damage. In particular, static random access memory (SRAM) and dynamic RAM (DRAM) cells

experience SEU due to radiation [23]. The equivalent circuit of an SRAM cell is shown in Figure 1.3. An SRAM cell is composed of four NMOS and two PMOS transistors. The cell consists of a latch created by two cross-coupled inverters [23, 24]. The latch eliminates the need for refresh operations. The remaining two NMOS transistors are control elements [4]. An SEU in an SRAM results from an ion strike on the drains of the four transistors that make up the inverters of the memory cell. A state change occurs and remains until the next write to the cell if the pulse of the ion strike's voltage is faster than the feedback loop between the inverters [23]. A DRAM cell is composed of a capacitor for data storage and a transistor to access the capacitor, as shown in Figure 1.4 [24]. Ion strikes cause SEU in DRAMs by creating cell storage and bit line errors. A cell storage error occurs when an ion strike alters the state of the storage data when the radiation strikes near the transistor of the DRAM cell and causes a spike in the charge [25]. It should be mentioned that only the state "1" is susceptible to SEU, not the state "0." An ion strike can disturb the pre-charged bit line, resulting in a bit line error [23]. Figure 1.4 shows the effect of a radiation strike on a DRAM cell. The damaging effects of radiation on memory cells can be mitigated by using ferroelectric materials in the memory elements.

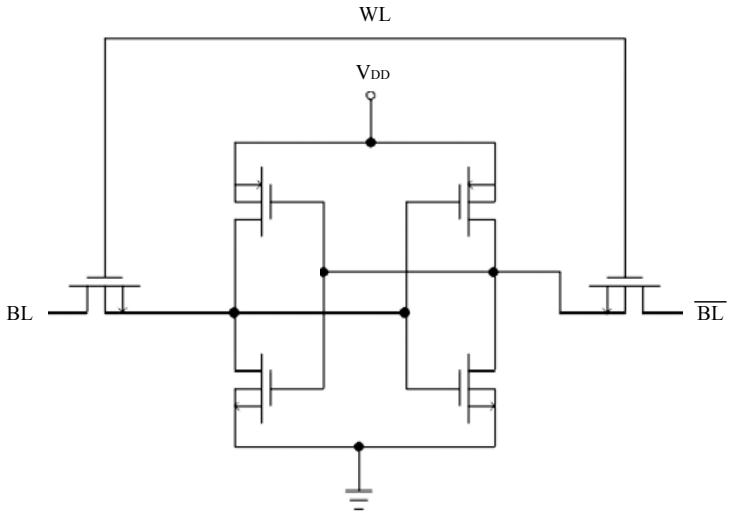

Figure 1.3 Circuit configuration of an SRAM cell [4]

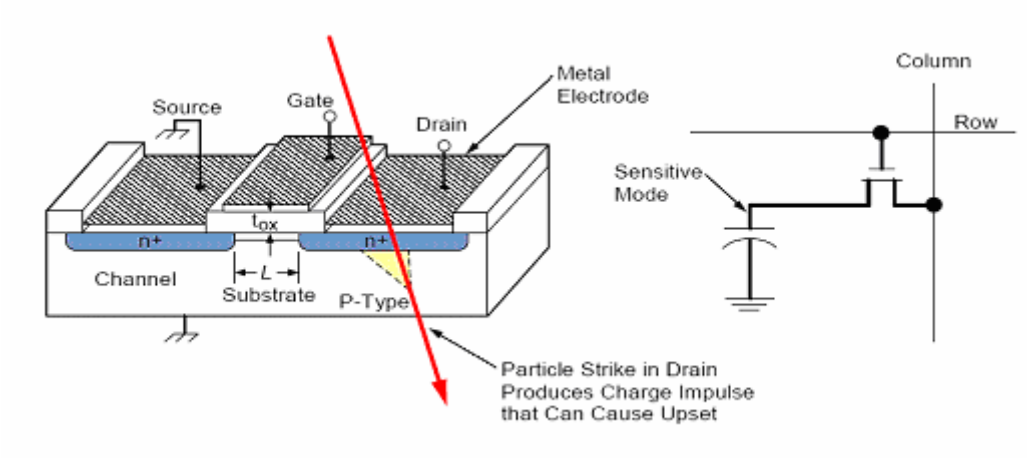

Figure 1.4 Effect of radiation on a DRAM cell and circuit configuration of a DRAM cell [20]

c. Advantages of Ferroelectric Materials

NASA's AAPS project is subdivided into multiple tasks, including Radiation-Hardened Volatile and Nonvolatile Memory. As part of this subtask, research is being carried out on the use of ferroelectric materials in memory. Ferroelectric materials possess several characteristics that distinguish them as viable candidates for radiation-hardened electronics and memory elements. Ferroelectric materials have been found to

have a high degree of radiation hardness, are nonvolatile, and are easily reconfigurable [26]. Moreover, ferroelectrics have a very low coercive field, a high remnant polarization, and good mechanical strength [26]. When used in memory devices, ferroelectric materials provide radiation-hardened, nonvolatile memory that is dense, low power, high speed, and high endurance [27].

Ferroelectric RAM (FRAM) has been found to counter the problems in the standard SRAM. Due to the high risk of data corruption in SRAM devices in radiation environments, the memory elements are built with three memory banks and require constant reading of each memory location and rewriting of errors [4]. This process utilizes triple module redundancy (TMR), where three systems exist to perform a function and a voting system produces a single output [25]. TMR leads to extra time, weight, power consumption, and complexity [4, 27]. Using FRAM memory cells eliminates the need for TMR, thereby mitigating the problems associated with this method.

d. The FASTSAT Satellite Memory Test Experiment

To verify the behavior of ferroelectric materials in space environments, an FRAM device will be placed on a satellite bus as part of the Memory Test Experiment. The satellite bus is the Fast and Affordable Science and Technology Satellite (FASTSAT). As its name suggests, the FASTSAT satellite is a low-cost, high-capability satellite developed by NASA for the purpose of providing a bus for numerous and varied payloads. An off-the-shelf 512K Ramtron FRAM will be placed on the FASTSAT bus without affecting the operation of any of the satellite's payloads. Specifically, the FM24C512 ferroelectric nonvolatile RAM is designed as 2^{16}x8 bits. The Memory Test

Experiment procedure is as follows. The flight computer generates a random number at each power-up and sends it to the communications board. The first eight bits of that number are stored in each memory cell of the FRAM. Then, every six minutes, a microcontroller located on the communications board reads each memory cell and compares its contents with the reference pattern. Any error found is recorded, along with the address of the memory cell where the error was found and a timestamp. This data is then transmitted to ground within twenty-four hours and will be analyzed in order to categorize the types of errors found. The following categories of errors are distinguished: error in writing to memory, error in reading from memory, change of state of a memory cell, and permanent pinned state of a memory cell. Besides identifying the type of error, the satellite's location will be calculated and the position of the memory cell on the chip will be noted. The location of the satellite is of importance since it indicates the radiation environment at the time of the error. The memory cell's on-chip position will help in identifying error clustering [25]. All this data will be invaluable in empirically determining the effect of radiation on ferroelectric materials and their behavior and efficiency in radiation environments.

e. Conclusion

It is clear that the field of ferroelectric-based electronics is large and far-reaching. The unique properties of ferroelectric materials distinguish them as materials that have the potential to mitigate some of the prevalent shortcomings of current electronic materials. Moreover, it is probable that ferroelectric materials will enable the proper functionality of many technologies in extreme environments.

C. FeFET Theory of Operation

The FeFET properties and theory of operation were explained in detail in the author's thesis [18], but the basic principles are included here for completeness. The FeFET is created by inserting a layer of ferroelectric material below the gate (or dielectric layer if it exists) and above the semiconductor substrate in the standard MOSFET structure. A schematic diagram of the standard n-channel FeFET is shown in Figure 1.5. The FeFET can be in one of two states: on or off. When the gate of an n-channel FeFET is positively poled, i.e., a positive gate-to-source voltage (V_{GS}) is applied at the gate and then removed, the FeFET is in the off state. When the gate is negatively poled, the FeFET is in the on state. The inclusion of the ferroelectric layer manifests unique ferroelectric properties, including partial polarization, spontaneous and reversible polarization at the device-specific Curie temperature, hysteretic I-V curves, and logarithmic drain current decay when the gate voltage is off. Ferroelectric polarization is spontaneous since at the Curie temperature, the ferroelectric material's crystal structure is transformed from the nonpolar to the polar state [28]. The reversibility of the ferroelectric polarization is due to the fact that the application of an electric field reverses the direction of polarization. Thus, simply inserting a layer of ferroelectric material in the basic MOSFET yields a different electronic device with unique characteristics.

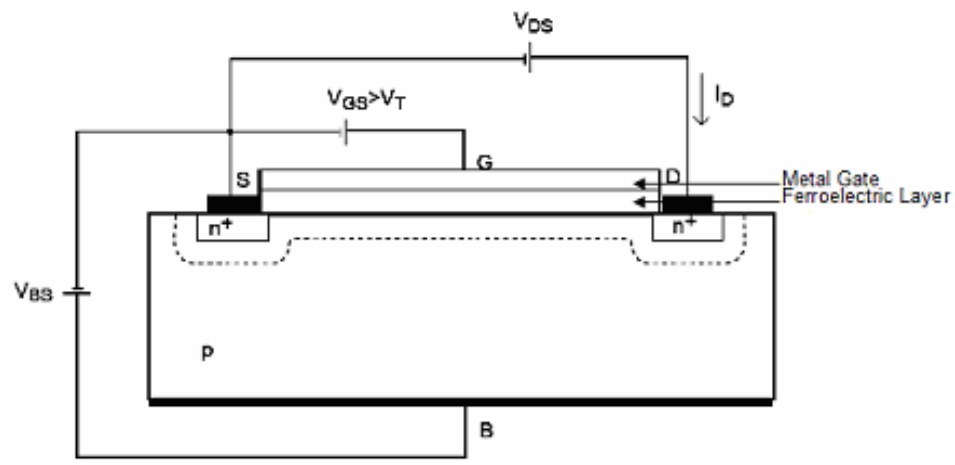

Figure 1.5 Schematic diagram of an n-channel FeFET [29]

D. Characterization of the FeFET

Before studying the FeFET-based analog circuits, the transistor must first be characterized. The FeFETs used in this study were 4x400μm n-channel thin-film lead zirconate titanate (PZT), i.e., the channel length, L, was 4μm and channel width, W, was 400μm, and were provided by Radiant Technologies Incorporated of Albuquerque, New Mexico. The gate was 1500Å-thick platinum with 1Ω/□ conductivity, the source and drain were each 1000Å-thick platinum with 1.5Ω/□ conductivity, the ferroelectric material was 3500Å of 20/80 PZT, and the semiconductor was 200Å-thick indium oxide. The substrate doping concentration, N_A, was 10^{19} cm^{-3}, and the surface mobility, μ, was approximated at 1250cm^2/V·sec. The remnant polarization, P_r, was 15μC/cm^2, and P_r was assumed to be 0.8 times the spontaneous polarization P_s. The coercive electric field was calculated by the coercive voltage, which was assumed 2.25V, divided by the thickness of the ferroelectric layer. Figure 1.6 shows an n-channel FeFET with some of the physical parameters described above, where N_D is the source/drain doping concentration, t_g is the gate thickness, and t_f is the ferroelectric thickness.

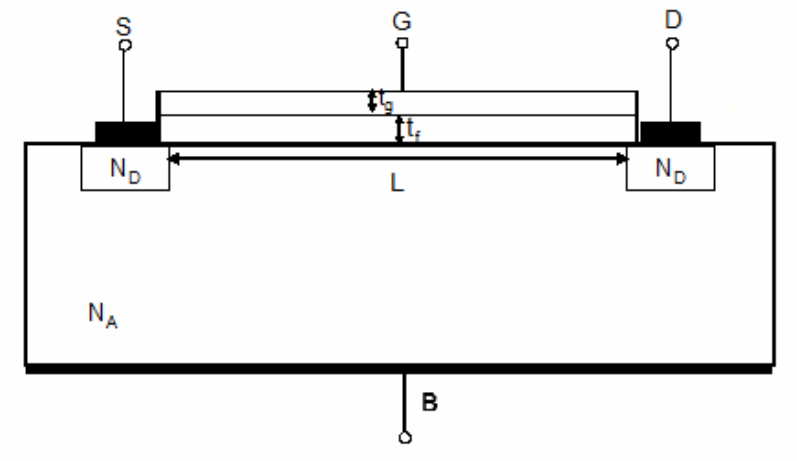

Figure 1.6 An n-channel FeFET with some physical parameters shown

Empirical characterization of the FeFET was carried out and the results presented in the author's thesis [18]. For this work, the modeled characterization of the FeFET is discussed. The first step in creating an accurate empirically-based model is to reproduce the hysteretic I-V plots of the FeFET for the gate voltage on and off cases, which are known as the active and remnant polarization plots, respectively. Based on the equations used to create the model presented in this dissertation, which are described in detail in the next chapter, the following two I-V plots were produced. Figure 1.7 shows the active polarization plot, and Figure 1.8 is the remnant polarization plot. As can be seen from the plots, the modeled characterization was carried out for three values of the drain-to-source voltage (V_{DS}), and as expected, the drain current increases with an increase in V_{DS}. Comparing this model's output plots with those produced by other models [2, 30, 31] proves the accuracy of this model. With the proper characterization of the FeFET, the model can be effectively used to simulate any FeFET-based circuit.

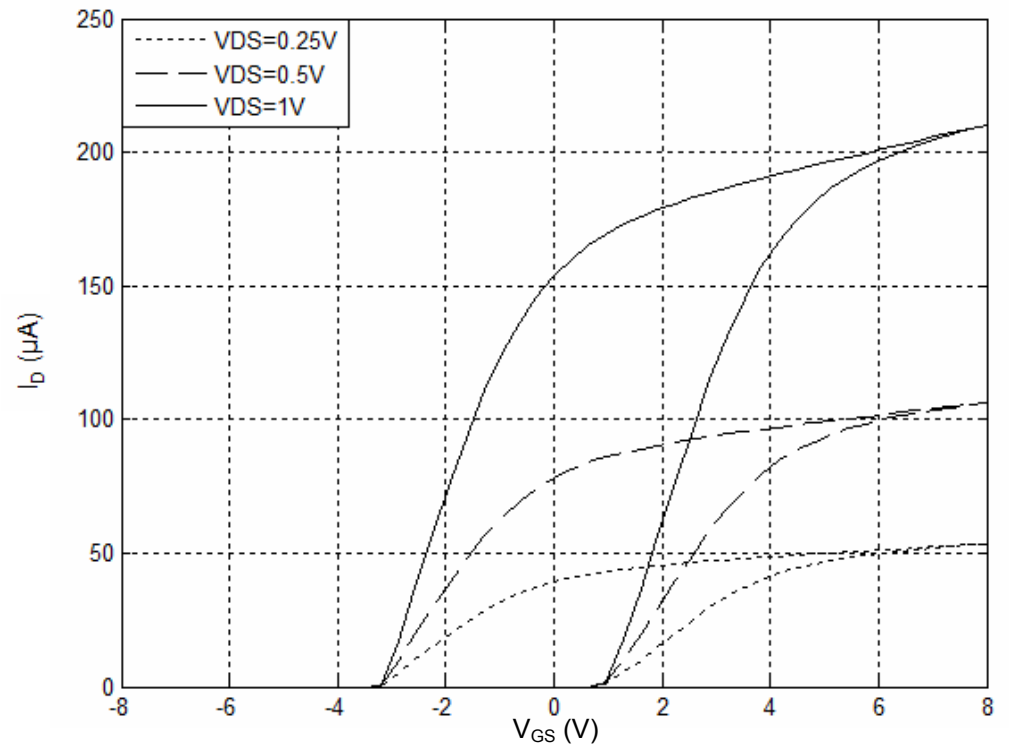

Figure 1.7 Modeled FeFET active hysteresis plot for three values of V_{DS}

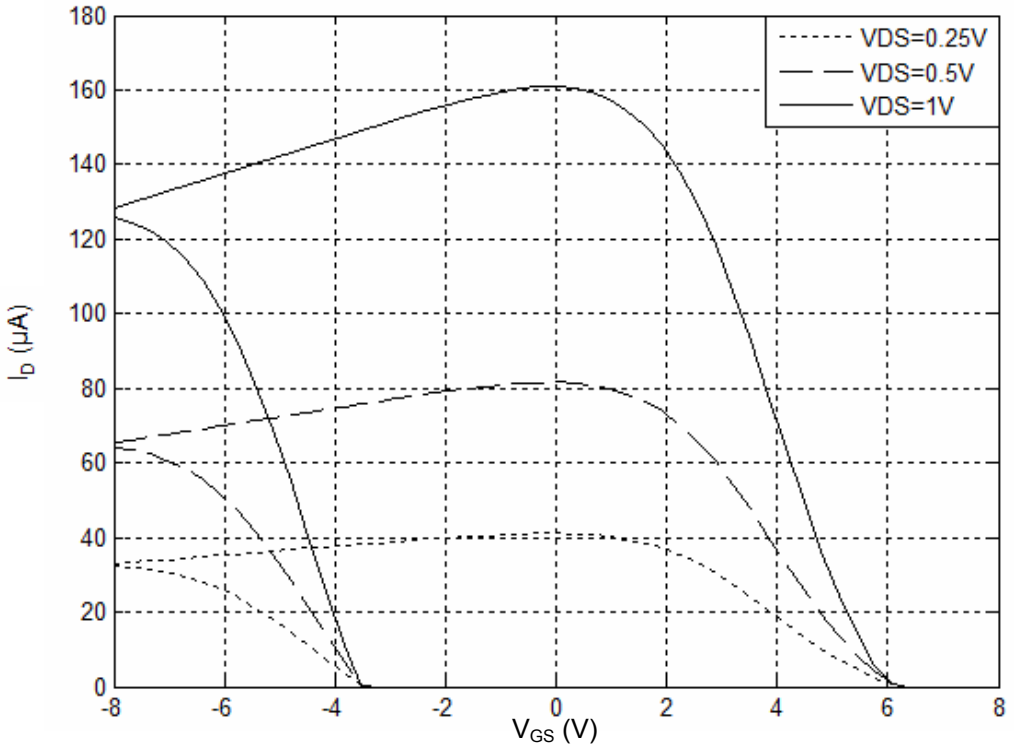

Figure 1.8 Modeled FeFET remnant hysteresis plot for three values of V_{DS}

E. Literature Review

The property of ferroelectricity and its use in memory devices has been extensively researched [4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17]; however, the application of ferroelectric transistors in analog circuits has hardly been explored. Furthermore, no physically-derived, empirically-based NQS model has been created to simulate the behavior of ferroelectric-based analog circuits. Three ferroelectric polycrystals are modeled in [32] using a micromechanical crystal plasticity model. Driga et al. [33] present a model using the finite element method and the boundary element method to describe the transient behavior of the electric fields in ferroelectric polymers. In [34], several ferroelectric micro-electromechanical models are reviewed and discussed. Six behavioral models for ferroelectric capacitors as applied to nonvolatile memories are surveyed in [35]; however, these behavioral models do not reflect the physics underlying ferroelectric capacitor operation, rather they empirically model the behavior of the ferroelectric capacitors as they are observed. Rate-independent models treating multi-axial behavior of ferroelectric materials are examined in [36]. A quasi-static model describing the operation of the ferroelectric transistor that is based on the charge-sheet model has been developed by Miller et al. [31, 37, 38]. Chai et al. [39] extend the work by Miller et al. [37] to include the actual local electric field rather than a macroscopic experimentally averaged field. Massoud [40] has created an electrostatic model of the FeFET in order to describe the capacitance-voltage characteristics of this transistor. The ferroelectric dipole distribution function is used in [41, 42] to model ferroelectric polarization. Jiang et al. [43] have proposed an empirical/numerical parallel-elements model. A mathematical model based on the quantification of the ferroelectric material's

domain wall energy is presented in [44, 45]. A compact model that is based on the Preisach theory that includes temperature and dynamic behavior of the FeFET has also been developed [46]. Ando et al. [47] use the Preisach theory to model and characterize ferroelectric devices operating in the quasi-static region. Meyer et al. [48] develop another compact model based on the Preisach theory to describe the ferroelectric polarization and electric field relationship. Despite the relatively large number of papers published on the application of the Preisach theory to ferroelectric characterization, this theory is mathematically too complicated to be effectively applied to ferroelectric circuits. Bailey and Ho [2] have created a quasi-static model that is based on the concept of partitioning the ferroelectric layer. MacLeod and Ho [49] have modified Bailey's model to account for nano-scale effects. A self-consistent quasi-static model has also been developed [50]. However, all these models were created to describe the behavior of the FeFET as an independent device. Some papers [51, 52, 53, 54] have been written on the use of FeFETs in digital circuits, but in the field of ferroelectric analog circuitry, very little data has been published. MacLeod and Ho [55] have built a FeFET-based CD amplifier and obtained experimental results, while Phillips et al. [56] have done the same for a FeFET-based differential amplifier. The author, Hunt, MacLeod, and Ho have published papers [57, 58, 59, 60] characterizing and mathematically modeling the FeFET-based CD and CS amplifiers, but even though the model created for these papers is empirically accurate and the first to simulate the behavior of ferroelectric amplifiers, it is not physically derived. Thus, despite the existence of multiple models that describe the FeFET, no NQS, physics-based model that is easily implemented in MATLAB® for computer-aided device simulation has been developed to model the FeFET. It is the aim

of this work to empirically characterize the FeFET-based CD, CS, CG, and differential amplifiers and to present an NQS model that simulates the behavior of these ferroelectric amplifiers in MATLAB®.

F. Scope of Work

This dissertation devotes a chapter to each of the FeFET amplifier types studied. Specifically, Chapter II characterizes and models the FeFET CD amplifier. Chapter III examines the basic characteristics of the FeFET CS amplifier and models it. The FeFET CG amplifier and its model are studied in Chapter IV. Chapter V details the FeFET differential amplifier data and its model. Finally, Chapter VI presents a summary and conclusion of the research.

CHAPTER II

CHARACTERIZATION AND MODELING OF THE FeFET COMMON-DRAIN AMPLIFIER

Analog circuit design is the building block of electronics, and the amplifier is, in turn, the basis of analog circuitry. It is therefore imperative to the study of ferroelectric electronics to develop a solid foundation of the operation of the standard FeFET-based amplifier circuits. Characteristics of the FeFET CD amplifier based on experimentally-derived data were determined. Furthermore, a physically-derived NQS model that is valid in accumulation, depletion, and all three inversion cases was developed and tested. The model's accuracy is verified by comparing the modeled results with empirical outputs. It is important to note that this model is the first FeFET model that is both NQS and physically and empirically accurate. The portion of this chapter relating the basic characteristics of the FeFET CD amplifier and the experimental results has been adapted from the author's thesis [18] and is included here for completeness.

A. Basic Structure

A FeFET CD amplifier, also known as a source follower, is built using a FeFET and a resistor. Figure 2.1 illustrates the FeFET CD amplifier circuit configuration. As can be seen from the figure, the load resistor, R, is connected to the source of the FeFET. The input voltage, which includes ac (v_{in}) and dc (V_{offset}) components, is provided from

the gate of the transistor to ground. V_{DD} is the voltage from the drain of the FeFET to ground. The output voltage, v_{out}, is measured at the source of the transistor and above the resistor.

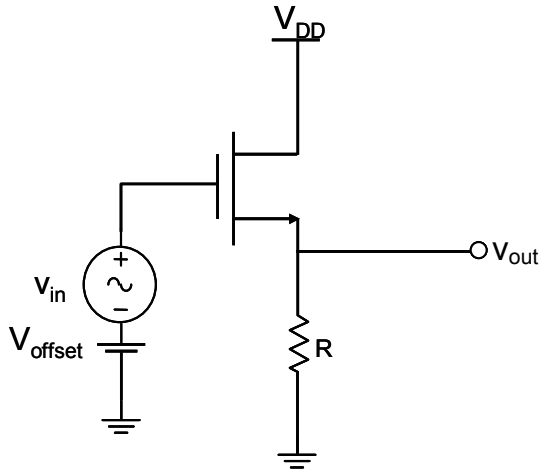

Figure 2.1 FeFET common-drain amplifier circuit configuration

B. Empirical Measurements of the FeFET CD Amplifier

After building the FeFET CD amplifier based on the configuration shown in Figure 2.1, measurements were carried out for this amplifier. The relationship between the frequency of the input signal and each of the phase shift of the output signal, output voltage, and voltage gain was examined. Also analyzed was the effect of load resistance on each of these three output parameters. Since the FeFET CD amplifier was the first circuit configuration tested, values for V_{DD} never exceeded 1V because of the fear of burning the transistor. As the tolerance of the transistors was determined, higher V_{DD} values were used, as will be seen with the CS, CG, and differential amplifiers.

a. Effect of Frequency on Phase Shift, Output Voltage, and Voltage Gain

The first parameter examined was the frequency of the input signal. Specifically, the effect of input frequency on the phase shift and peak voltage of the output signal and the voltage gain of the amplifier was analyzed. Using a function generator to adjust the frequency of the input signal, the input frequency was varied from 500 to 2100Hz in increments of 100Hz. The phase shift in degrees was plotted against the logarithm of frequency, with V_{DD} set to 0.5V and the resistor to 1MΩ, for three different values of the amplitude of v_{in}, denoted by V_{in}: 3V, 4V, and 6V, as shown in Figure 2.2. (Note that all logarithms in these measurements are of base 10.)

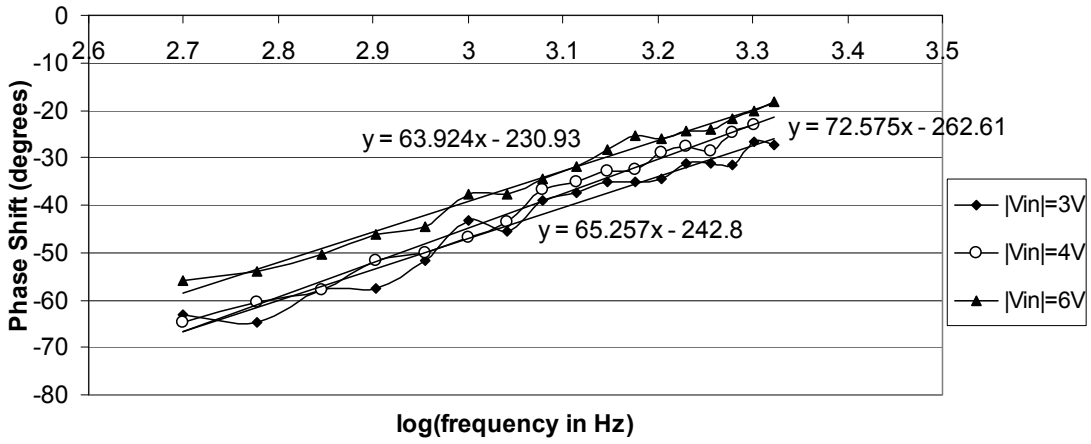

Figure 2.2 Plot of phase shift vs. logarithm of frequency for three values of V_{in}

This plot depicts several important characteristics. First, the negative values of phase shift indicate that, for the specified values of frequency, input voltage, and resistance, the output signal lags the input signal. It must be noted that the output signal does not always lag the input signal, as will be shown later. Also, all the data sets display a linear trend, and the data points tend to more closely follow their corresponding trend

line as the input voltage increases. Thus, increasing the input voltage leads to more consistent data in phase shift analysis.

The effect of input frequency on the output voltage was also measured and plotted. Figure 2.3 displays the results for V_{in} values of 3, 4 and 6V, which were obtained for frequencies ranging from 500 to 2100Hz in 100Hz increments, and where V_{DD} was again 0.5V and the resistor was set to 1MΩ.

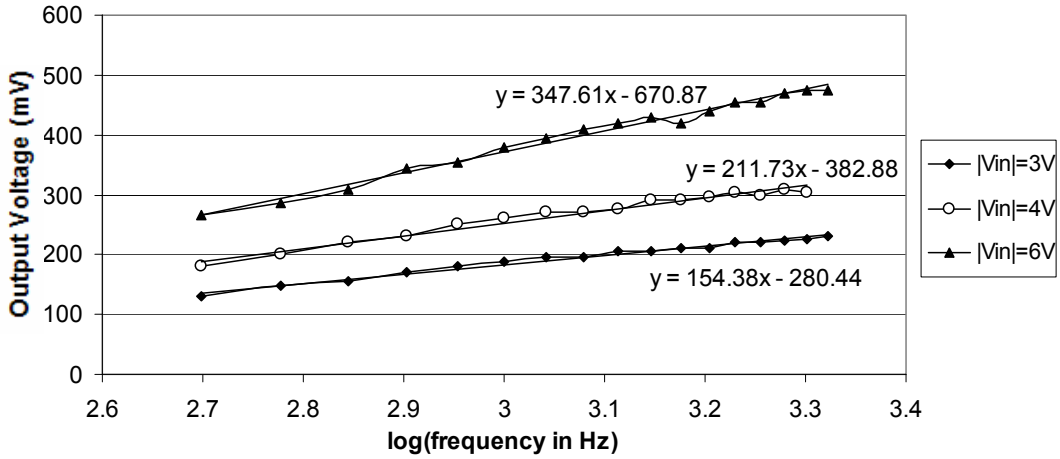

Figure 2.3 Plot of output voltage vs. logarithm of frequency for three values of V_{in}

From this plot, it can be seen that there is a distinctly linear relationship between the logarithm of frequency and the output voltage. Each of the three data sets very closely follows its respective trend line, whose equation is shown on the plot. It is also noticed that for all frequencies, as the value of the input voltage increases, the value of the output voltage also increases. Overall, output voltage has an almost completely linear relationship with the logarithm of frequency.

Finally, frequency's effect on the voltage gain was examined. Keeping V_{DD} at 0.5V and the resistor at 1MΩ, the frequency was again varied from 500 to 2100Hz at

increments of 100Hz for the same three values of V_{in} as before. Then the voltage gain was calculated and plotted. The voltage gain was determined by dividing the output voltage at each value of frequency by the amplitude of the input voltage for each of the three input voltage values tested. The plot of Figure 2.4 shows the voltage gain vs. the logarithm of frequency.

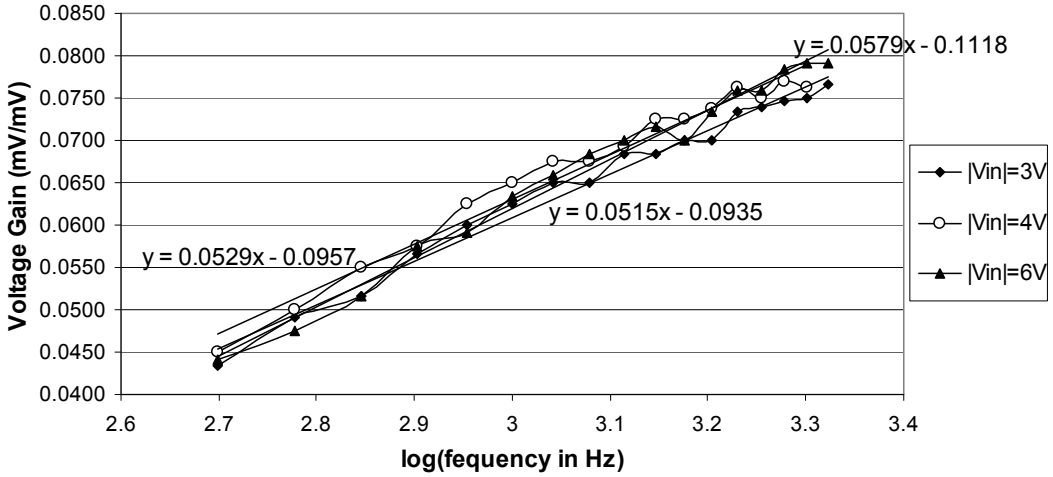

Figure 2.4 Plot of voltage gain vs. logarithm of frequency for three values of V_{in}

The above plot also displays a linear trend, and all three trend lines are very close to each other and sometimes overlap. Moreover, the voltage gains for all the data sets can be estimated by almost the same linear trend line since the equations of the three trend lines are very similar and have nearly the same slope and y-intercepts.

b. Effect of Load Resistance on Phase Shift, Output Voltage, and Voltage Gain

The effect of varying the value of the resistor R of the CD amplifier configuration shown in Figure 2.1 was also examined. It was noted that changing the resistance altered the phase shift of the output signal, the output voltage, and the voltage gain of the amplifier. However, the relationship between the logarithm of the resistance value and

each of the aforementioned three parameters was drastically different from the relationship between the logarithm of frequency and the three output parameters, as will be seen from the plots.

The first parameter measured was the phase shift of the output signal. The resistance values tested ranged from 35kΩ to 9MΩ. V_{in} was set to 2V and V_{DD} was set to 0.7V. Measurements were taken at five different frequencies, which were 100Hz, 1kHz, 10kHz, 100kHz, and 1MHz. One more variable was added to this analysis: the polarization voltage, V_p. This voltage was added to ensure that the FeFET was operating in saturation since operation outside the saturation region involved dependence on previous values, which could affect the accuracy of the data collected. The inclusion of V_p was necessary to guarantee operation in the saturation region since with V_{in} = 2V and the amplitude of the gate-to-source voltage V_{GS}, which is given by $V_{GS} = V_{in} - V_{out}$, where V_{out} is the amplitude of the output signal, V_{GS} is too low to guarantee operation in the saturation region. Two values of V_p were used in the FeFET CD amplifier research, +8V and -8V. The following two plots show the phase shift vs. the logarithm of the resistance values for each value of V_p.

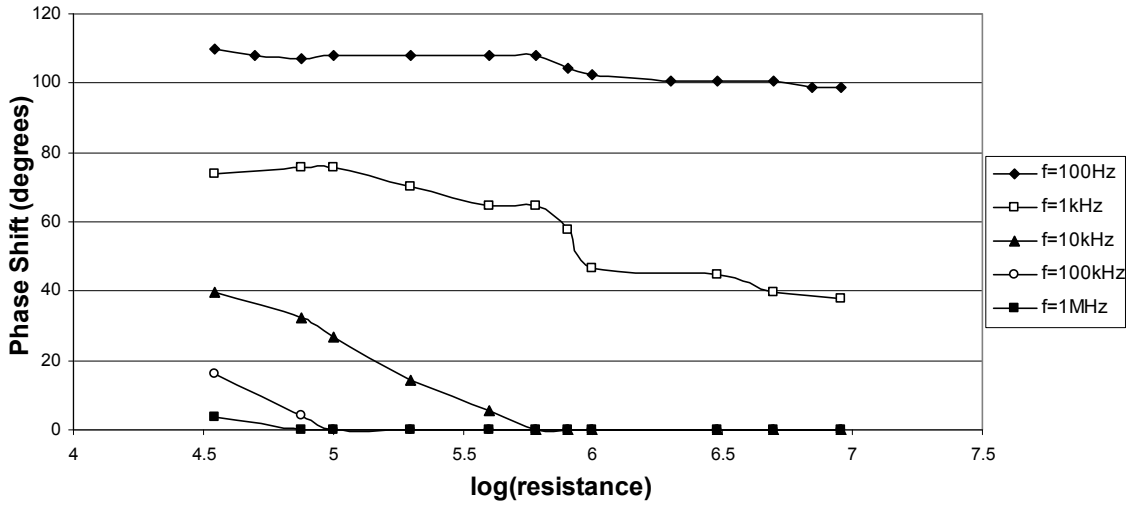

Figure 2.5 Plot of phase shift vs. logarithm of resistance for five input frequencies for negative polarization voltage

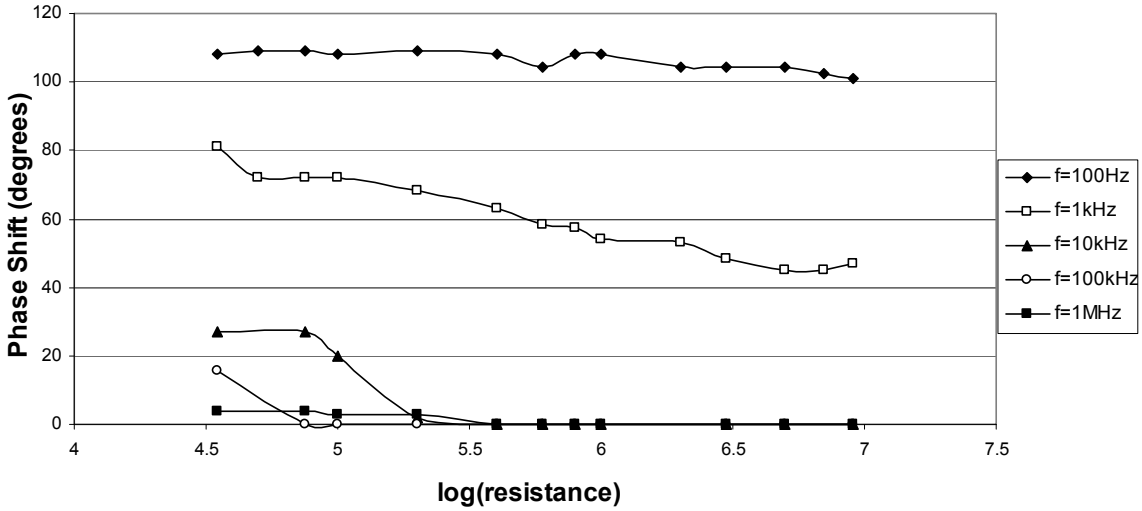

Figure 2.6 Plot of phase shift vs. logarithm of resistance for five input frequencies for positive polarization voltage

The first noticeable characteristic of these two plots is the fact that the output signal leads or is in phase with the input signal since the phase shift is nonnegative. Also, the phase shift decreases with increasing frequency. For the 10kHz, 100kHz, and 1MHz

frequencies, the output signal is in phase with the input signal for resistor values higher than 600kΩ for V_p = -8V and higher than 400kΩ for V_p = +8V. For a frequency of 100Hz, both plots show an almost horizontal line, while the 1kHz data set on each plot has a negative slope. The data sets for the three highest frequencies decrease to zero in both plots. Therefore, the lowest frequency data set displays a horizontally linear relationship between logarithm of resistance and the phase shift of the output signal.

The next parameter studied was the output voltage. Data was collected for the same resistor values and the same five frequencies as before, and V_{in} and V_{DD} remained unchanged. The plots for output voltage vs. the logarithm of resistance for the negative and positive values of V_p are given in Figures 2.7 and 2.8, respectively.

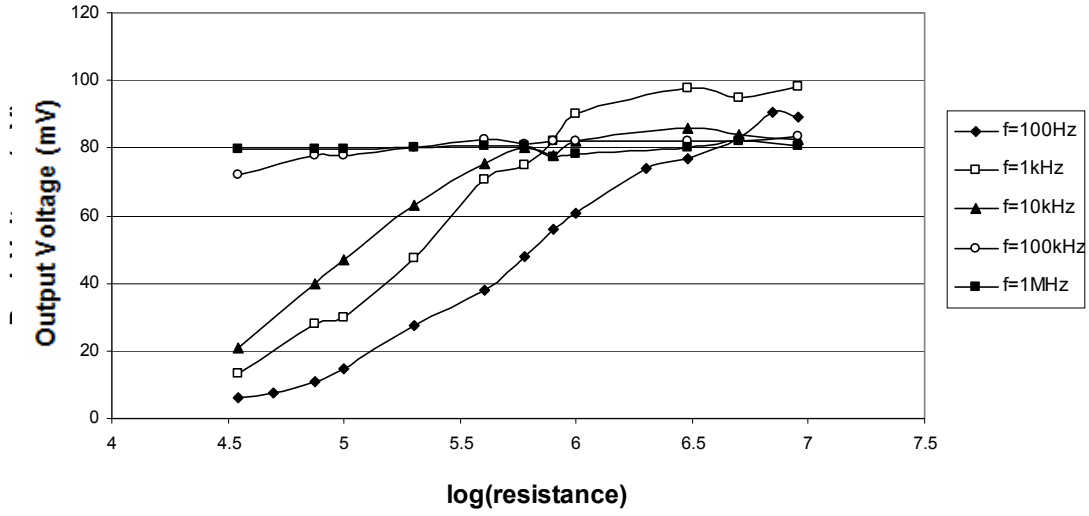

Figure 2.7 Plot of output voltage vs. logarithm of resistance for five input frequencies for negative polarization voltage

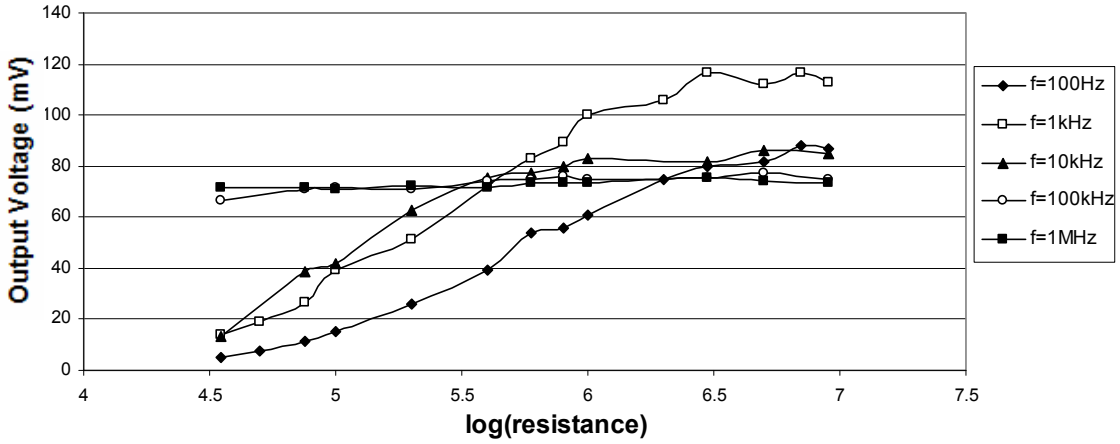

Figure 2.8 Plot of output voltage vs. logarithm of resistance for five input frequencies for positive polarization voltage

Comparing the two previous plots, it is observed that for both values of $V_{p,}$ the data sets for the frequencies of 100Hz, 1kHz, and 10kHz have a similar trend and slope, while the data sets for the frequencies of 100kHz and 1MHz are almost horizontal lines. The output voltage is not necessarily higher for the positive V_p. At higher frequencies, the output voltage is very linearly related to the logarithm of resistance.

The last parameter tested was the voltage gain of the amplifier as the resistor value was altered. The voltage gain was calculated as before by dividing the amplitude of the output voltage by the amplitude of the input voltage, V_{in}, which was set to 2V. The frequencies, resistor values, and V_{DD} remained unchanged from before. The plots of the voltage gain vs. the logarithm of resistance are given in Figures 2.9 and 2.10 for V_p = -8V and +8V, respectively.

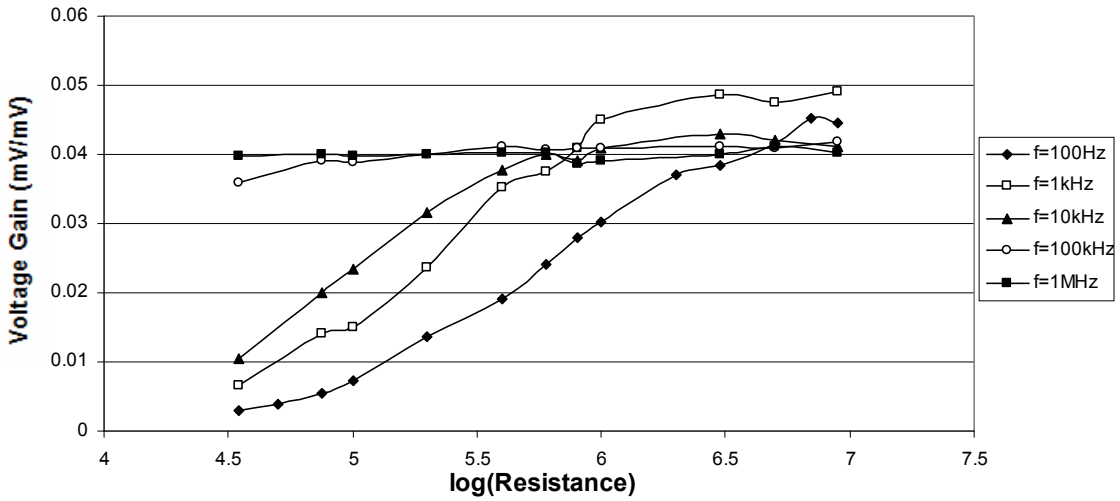

Figure 2.9 Plot of voltage gain vs. logarithm of resistance for five input frequencies for negative polarization voltage

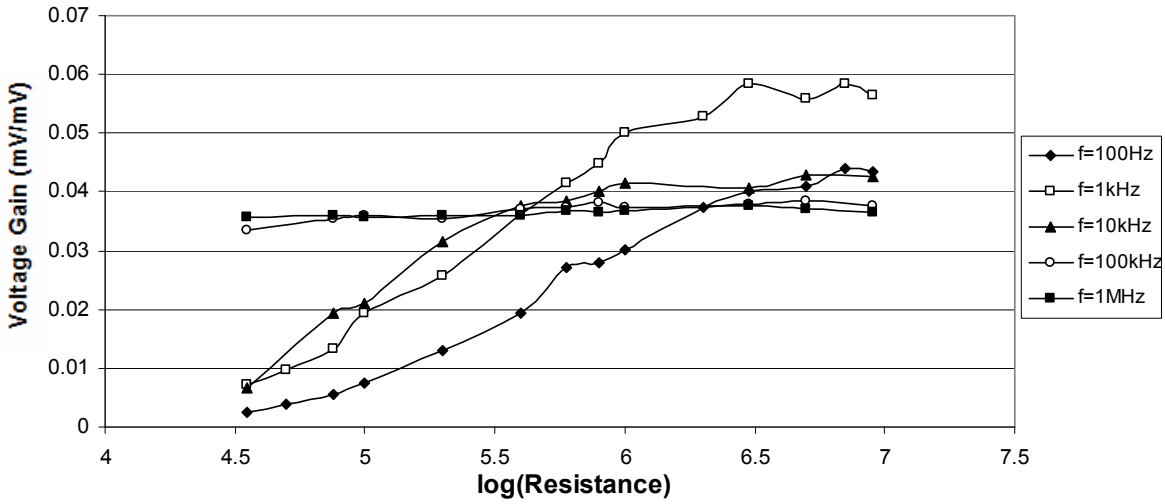

Figure 2.10 Plot of voltage gain vs. logarithm of resistance for five input frequencies for positive polarization voltage

As with the output voltage plots, the voltage gain plots show that the data sets for the two highest frequencies are similar to each other and are almost horizontal lines, while the data sets for the other three frequencies display an increasing, almost linear

slope. The voltage gain is not necessarily higher for the positive V_p data than for the negative V_p data.

C. Comparison of the Voltage Gain and Phase Shift of the FeFET and MOSFET CD Amplifiers

A major property of the MOSFET CD amplifier is its ability to achieve unity voltage gain. The reason behind this voltage gain is that this configuration is a source follower. Thus, the voltage at the source (the output voltage) follows the voltage at the gate (the input voltage), i.e., the output voltage is almost equal to the input voltage [1]. However, observing all the previous plots that include voltage gain shows that the FeFET CD amplifier never produced a voltage gain of one. The input voltage of the FeFET source follower is given by the voltage at the gate (V_{GS}), while the output voltage is just the voltage across the resistor. Since the values for V_{DD} that were experimented with never exceeded 1V because of the fear of burning the transistor, the voltage across the resistor, and therefore V_{out}, was very low. This accounts for the very low values of voltage gain. Higher voltage gain can be obtained by increasing V_{DD}, which would increase V_{out}. In order to safely increase V_{DD}, a larger load resistance must be used.

Another characteristic property of the MOSFET source follower is the absence of phase shifting between the input and output voltage signals at low frequencies. However, the plots of phase shift for the FeFET source follower all show a significant amount of phase shifting at most values of frequency, especially at the lower frequencies. The phase shift between the input and output signals of the FeFET amplifier can be attributed to the ferroelectric property of hysteresis. The output phase shift is related to frequency because the hysteresis curve of the I-V characteristic plot of the FeFET is itself

frequency-dependent, and since phase shifting in the FeFET CD amplifier is a result of the transistor's hysteresis property, changing frequency changes the amount of phase shift. In fact, it was noted that at higher frequencies, there was little to no phase shift in the output signal, and the output signal closely resembled the input signal. Therefore, the FeFET CD amplifier differs from the MOSFET CD amplifier in the phase shifting of the output signal.

D. The Frequency Response

The frequency response of an amplifier, regardless of the amplifier's type, is a critical point of study in the understanding of the amplifier's behavior. One of the most noticeable features of the relationship between the voltage gain and the logarithm of the input frequency is its linearity. The voltage gain is thus logarithmically related to frequency. The frequency response of the MOSFET-based CD amplifier displays a low-frequency band, midband, and high-frequency band [1]. In order to compare the FeFET CD amplifier's frequency response with that of the MOSFET amplifier, the voltage gain in decibels (dB) was plotted against the frequency in Hz, as shown in Figure 2.11. The plot shows logarithmic growth in the low-frequency range and begins to level off at a frequency of 2kHz, which is around the beginning of the mid-frequency range. The plot is therefore analogous to the low-frequency band and the beginning of the mid-frequency band of the MOSFET amplifier's frequency response. Further work on the FeFET CD amplifier can include experimentation with higher frequencies in order to more completely visualize the FeFET mid-frequency response and determine its high-frequency response.

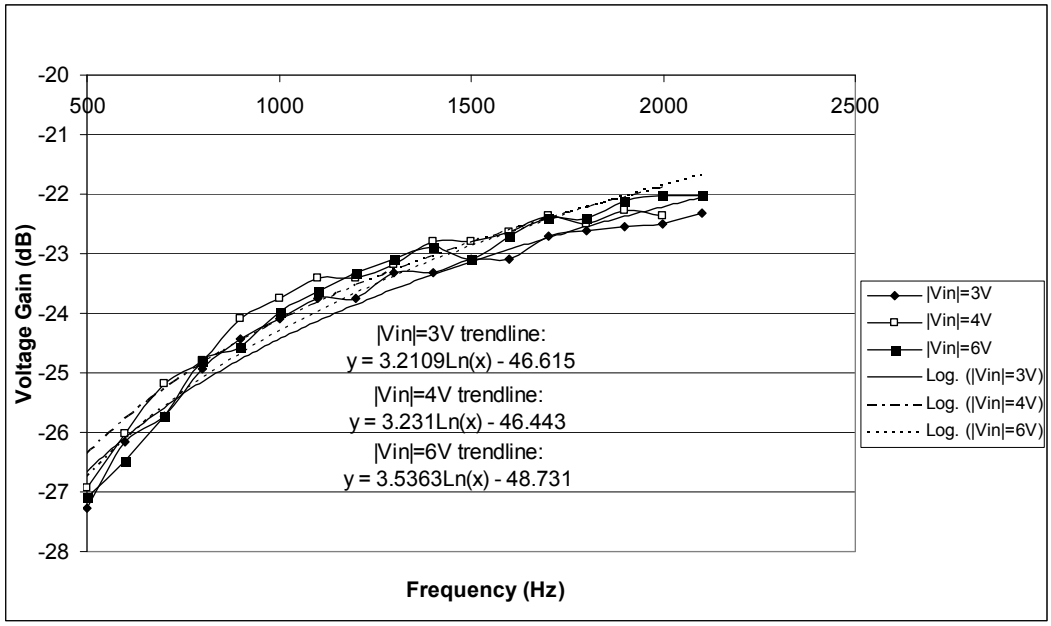

Figure 2.11 FeFET CD amplifier low-frequency response

E. Conclusion of Experimental Results

The linear relationship between the logarithm of frequency and each of the phase shift, output voltage, and voltage gain means that each of these three parameters is logarithmically related to frequency. The same holds true for the resistor value and each of the same three output parameters. The linearity of the relationship between the voltage gain and the logarithm of frequency of the FeFET source follower can have many useful applications. Future work in ferroelectrics can examine the impact of this linear behavior on various circuit configurations, as well as more closely study the relationship between frequency and the hysteresis shape of the FeFET's I-V plots. It was determined that the FeFET CD amplifier produces low voltage gain due to the low values used for V_{DD}. Further measurements with higher values for V_{DD} need to be carried out in order to more effectively compare the FeFET source follower's voltage gain with the voltage gain of

the MOSFET source follower. Moreover, it was noted that the low-frequency response of the FeFET amplifier resembles its MOSFET counterpart, but further study needs to be done on the mid- and high-frequency responses of the FeFET CD amplifier to fully understand this amplifier's frequency response.

F. Nonquasi-Static FeFET CD Amplifier Model

A physically-derived NQS model that is valid in accumulation, depletion, and weak, moderate, and strong inversion and describes the behavior of the FeFET CD amplifier was created in MATLAB®. The model is based on the method of partitioned channel and ferroelectric layer [2]. Partitioning the ferroelectric layer allows for the independence of the partition polarization charges. The effects of time, channel position, applied electric field, polarization, and frequency are incorporated into this model.

The model allows the user to specify values for V_{DD}, input frequency, load resistance (R), phase shift in degrees (θ), number of ferroelectric layer/channel partitions (N), amplitude of the input signal (V_{in}), and input offset voltage (V_{offset}), if it exists. With these user-specified parameters, a sinusoidal input signal is applied at the gate. The signal is then converted to its phasor representation in order to facilitate the calculations. Then, the model numerically calculates the surface potential of the channel with respect to channel position from the source to the drain using Newton's method. With the determined values of surface potential, the MATLAB® code propagates through a function for the estimation of the active and remnant polarization values at the specified ferroelectric partition. This function implements the differential equations describing ferroelectric polarization as a function of an applied electric field [37, 38]. Then, the charge in the ferroelectric layer is calculated, which in turn is used to calculate the

threshold voltage. The NQS y-parameter representation of the drain current is then determined using the calculated threshold voltage and the y-parameters [3]. Finally, the output voltage is determined using Ohm's Law with the drain current and the load resistor.

a. Equations of Variables

The model created is based on the ferroelectric polarization differential equations [37, 38] as well as the standard MOSFET equations [3] modified to reflect the inclusion of the ferroelectric layer. The first equation used is the sinusoidal gate-to-substrate input signal given by

$$v_{gb}(t) = V_{in} \times \cos(\omega t + \theta) + V_{offset}, \tag{2.1}$$

where ω is the angular frequency and t is time. Even though the input signals generated by the function generator were sine waves, cosine equations were used in the code (with the necessary phase shift adjustments that result in sine waves) in order to work with the real part of the phasor quantities. The phasor representation of the transistor voltages and currents are used throughout the model and in the equations of this work due to their simplified form. Thus, the phasor representation of v_{gb} is denoted by V_{gb} and is given by

$$V_{gb} = V_{in} \angle \theta + V_{offset} = \Re(V_{in} \times e^{j(\omega t + \theta)} + V_{offset}). \tag{2.2}$$

Netwon's method is then employed to determine the surface potential at each channel partition. First, V_{gb} is given by a potential balance equation that has been modified from the standard MOSFET version [3] to account for the inclusion of the ferroelectric layer as follows:

$$V_{gb} = \psi_F + \psi_s(x,t) + \phi_{MS}, \tag{2.3}$$

where ψ_F is the ferroelectric potential, $\psi_s(x,t)$ is the surface potential function with respect to channel position x and time t, and ϕ_{MS} is the metal-semiconductor work function. The ferroelectric potential is simply given by

$$\psi_F = -\frac{q'_F}{C'_F}, \tag{2.4}$$

where q'_F is the ferroelectric charge per unit area and C'_F is the ferroelectric capacitance per unit area. Equation (2.3) is then rewritten in terms of the total channel charge per unit area q'_C as follows:

$$V_{gb} = V_{FB} + \psi_s(x,t) + \zeta \frac{q'_C}{C'_F}, \tag{2.5}$$

where V_{FB} is the flat-band voltage and ζ is a variable equal to -1 if $V_{gb} \geq V_{FB}$ or 1 if $V_{gb} < V_{FB}$. The flat-band voltage for the FeFET is given by

$$V_{FB} = \phi_{MS} - \frac{Q'_F}{C'_F}. \tag{2.6}$$

The parameter q'_C in Equation (2.5) is given by the following equation [3]:

$$q'_C = \zeta \sqrt{2q\varepsilon_i N_A} \sqrt{\phi_t e^{\frac{-\psi_s(x,t)}{\phi_t}} + \psi_s(x,t) - \phi_t + e^{\frac{-2\phi_F}{\phi_t}} \left(\phi_t e^{\frac{(\psi_s(x,t)-V_{cb})}{\phi_t}} - \psi_s(x,t) - \phi_t e^{\frac{-V_{cb}}{\phi_t}} \right)}, \tag{2.7}$$

where q is the electronic charge, ε_i is the permittivity of indium oxide, which was assumed to be 8.9 times the permittivity of free space [61], N_A is the acceptor concentration, ϕ_t is the thermal voltage and is equal to 0.0259V, ϕ_F is the Fermi potential, and V_{cb} is the phasor representation of the channel-to-substrate voltage with

respect to channel position x and time t. Thus, to determine the surface potential at the source $\psi_{s0}(t)$, V_{sb} (the phasor source-to-substrate voltage) is substituted in place of V_{cb}, whereas to find the surface potential at the drain $\psi_{sL}(t)$, V_{db} (the phasor drain-to-substrate voltage) is used. At the edges of the channel partitions, V_{cb} is used, and the surface potential difference across a partition is the average of the surface potentials at the partition's two edges. Substituting Equation (2.7) into Equation (2.5) yields

$$V_{gb} = V_{FB} + \psi_s(x,t) - \zeta\gamma\sqrt{\phi_t e^{\frac{-\psi_s(x,t)}{\phi_t}} + \psi_s(x,t) - \phi_t + e^{\frac{-2\phi_F}{\phi_t}}\left(\phi_t e^{\frac{(\psi_s(x,t)-V_{cb})}{\phi_t}} - \psi_s(x,t) - \phi_t e^{\frac{-V_{cb}}{\phi_t}}\right)}, \tag{2.8}$$

where γ is the body effect coefficient and is modified from its MOSFET definition [3] to include the ferroelectric capacitance as follows:

$$\gamma = \frac{\sqrt{2q\varepsilon_i N_A}}{C'_F}. \tag{2.9}$$

To iteratively solve for $\psi_s(x,t)$ using Newton's method, Equation (2.8) must first be rewritten as follows:

$$g = V_{gb} - V_{FB} - \psi_s(x,t) + \zeta\gamma\sqrt{\phi_t e^{\frac{-\psi_s(x,t)}{\phi_t}} + \psi_s(x,t) - \phi_t + e^{\frac{-2\phi_F}{\phi_t}}\left(\phi_t e^{\frac{(\psi_s(x,t)-V_{cb})}{\phi_t}} - \psi_s(x,t) - \phi_t e^{\frac{-V_{cb}}{\phi_t}}\right)}. \tag{2.10}$$

According to Newton's method, the first iteration begins with an initial value m_0, and a new value m_1 and all values resulting from subsequent iterations are calculated by the following set of equations:

$$
\begin{aligned}
m_1 &= m_0 - \frac{g}{\frac{\partial g}{\partial \psi_s}} \\
&\vdots \\
m_n &= m_{n-1} - \frac{g}{\frac{\partial g}{\partial \psi_s}},
\end{aligned}
\tag{2.11}
$$

where the partial derivative of g with respect to ψ_s, $\partial g/\partial \psi_s$ [2], is given by

$$
\frac{\partial g}{\partial \psi_s} = -1 + \frac{\zeta\gamma\left[-e^{\frac{-\psi_s(x,t)}{\phi_t}} + 1 + e^{\frac{-2\phi_F}{\phi_t}}\left(e^{\frac{\psi_s(x,t)-V_{cb}}{\phi_t}} - 1\right)\right]}{2\sqrt{\phi_t e^{\frac{-\psi_s(x,t)}{\phi_t}} + \psi_s(x,t) - \phi_t + e^{\frac{-2\phi_F}{\phi_t}}\left(\phi_t e^{\frac{\psi_s(x,t)-V_{cb}}{\phi_t}} - \psi_s(x,t) - \phi_t e^{\frac{-V_{cb}}{\phi_t}}\right)}}.
\tag{2.12}
$$

The value resulting from the final iteration, m_n, is the value used for $\psi_s(x,t)$. The model is coded so that the number of iterations is determined by the closeness of the resulting values of successive iterations. Thus, a precision value is set so that the loop executing Newton's method ends when the difference between two successive values is less than or equal to the precision value.

In order to make the model as accurate and as representative of the parameters and operation of the actual FeFET used as possible and to guide the modeled results to more empirical accuracy, a best-fit equation was derived for the surface potential so that the empirically-obtained plot of the surface potential vs. the gate voltage of the transistor [62], as shown in Figure 2.12, matches the plot obtained from the model's equations, which is shown in Figure 2.13. The best-fit equation was determined to be the following:

$$
\psi_{s,new}(x,t) = 15.75 * \left[-\left(\frac{200}{N+1}\right) * \left(\psi_s(x,t) + \frac{1.11}{3}\right) + 0.6\right],
\tag{2.13}
$$

where $\psi_{s,new}(x,t)$ is the updated surface potential equation and what is used in the rest of the model when the surface potential value is required. Comparing Figures 2.12 and 2.13 shows that Equation (2.13) results in surface potential values that are very close to the actual empirically-obtained values.

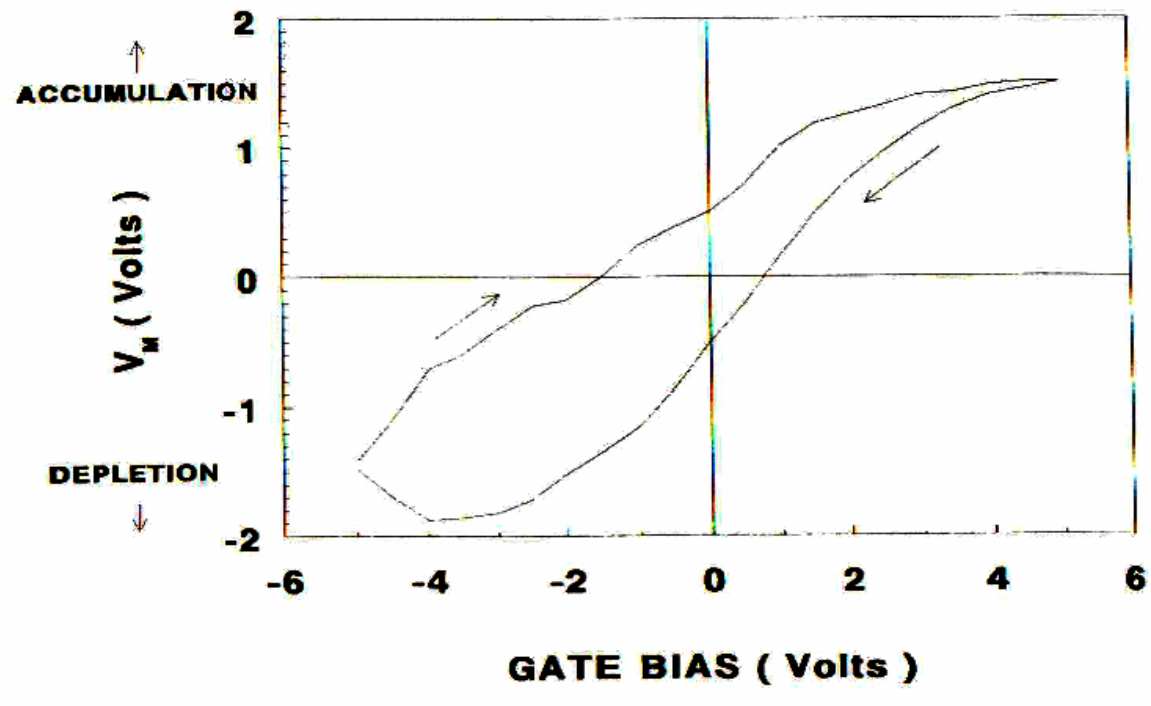

Figure 2.12 Empirical values of surface potential for varying gate voltages of FeFET used in research [62]

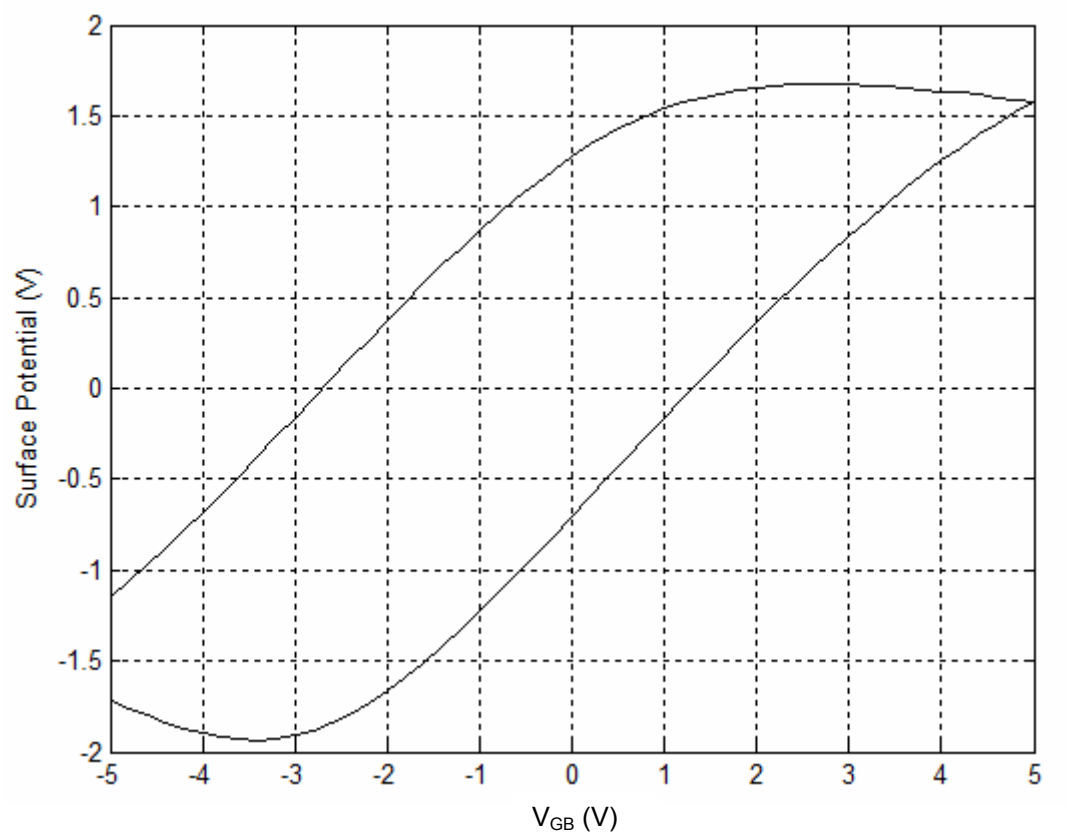

Figure 2.13 Surface potential vs. gate voltage using best-fit equation for surface potential

After determining the surface potential at the source and drain and potential difference across the partitions in the channel, the model propagates through a function for polarization calculation for each channel partition based on the applied electric field [2, 31, 37, 38]. The function begins with the basic saturation polarization equations and the dipole polarization (P_d)-electric field (E) differential equation dP_d/dE as follows [31, 38]:

$$P_{sat}^{+}(E) = P_s \tanh\left[(E - E_c)/2\delta\right] \tag{2.14}$$

and

$$P_{sat}^{-}(E) = -P_{sat}^{+}(-E), \tag{2.15}$$

where

$$\delta = E_c \left[\ln\left(\frac{1 + P_r / P_s}{1 - P_r / P_s} \right) \right]^{-1}. \tag{2.16}$$

$P_{sat}^{+}(E)$ is the positive-going branch of the saturated polarization loop, $P_{sat}^{-}(E)$ is the negative-going branch of the loop, P_s is the spontaneous polarization, P_r is the remnant polarization, and E_c is the coercive electric field, which is the value at which the saturated polarization is zero. With increasing electric field, $P_{sat}^{+}(E)$ is used, while with decreasing field, $P_{sat}^{-}(E)$ is used. The characteristic differential equation describing the relationship between the dipole polarization P_d and the applied electric field [31, 37] is given by

$$\frac{dP_d}{dE} = \Gamma \frac{dP_{sat}}{dE}, \tag{2.17}$$

where

$$\Gamma = 1 - \tanh\left[\left(\frac{P_d - P_{sat}}{\xi P_s - P_d} \right)^{1/2} \right], \tag{2.18}$$

$$\frac{dP_d^{+}(E)}{dE} = P_s \left[2\delta \cosh^2\left(\frac{E - E_c}{2\delta} \right) \right]^{-1}, \tag{2.19}$$

and

$$\frac{dP_d^{-}(E)}{dE} = \frac{dP_d^{+}(-E)}{dE}. \tag{2.20}$$

$P_d^{+}(E)$ is the positive-going branch of the dipole polarization loop and $P_d^{-}(E)$ is the negative-going branch of the loop. The model takes into account the varying electric field history, which is responsible for the varying polarization across the channel. The equation used in the model to simulate the channel position dependence of the applied electric field [2] is given by

$$E_i = \frac{V_{gb} - \left(\frac{\psi_i + \psi_{i+1}}{2} \right)}{t_f}, \tag{2.21}$$

where E_i is the applied electric field at the i^{th} partition, ψ_i is the surface potential at the first edge of the i^{th} partition and ψ_{i+1} is the surface potential at the second edge (and the average of the two potentials yields the surface potential across the partition), and t_f is the thickness of the ferroelectric layer.

After determining each ferroelectric partition's polarization, the total ferroelectric charge per unit area q'_F is found by summing each partition's polarization and dividing by the number of partitions. With this value for q'_F, the threshold voltage V_T can now be accurately calculated by the following equation [3], which accounts for the presence of the ferroelectric layer by using the equation for V_{FB} that has been adapted for the FeFET:

$$V_T = V_{FB} + \phi_B + \gamma \sqrt{\phi_B + V_{SB}}, \tag{2.22}$$

where $\phi_B = 2\phi_F + 6\phi_t$ and V_{SB} is the dc component of $v_{sb}(x,t)$.

At this point, the model calculates the drain current using the NQS y-parameter model. In this representation, the phasor form of the drain current I_d [3] is given by

$$I_d(\omega) = \frac{N_{dd}(\omega)V_{ds} + N_{dg}(\omega)V_{gs} + N_{db}(\omega)V_{bs}}{D(\omega)}, \tag{2.23}$$

where V_{ds}, V_{gs}, and V_{bs} are the phasor representation of $v_{ds}(x,t)$ (the drain-to-source voltage), $v_{gs}(x,t)$ (the gate-to-source voltage), and $v_{bs}(x,t)$ (the substrate-to-source voltage), respectively, and the quantities $N_{kl}(\omega)$ and $D(\omega)$ are infinite series in $j\omega$ of the form [3]

$$N_{kl}(\omega) = n_{kl0} + (j\omega)n_{kl1} + (j\omega)^2 n_{kl2} + \ldots \tag{2.24}$$

$$D(\omega) = d_0 + (j\omega)d_1 + (j\omega)^2 d_2 + \ldots \tag{2.25}$$

Specifically, $D(\omega)$ up to second order [3] is given by

$$D(\omega) = 1 + j\frac{\omega}{\omega_0}\frac{4}{15}\frac{1+3\eta+\eta^2}{(1+\eta)^3} + (j\omega)^2\frac{1}{45\omega_0^2}\frac{1+4\eta+\eta^2}{(1+\eta)^4}, \tag{2.26}$$

$$\begin{aligned}
d_0 &= 1, \\
d_1 &= \frac{4}{15\omega_0}\frac{1+3\eta+\eta^2}{(1+\eta)^3}, \\
d_2 &= \frac{1}{45\omega_0^2}\frac{1+4\eta+\eta^2}{(1+\eta)^4},
\end{aligned}$$

where

$$\begin{aligned}
\eta &= \begin{cases} 1-\dfrac{V_{DS}}{V'_{DS}}, V_{DS} \le V'_{DS} \\ 0, V_{DS} > V'_{DS} \end{cases} \\
V'_{DS} &= \frac{V_{GS}-V_T}{\alpha}, \\
\alpha &= 1+\frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}, \\
\omega_0 &= \frac{V_{GS}-V_T}{L^2\alpha}.
\end{aligned} \tag{2.27}$$

V_{DS}, V_{GS}, and V_{SB} are the dc components of $v_{ds}(x,t)$, $v_{gs}(x,t)$, and $v_{sb}(x,t)$, respectively. L is the channel length. The y-parameters [3] are given by

$$y_{kl} = \frac{N_{kl}(\omega)}{D(\omega)}. \tag{2.28}$$

The equations defining the y-parameters are as follows [3], where W is the channel width and μ is the surface mobility:

$$
\begin{aligned}
n_{dd0} &= \mu \frac{W}{L} C'_F (V_{GS} - V_T)\eta \\
n_{dd1} &= \frac{2}{3} \alpha C_F \frac{\eta(2+\eta)}{(1+\eta)^2} \\
n_{dd2} &= \frac{C_F}{\omega_0} \frac{2}{45} \alpha \frac{\eta(5+8\eta+2\eta^2)}{(1+\eta)^4} \\
n_{dg0} &= \mu \frac{W}{L} C'_F \frac{(V_{GS} - V_T)}{\alpha}(1-\eta) \\
n_{dg1} &= -\frac{2}{3} C_F \frac{\eta(2+\eta)}{(1+\eta)^2} \\
n_{dg2} &= -\frac{C_F}{\omega_0} \frac{2}{45} \frac{\eta(5+8\eta+2\eta^2)}{(1+\eta)^4} \\
n_{db0} &= (\alpha - 1) n_{dg0} \\
n_{db1} &= (\alpha - 1) n_{dg1} \\
n_{db2} &= (\alpha - 1) n_{dg2}
\end{aligned}
\tag{2.29}
$$

To verify the accuracy of the model and its closeness to the FeFET's actual operation, the drain current vs. the drain-to-source voltage was plotted for several gate voltages and compared to the empirically-obtained plot [63]. The empirical plot is shown in Figure 2.14, and the modeled plot is given in Figure 2.15. Examining the figures shows that in both plots, the current increases as the gate voltage increases. The similarity of the plots' shape and values verifies the model's equations.

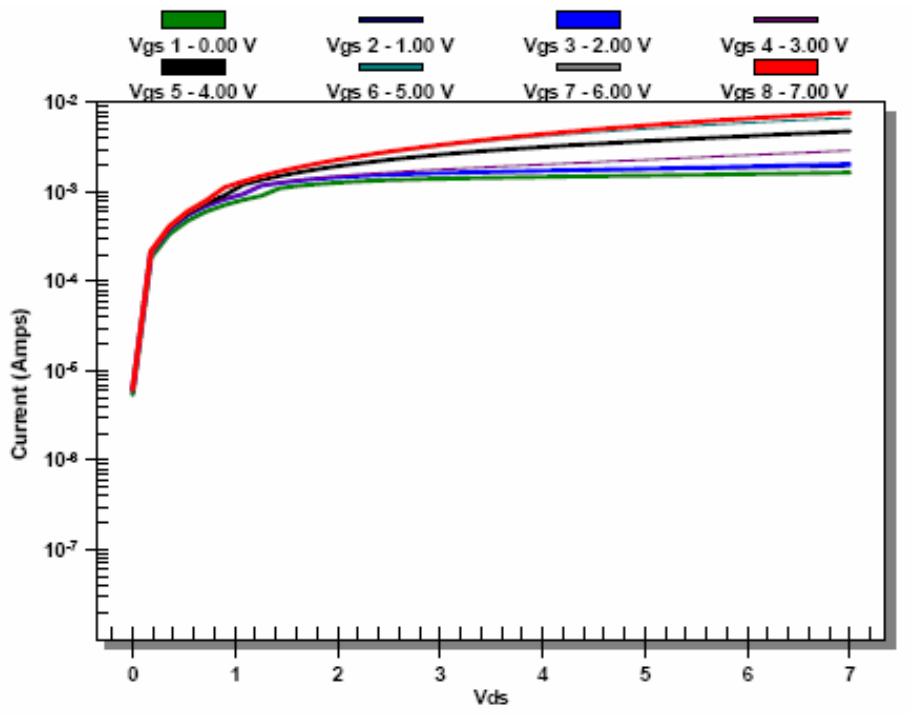

Figure 2.14 Empirical values of drain current vs. drain voltage for varying gate voltages of FeFET used in research [63]

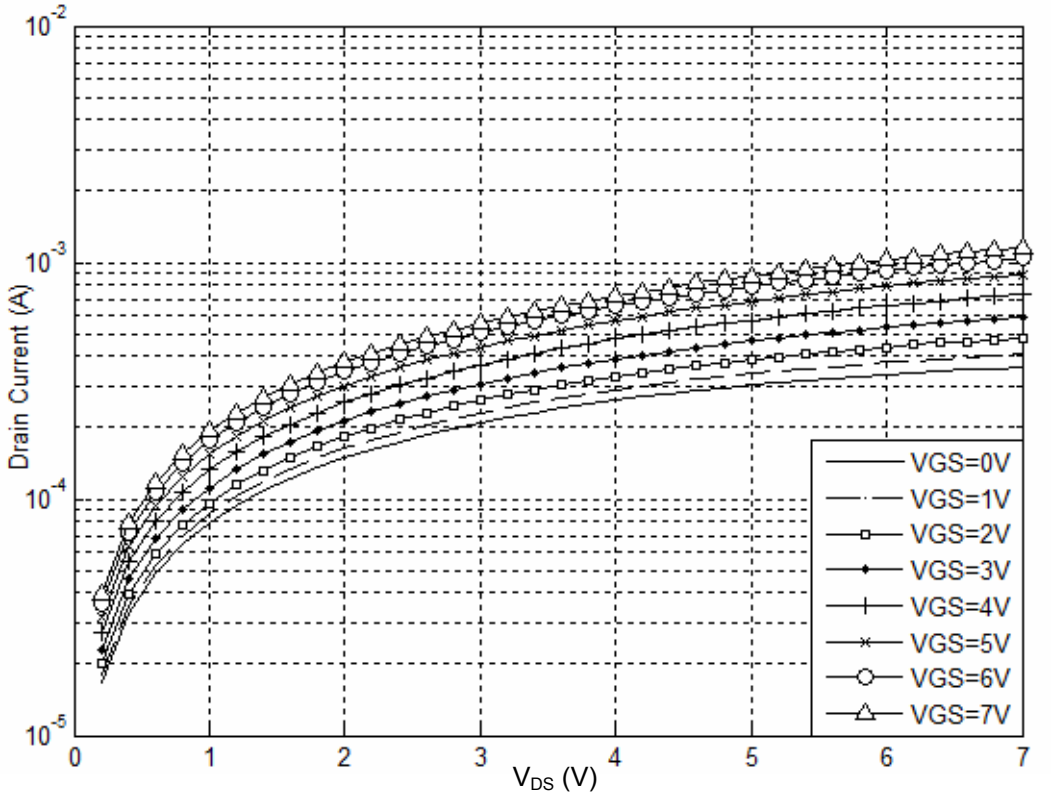

Figure 2.15 Drain current vs. drain voltage for varying gate voltages

Finally, the output voltage is found using Ohm's Law by multiplying the current resulting from substituting Equations (2.24)-(2.29) into Equation (2.23) by the load resistance. The model code produces a plot of the input voltage (V_{in}) and output voltage (V_{out}) with respect to ωt.

b. Simulation Steps

The steps taken to simulate the behavior of the FeFET CD amplifier in MATLAB® are outlined below. These simulation steps were used to obtain the modeled results presented in the next section. A flowchart of the detailed simulation steps is shown in Figure 2.16.

1. Enter fabrication parameters (L, W, N_A, t_f, μ, etc.), simulation time interval, amplifier parameters (V_{DD}, input frequency, amplitude of input signal, load resistance, etc.), dc terminal voltages (V_D, V_G, V_S, and V_B), and number of channel partitions (N).
2. Define the sinusoidal input signals v_{gs} and v_{gb} using the amplifier parameters entered and the current time step.
3. Rewrite the input signals using their phasor representations.
4. Calculate the surface potential at the source ($\psi_{s0}(t)$) and the surface potential at the drain ($\psi_{sL}(t)$) using Newton's method.
5. For each channel partition, calculate the surface potential at both edges of the partition using Newton's method. Then, determine the surface potential across the partition by averaging the potentials at the edges and plugging this value into Equation (2.13) to obtain the most accurate surface potential value.

6. Propagate through a function for polarization and electric field calculations for each partition based on Equations (2.14)-(2.21).
7. Calculate the total ferroelectric charge per unit area, q'_F, by summing each partition's polarization and dividing by the number of partitions.
8. Determine the threshold voltage using Equation (2.22).
9. Use the y-parameter model to calculate the drain current as described in Equations (2.23)-(2.29).
10. Multiply the drain current by a scaling factor to obtain more empirically accurate results.
11. Determine an initial value for the output voltage, V_{out}, using Ohm's Law by multiplying the drain current just determined by the load resistance.
12. Multiply V_{out} by a scaling factor.
13. Update the value of the drain current using Equation (2.23) with V_{ds} being replaced with the difference of V_{DD} and the value for V_{out} just calculated, V_{gs} replaced with the difference of the previous value of V_{gs} and V_{out}, and V_{bs} replaced with the negative of V_{out}.
14. Multiply the drain current by another scaling factor.
15. Recalculate V_{out} using the last value obtained for the drain current.
16. Multiply V_{out} by the same scaling factor used earlier for the initial value of V_{out}.
17. Increment the simulation time by one time step.
18. If the incremented time is less than or equal to the final time step, go to Step 4. Otherwise, plot the output voltage with respect to ωt.

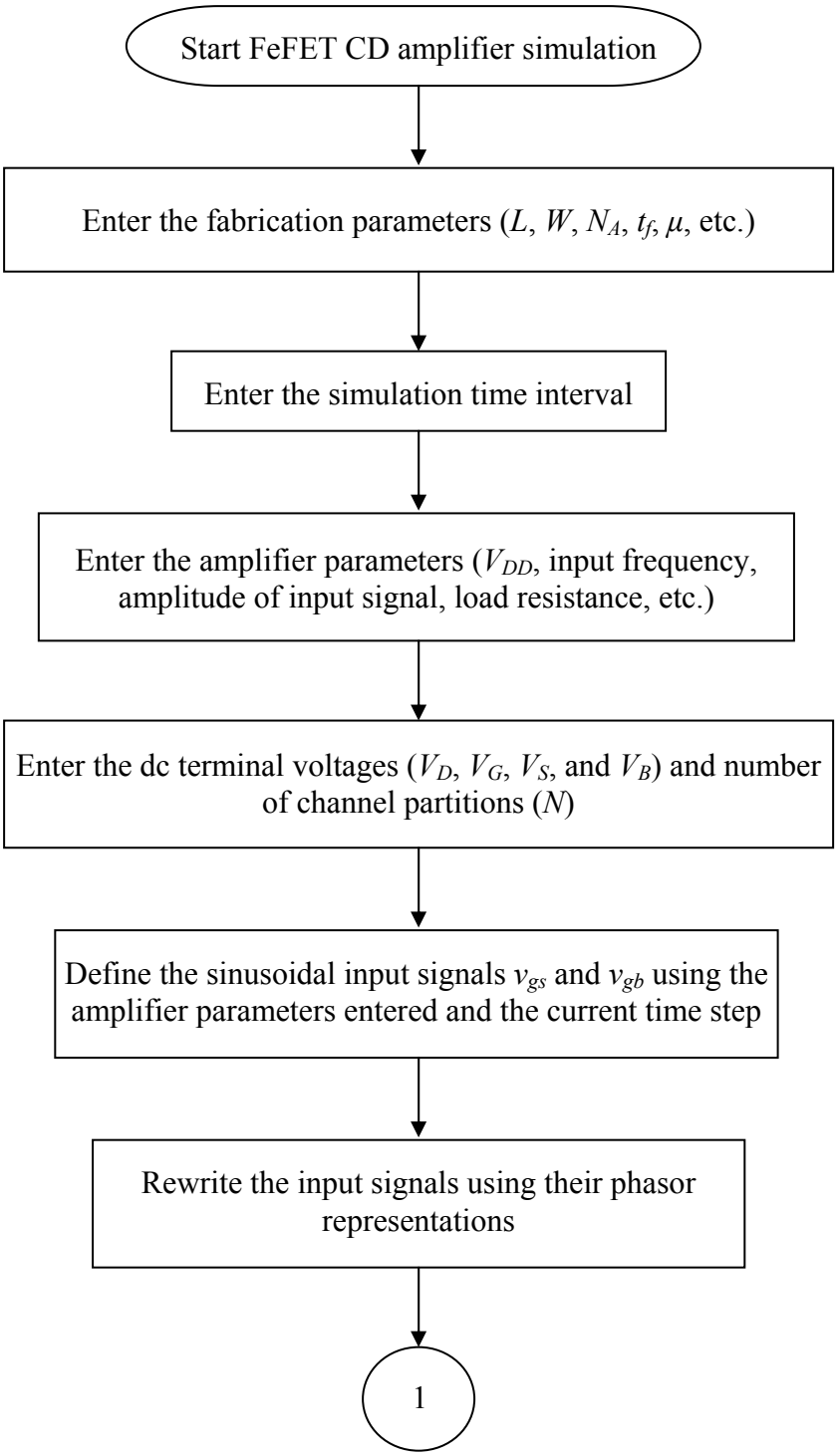

Figure 2.16 FeFET CD amplifier simulation steps

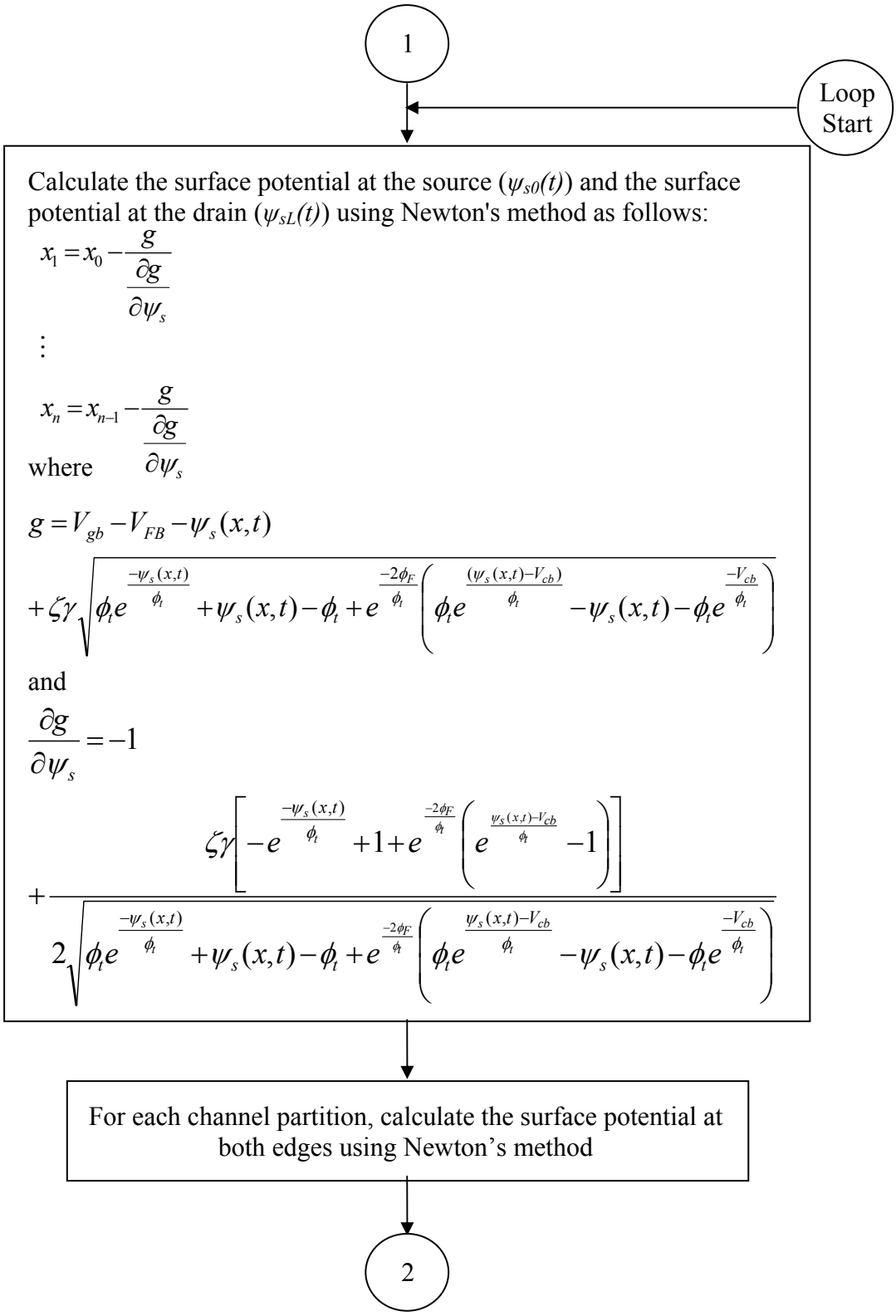

Figure 2.16 FeFET CD amplifier simulation steps (continued)

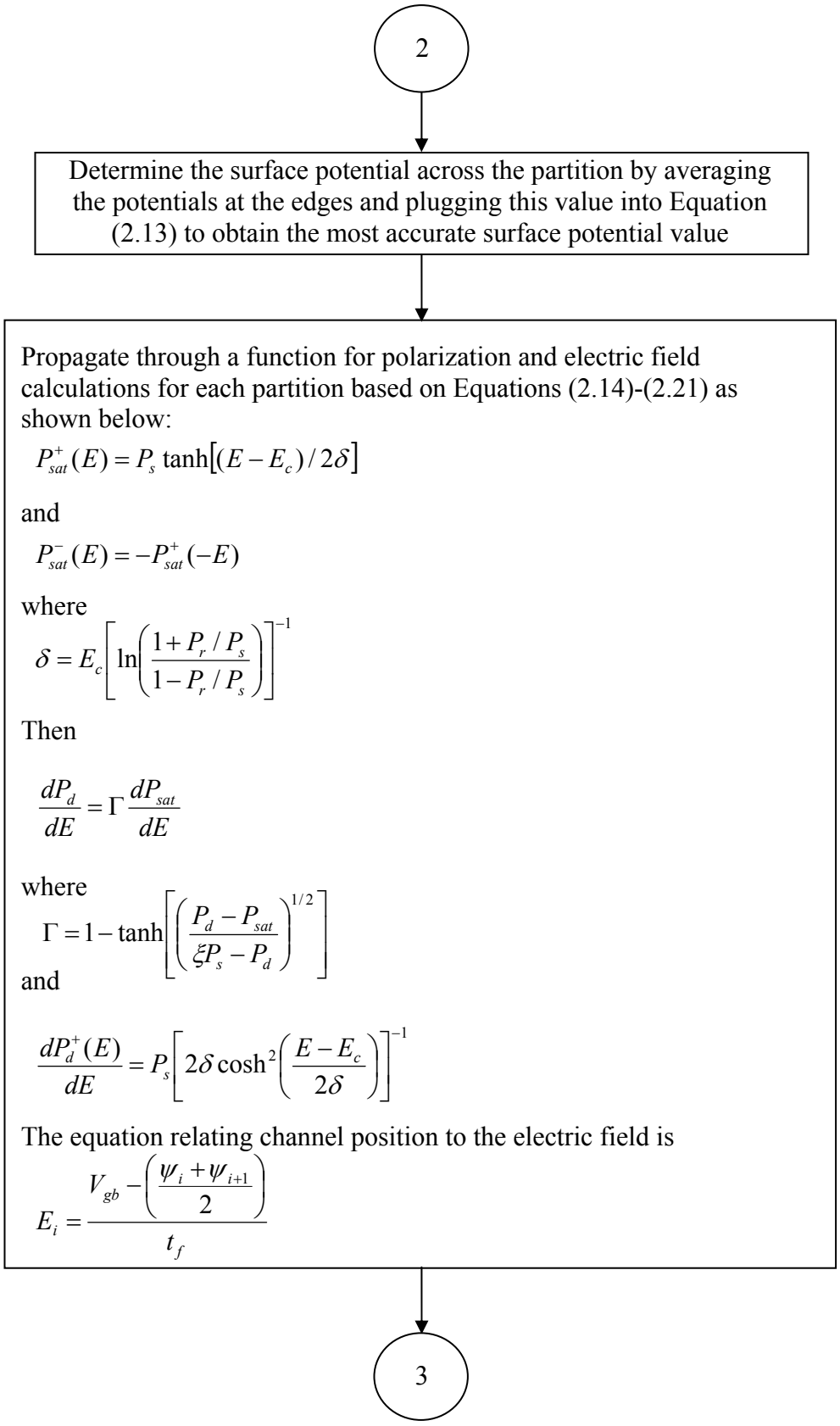

Figure 2.16 FeFET CD amplifier simulation steps (continued)

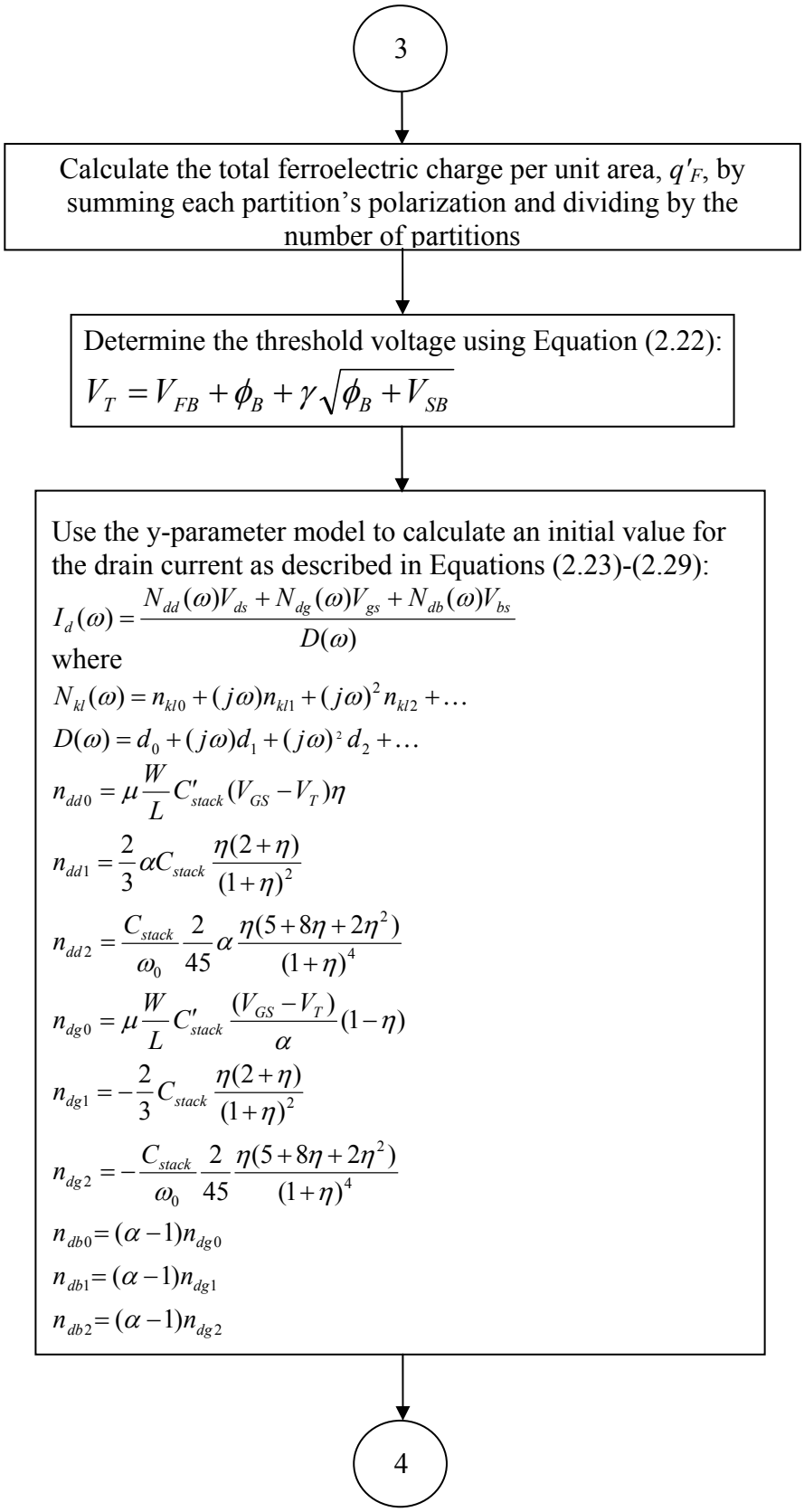

Figure 2.16 FeFET CD amplifier simulation steps (continued)

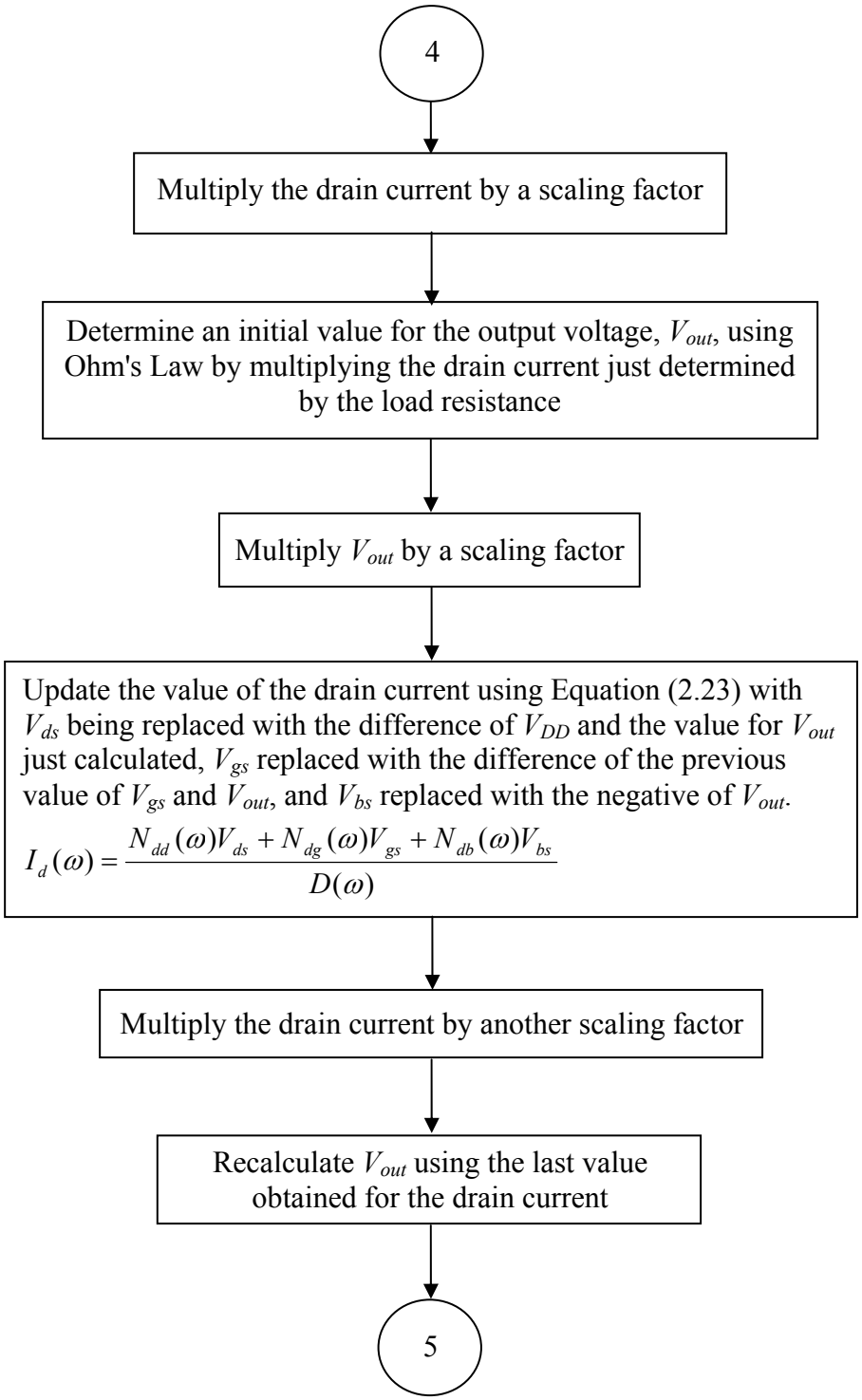

Figure 2.16 FeFET CD amplifier simulation steps (continued)

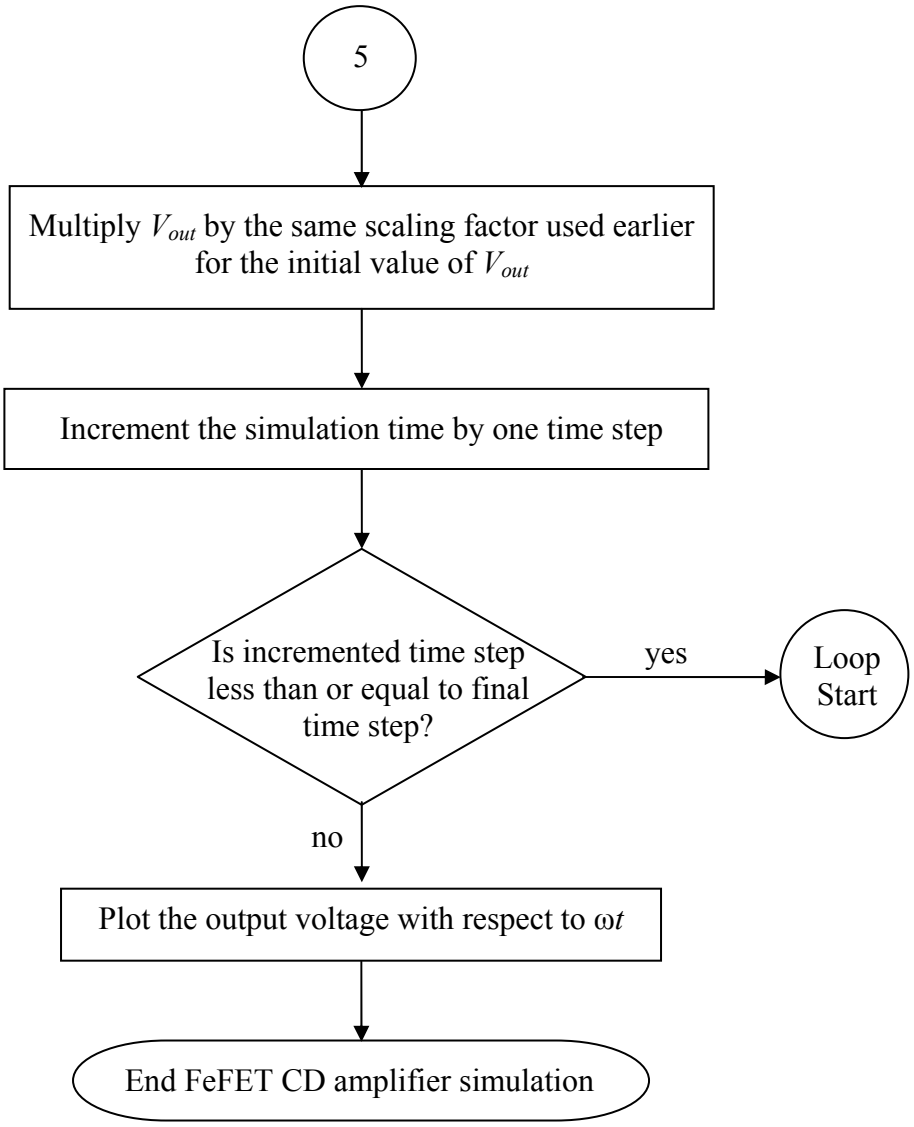

Figure 2.16 FeFET CD amplifier simulation steps (continued)

c. Model Results

In order to verify the accuracy and efficiency of the model, two test cases were carried out to compare the modeled with the empirical results. In the first test case, V_{DD} was 0.5V, the amplitude of the input signal was set to 7V, the input frequency was 1MHz, the load resistance was 100kΩ, the drain current's scaling factor was selected to be 8.0×10^{-11}, and the output voltage's scaling factor was 301. Even though only low

values were used for V_{DD}, the model is still applicable at high V_{DD} values. Figure 2.17 shows the oscilloscope output and Figure 2.18 is the modeled output. It should be noted that on the oscilloscope plots throughout this work, the input and output signals are not always plotted on the same scale. In these cases, the modeled plots are also plotted using different scales.

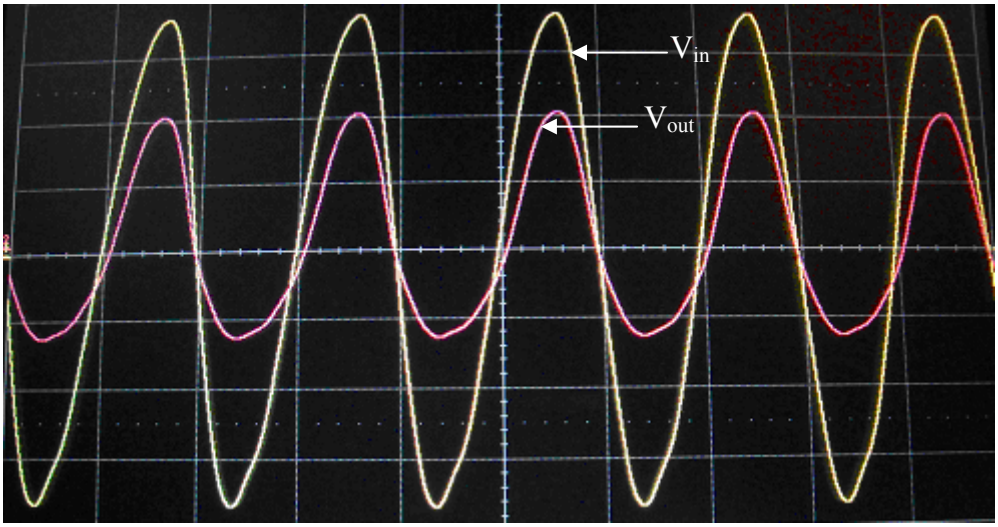

Figure 2.17 Oscilloscope output for the first test case with a scale of 2V per division for V_{in} and 0.5V per division for V_{out}

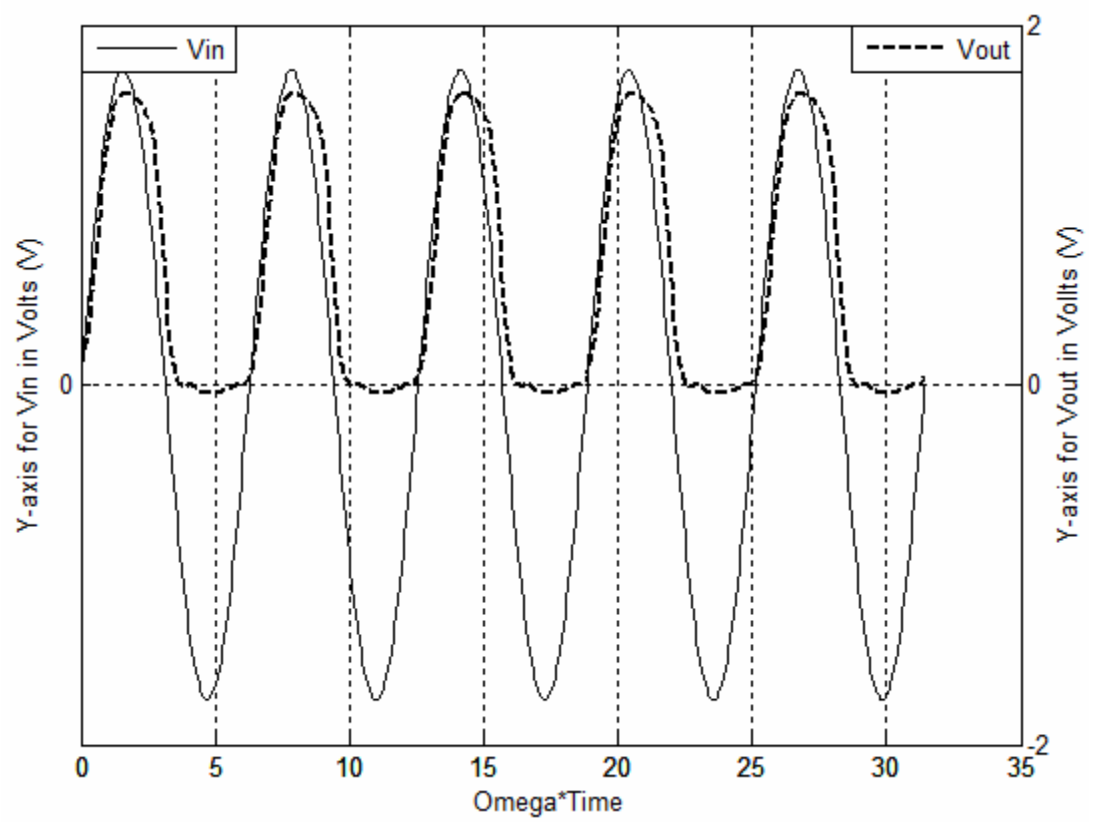

Figure 2.18 Modeled output for the first test case

Examining the modeled plot shows that the model produces an output voltage signal that is similar in shape to the oscilloscope plot; however, the modeled signal barely crosses the x-axis, whereas in the oscilloscope plot, the output signal has a significant negative portion. Despite the modeled plot's accuracy in reproducing the shape and magnitude of the output signal, the maximum and minimum values are not very similar due to the fact that the modeled plot does not go too negative. This dissimilarity between the modeled and oscilloscope plots was only observed with the FeFET CD amplifier since very low values were used for V_{DD} to ensure that the FeFET does not burn since, as aforementioned, the CD amplifier configuration was the first configuration studied. At such low V_{DD} values, any assumptions made in the model were more prominently felt.

For all the amplifier configurations modeled, the modeled output voltage signals displayed inherent phase shifts. For this test case, an inherent phase shift of around 90° was present in the output signal, so the modeled input signal's phase shift parameter was adjusted to produce a phase shift that is similar to that seen in the oscilloscope plot. The precise maximum and minimum values of the simulated output signal and the oscilloscope output signal for the two CD test cases are given in Table 2.1.

For the second test case, V_{DD} was kept at 0.705V, the amplitude of the input signal was 2V, the input frequency was 1MHz, the load resistance was set to 5.6kΩ, and the scaling factors were $7.7\text{x}10^{-7}$ for the drain current and 1 for the output voltage. For this test case, a negative polarization voltage, $V_{p,neg}$, was included to ensure operation in the saturation region, and $V_{p,neg}$ was -8 V. Figures 2.19 and 2.20 show the modeled and oscilloscope output plots, respectively. It should be noted that in the oscilloscope and modeled plots, the offset voltage is not shown.

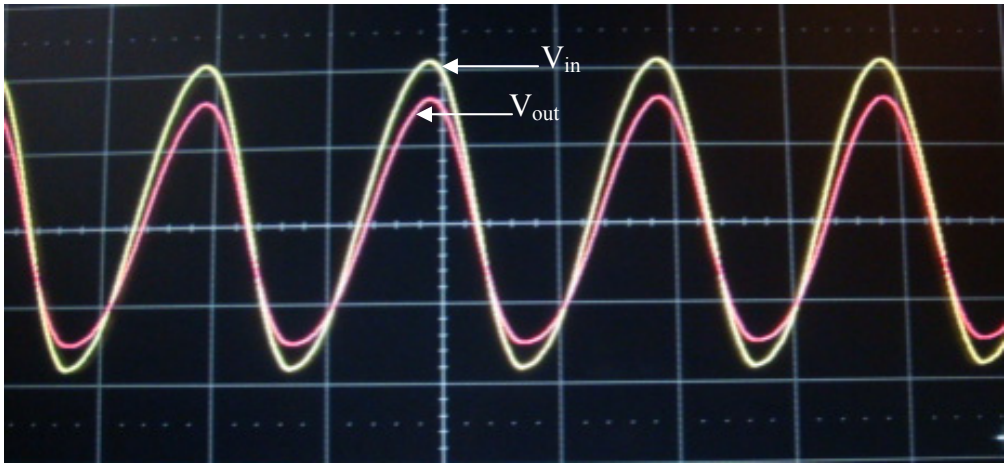

Figure 2.19 Oscilloscope output for the second test case with a scale of 1V per division for V_{in} and 0.05V per division for V_{out}

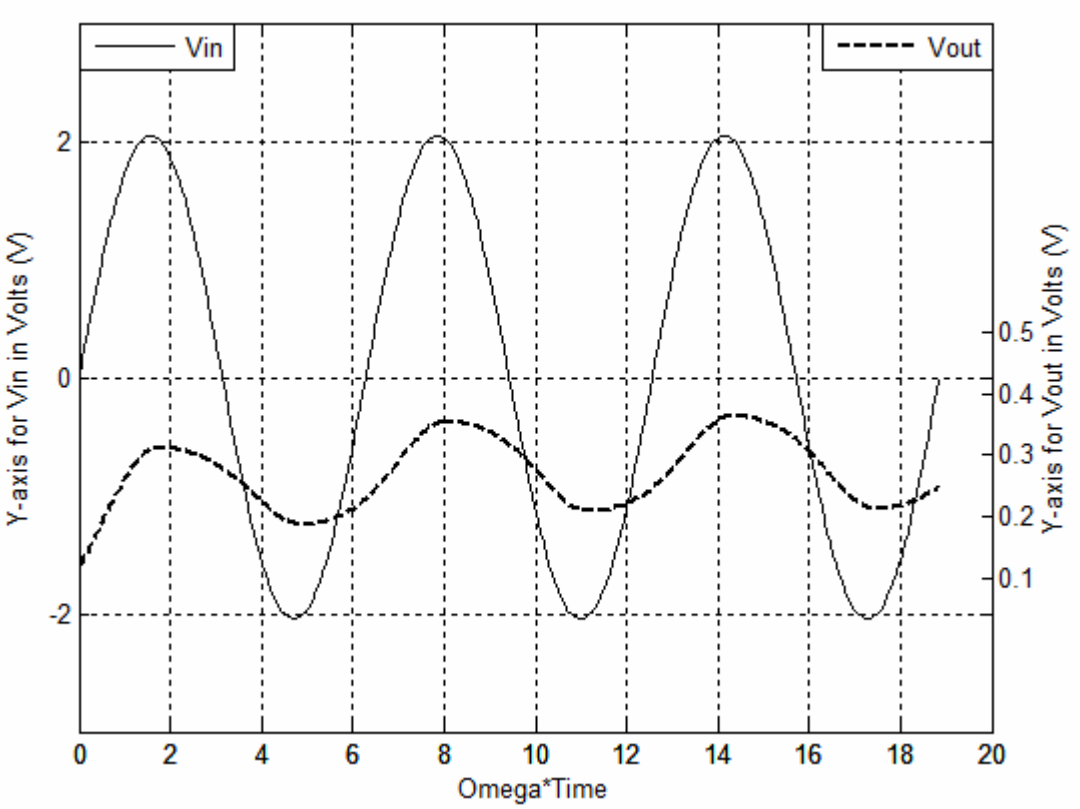

Figure 2.20 Modeled output for the second test case

As with the previous test case, the modeled plot displays great similarity to the oscilloscope plot in the shape and magnitude of the output signal, but the maximum and minimum values, as shown in Table 2.1, are again divergent due to the low values of V_{DD} used. The modeled output plot shows that the output voltage signal takes a few seconds to stabilize and reach consistent values. This is most probably attributed to the effect of ferroelectric polarization, which was sometimes found to fluctuate at the beginning of the oscilloscope plots until it reached a stable position. These fluctuations in ferroelectric polarization affected the drain current of the FeFET, which in turn, affected the output voltage. When the polarization stabilized, the output signal stabilized and the shape and magnitude of the output signal were very close to those of the oscilloscope plot. Also,

the inherent phase shift noticed in this test case's modeled plot was around 100°, so the input signal's phase shift was adjusted accordingly. Despite the differences in the maximum and minimum values of the modeled and oscilloscope signals, the modeled plots are still very similar to the oscilloscope plots for both test cases, yet when higher, more practical values of V_{DD} were used in the other amplifier configurations, the modeled plots were much more accurate and similar to the oscilloscope plots, as will be seen in the next chapters of this work.

Table 2.1 Oscilloscope and simulation results for FeFET CD amplifier

	Test Case I		Test Case II	
	Max. value	Min. value	Max. value	Min. value
Oscilloscope Results	0.975	-0.675	0.083	-0.072
Simulation Results	1.618	-0.0461	0.364	0.213

G. Conclusion of Modeled Data Analysis

A physically-derived NQS model has been developed to describe the behavior of the FeFET CD amplifier. Voltage plots generated in MATLAB® were compared to oscilloscope plots and similarities in shape and magnitude were observed. The modeled results have been shown to be as physically and empirically accurate and effective in describing the ferroelectric-based CD amplifier as possible, given the very low V_{DD} values used in the CD amplifier research. The model's adaptability and effectiveness allow it to be applied to other amplifier configurations, as will be shown later in this work.

CHAPTER III

CHARACTERIZATION AND MODELING OF THE FeFET COMMON-SOURCE AMPLIFIER

The CS amplifier is the most common type of amplifier in MOSFET technology. Therefore, it is of great importance in the advancement of FeFET analog circuitry to characterize and model the behavior of the FeFET-based CS amplifier. This amplifier was built and characterized, then a model was created to describe the amplifier's behavior. Creating a physically-derived NQS model to simulate the behavior of this FeFET amplifier will greatly facilitate the study and design of the FeFET CS amplifier and any circuit configuration that uses this amplifier.

A. Basic Structure

A FeFET CS amplifier is built using a FeFET and a resistor. Figure 3.1 shows the FeFET CS amplifier circuit configuration. A load resistor, R, is connected to the drain of the FeFET. V_{DD} is the voltage from the drain of the transistor, above R, to ground. The source of the FeFET is grounded. The input voltage is provided from the FeFET's gate to ground. The input voltage is comprised of two signals: the dc V_{GS} and the ac v_{gs}. The output voltage v_{out} is taken at the drain below the load resistor. Thus, v_{out} is equivalent to the drain-to-source voltage of the amplifier.

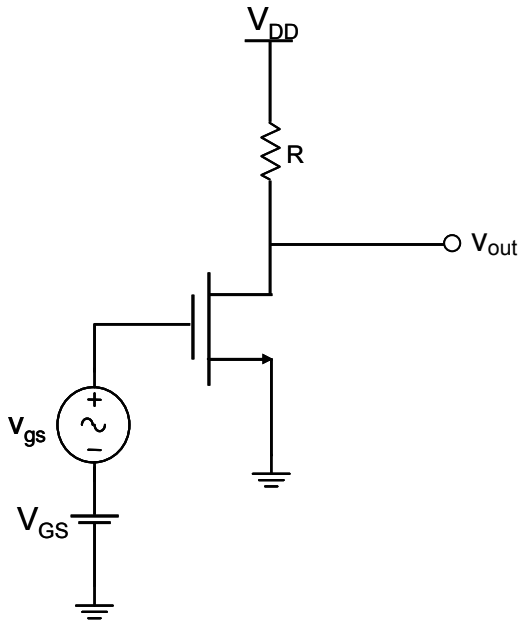

Figure 3.1 FeFET common-source amplifier circuit configuration

B. Empirical Measurements of the FeFET CS Amplifier

Using the circuit configuration shown in Figure 3.1, measurements were carried out to determine the relationship between the frequency of the input signal and each of the phase shift of the output signal, output voltage, and voltage gain of the amplifier. The effect of the load resistance on each of these output parameters was also examined. Then, the relationships between the dc input voltage, output voltage, drain current, and load resistance were studied. Using these measurements, the quiescent point was then calculated. Finally, the power dissipated by the FeFET was observed.

a. Effect of Frequency on Phase Shift, Output Voltage, and Voltage Gain

The first relationship examined is the effect of the input frequency on the phase shift of the output signal. In order to analyze this effect independently from other parameters, V_{DD} was set to 4V and the load resistance was set to 10kΩ, and these variables

remained constant throughout this data set. Then the phase shift of the output signal was measured at frequencies of 1, 10, 100, 1k, 10k, 50k, 100k, 250k, 500k, 1M, and 2.3MHz for V_{in} of 2V, 4V, and 8V, and V_{in} of 2V with V_{offset} of 1.1V. In all the empirical measurements of the CS amplifier, V_{in} is equivalent to the peak-to-peak value of the ac signal v_{gs}, and V_{offset}, if it is included, is the peak-to-peak value of the dc offset signal V_{GS}. These values for V_{DD}, the input voltage, the offset voltage, and the load resistance were chosen to ensure that the magnitude of the gate voltage never exceeds 8V in order not to rupture the gate of the FeFET and that the current flowing through the transistor at any time never exceeds 1mA so the transistor is not burned. The degree values of the phase shifts were plotted against the logarithm of frequency, as shown in Figure 3.2. Throughout this work, negative values of phase shift indicate that the output signal is lagging the input signal, whereas positive values of phase shift mean that the output signal is leading the input signal. Also, all logarithms in these measurements are of base 10.

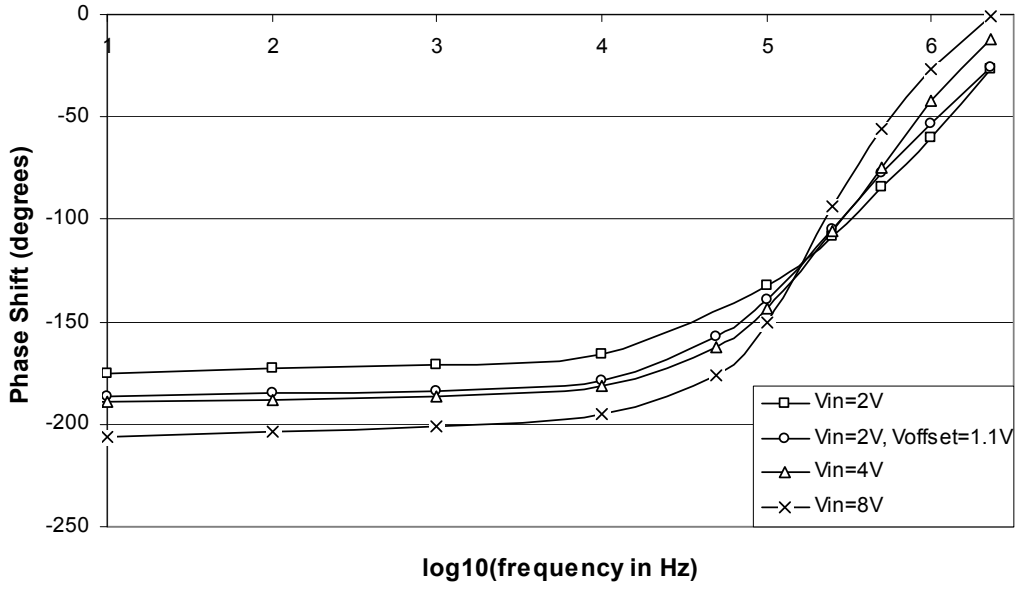

Figure 3.2 Plot of phase shift vs. logarithm of frequency for four values of V_{in}

This plot shows a distinct trend in the relationship between the output phase shift and the input frequency. The almost perfectly linear plot lines that connect the data points when the logarithm of the input frequency is less than or equal to four indicate that the phase shift is logarithmically related to the input frequency for these frequency values. The same holds true for the data points at frequency values whose logarithm is higher than four. These logarithmic relationships, along with the equations of the trend lines that best describe them, are shown in Figure 3.3. As can be seen from this figure, the data lines for input frequencies at or below 10kHz have almost the same slope and are nearly parallel. The data lines for frequencies above 10kHz also have very similar increasing slopes. Both figures show that at lower frequencies, the higher the input voltage, the higher the magnitude of the phase difference that exists between the input and output signals. However, at higher frequencies, the magnitude of the phase shift decreases with increasing input voltage.

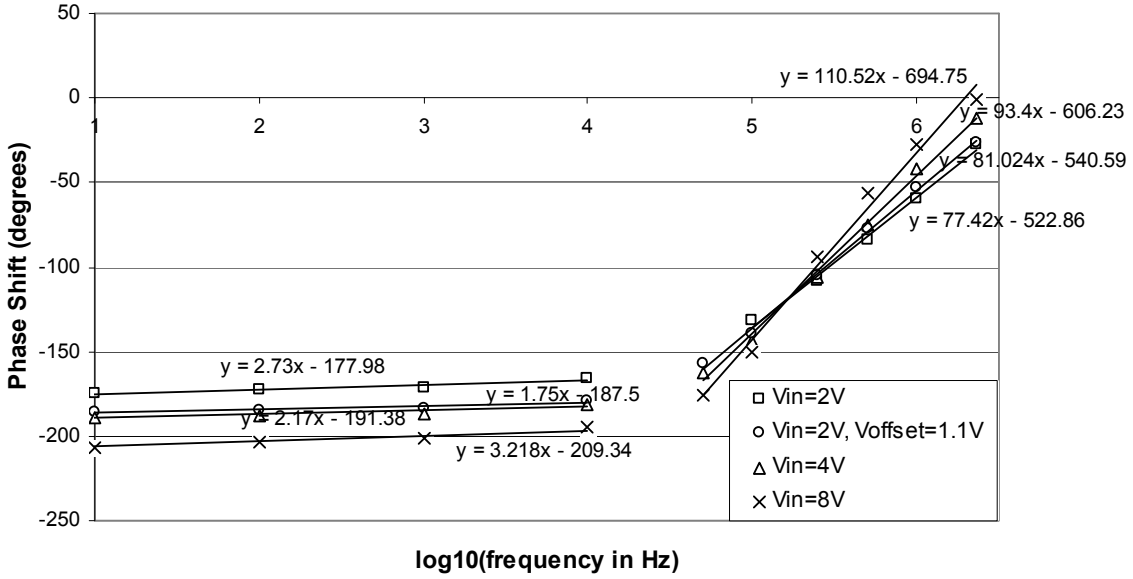

Figure 3.3 Plot of phase shift vs. logarithm of frequency for four values of V_{in} with trend lines

The effect of input frequency on the output voltage was also examined. V_{DD} and the load resistance remained at 4V and 10kΩ, respectively. The peak-to-peak output voltage in volts was measured at each of the aforementioned input frequencies between 1Hz and 2.3MHz for the input voltages of 2V, 4V, 8V, and 2V with 1.1V offset. Figure 3.4 shows the data points of the output voltage vs. the input frequency for these four input voltages.

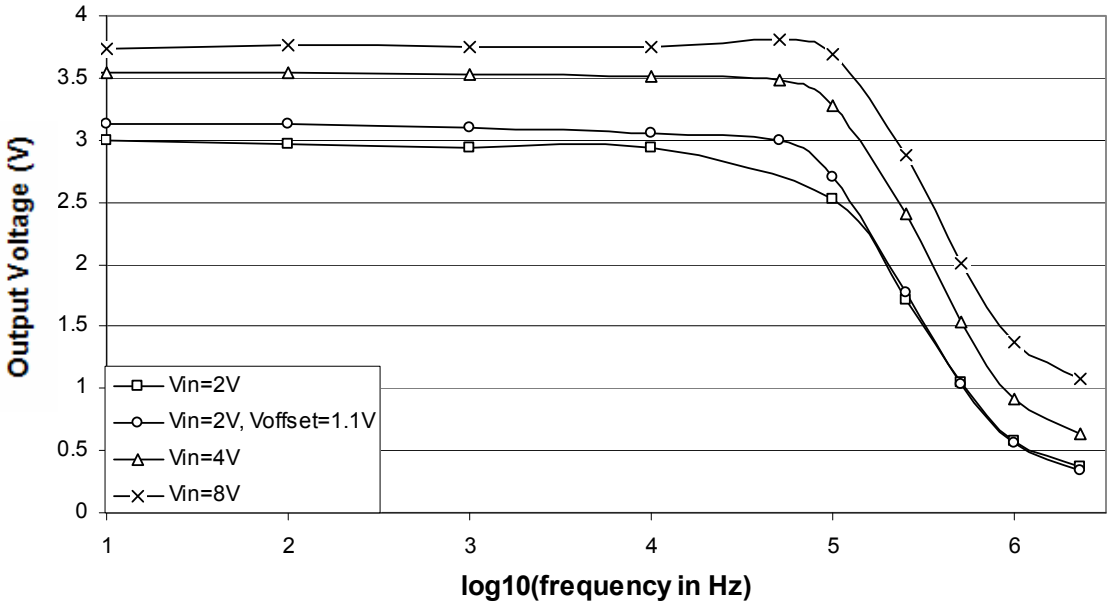

Figure 3.4 Plot of output voltage vs. logarithm of frequency for four values of V_{in}

This plot shows several important characteristics about the effect of input frequency on the output voltage. At input frequencies lower than 10kHz, the relationship between these two parameters can be described by nearly straight lines for all values of the input voltage, which indicates that the output voltage is logarithmically related to the input frequency at lower frequency values. There is also a logarithmic relationship between the output voltage and the input frequency for frequencies of 10kHz or higher. These

correlations are shown in Figure 3.5, where linear trend lines connect the data points and the equations governing these trend lines are shown. As can be seen from this figure, the four lower-frequency lines are almost parallel, and the four higher-frequency lines have similar decreasing slopes. Moreover, both figures show that at nearly all frequencies, the higher the input voltage, the higher the voltage produced at the output. However, one observation that is not noted in Figure 3.5 but is seen in Figure 3.4 is that each plot line tends toward a constant value for very high input frequencies. Since the function generator used was not capable of generating input frequencies higher than 2.3MHz, this leveling-off effect was not closely studied; however, this circuit's behavior at very high frequencies is a very interesting point for future study.

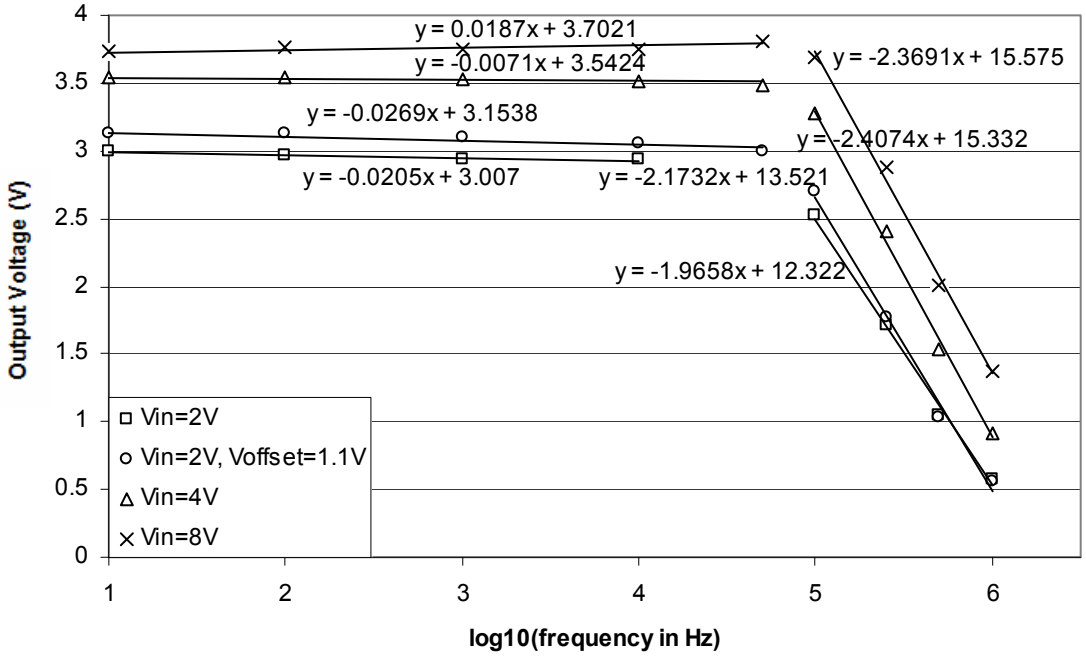

Figure 3.5 Plot of output voltage vs. logarithm of frequency for four values of V_{in} with trend lines

The last parameter measured against input frequency was the voltage gain. Keeping V_{DD} and the load resistance unchanged from the previous measurements, the voltage gain was measured in V/V and plotted at the four aforementioned input voltages using the same range of input frequencies. Figure 3.6 shows the plots of the voltage gain vs. the logarithm of frequency.

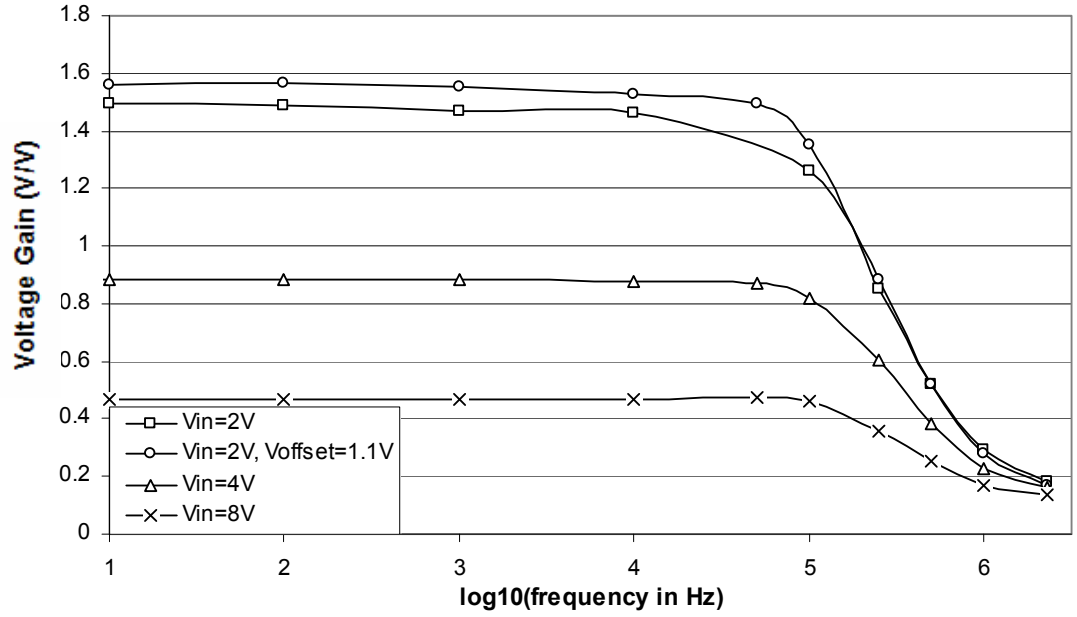

Figure 3.6 Plot of voltage gain vs. logarithm of frequency for four values of V_{in}

As expected, the voltage gain plot was similar in shape to the output voltage plot, since the voltage gain is simply the output voltage divided by the input voltage. The voltage gain plot also displays the same key characteristics as the output voltage plot. Thus, the voltage gain data lines are linear and parallel for input frequencies below 10kHz and are linear with negative slopes for frequencies between 10kHz and 1MHz. This logarithmic relationship is shown in Figure 3.7, where the equations of the linear trend lines are given. Also similar to the output voltage plot, the voltage gain plot of Figure 3.6 shows that at frequencies higher than 1MHz, a leveling-off effect occurs and the data

points tend toward a constant value; but with the voltage gain plots, the four data sets seem to converge to a single constant value rather than a constant value for each input voltage. Despite these similarities, there is one striking difference between the voltage gain plot and the output voltage plot—unlike the output voltage data lines, the voltage gain lines decrease with increasing input voltage. This is due to the fact that, as Figure 3.4 shows, the increase in the output voltage was not as large as the increase in the input voltage. Therefore, when the output voltages were divided by the increasing input voltages, smaller gain was produced at higher input voltages. The one data set that seems to not follow the trend of decreasing gain with increasing input voltage is the data set for V_{in} = 2V and V_{offset} = 1.1V. The reason for this data set's difference is not incongruity of the data, rather it is a result of the definition for voltage gain used throughout this dissertation; specifically the voltage gain is the output voltage divided by the ac input voltage, i.e., v_{gs} in the circuit configuration shown in Figure 3.1.

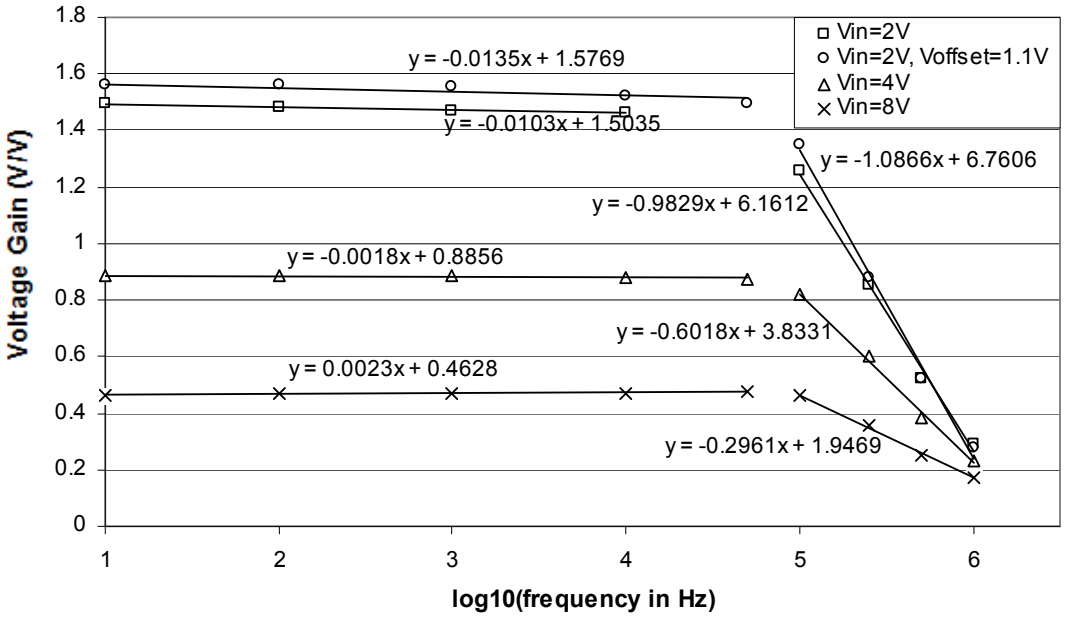

Figure 3.7 Plot of voltage gain vs. logarithm of frequency for four values of V_{in} with trend lines

b. Effect of Load Resistance on Phase Shift, Output Voltage, and Voltage Gain

After examining the relationship between the input frequency and each of the phase shift, output voltage, and voltage gain, the effect of the load resistance on each of these three parameters was examined. For these measurements, V_{DD} was set to 4V and V_{in} was chosen to be 2V. Then, for each of the input frequencies of 100Hz, 50kHz, and 100kHz, the phase shift, output voltage, and voltage gain were measured at load resistances of 5k, 10k, 15k, 20k, 30k, 40k, 50k, 100k, and 250kΩ.

Figure 3.8 shows the relationship between the phase shift of the output signal and the logarithm of the load resistance with linear trend lines and their equations. As can be seen from the plot, the phase shift is almost linearly related to the logarithm of resistance; i.e., the phase shift is logarithmically related to the load resistance. Also, as the input frequency increases, the magnitude of the phase shift decreases. Examining the equations of the trend lines shows that the 50kHz and 100kHz trend lines are almost parallel.

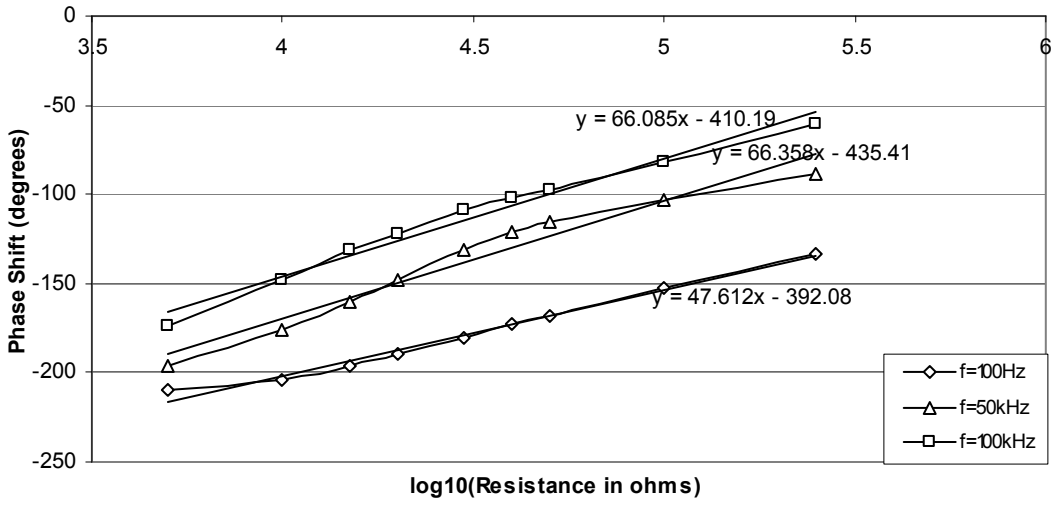

Figure 3.8 Plot of phase shift vs. logarithm of resistance for three frequencies with trend lines

The next relationship examined was the effect of the load resistance on the output voltage. Figure 3.9 is a plot of the output voltage vs. the logarithm of the load resistance. The three data lines are similar in shape, but the 50kHz and 100kHz plots are especially alike, as was noted in the phase shift vs. resistance plots. At almost all resistor values, the output voltage decreases with increasing frequency.

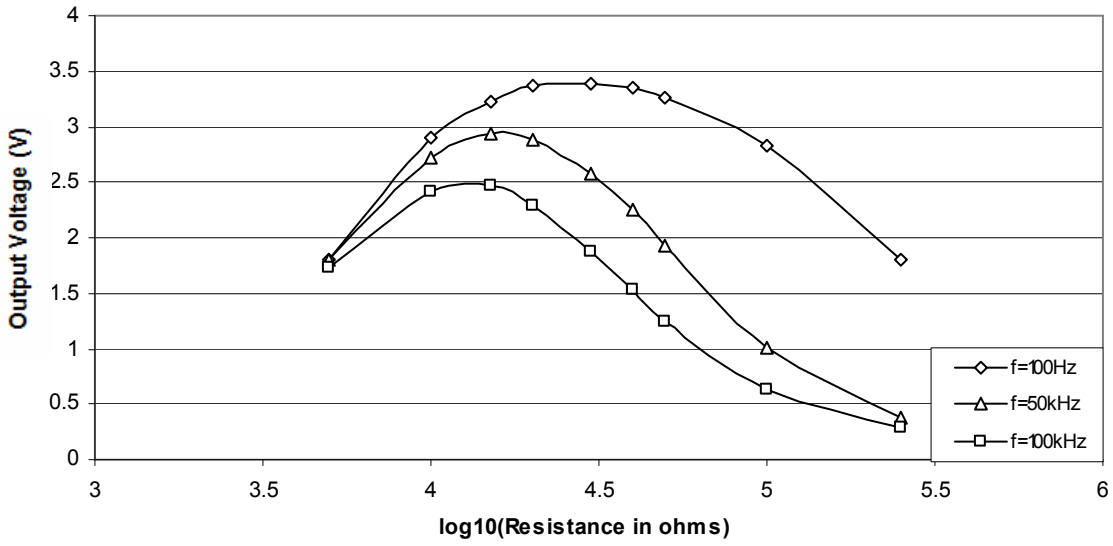

Figure 3.9 Plot of output voltage vs. logarithm of resistance for three frequencies

The last parameter measured against the logarithm of resistance was the voltage gain. The plot depicting this relationship is shown in Figure 3.10. As with the output voltage plot, the three data lines are alike in shape, and the 50kHz and 100kHz data lines are very similar to each other. As was expected from examining the output voltage vs. logarithm of resistance plot, the voltage gain decreases with increasing frequency.

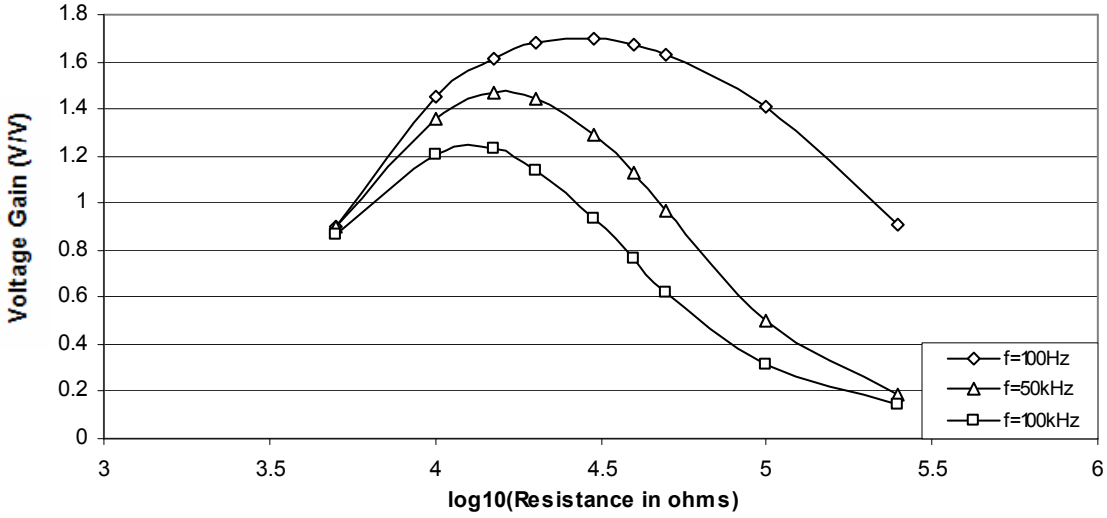

Figure 3.10 Plot of voltage gain vs. logarithm of resistance for three frequencies

c. Relationships between DC Input Voltage, Output Voltage, Drain Current, and Load Resistance

After examining the behavior of the CS amplifier's phase shift, output voltage, and voltage gain and the effects of the input frequency and the load resistance on each of these parameters, the relationships between the dc input voltage (V_{GS}), output voltage (V_{out}), drain current (I_D), and load resistance (R) were examined. First, the output voltage was plotted against the dc input voltage for three different values of load resistance: 5kΩ, 10kΩ, and 15kΩ. For each case, V_{DD} was set to 4V, and the FeFET was positively and negatively polarized. Positive polarization of the transistor gate was achieved by pulsing V_{GS} at 5V, while the gate was negatively polarized by pulsing V_{GS} at -5V. Then, the effect of the input voltage on the drain current was studied for the same three resistance values for both positive and negative polarizations. Finally, the relationship between the output voltage and the drain current was determined.

The first relationship examined was that of V_{out} vs. V_{GS}. Since only the effect of the dc component of the input voltage on the output voltage was to be studied, v_{gs} was set to 0V. For each of the three values of load resistance tested, the gate of the FeFET was polarized twice: once positively and once negatively. Positive polarization testing was carried out by setting V_{GS} to 0V then increasing it to 1.5V in 0.5V increments, followed by a 0.25V incremental increase to around 5V. At each value of the dc input voltage, the output voltage was tested for each of the load resistance values of 5kΩ, 10kΩ, and 15kΩ. Then, the FeFET under negative polarization was examined. V_{GS} was decreased to around -3V and increased to about 3V in 0.25V increments. Again, the value of V_{out} at each V_{GS} value was measured for each of the three resistance values. Figure 3.11 is the plot of V_{out} vs. V_{GS} for both positive and negative polarizations at all three load resistances.

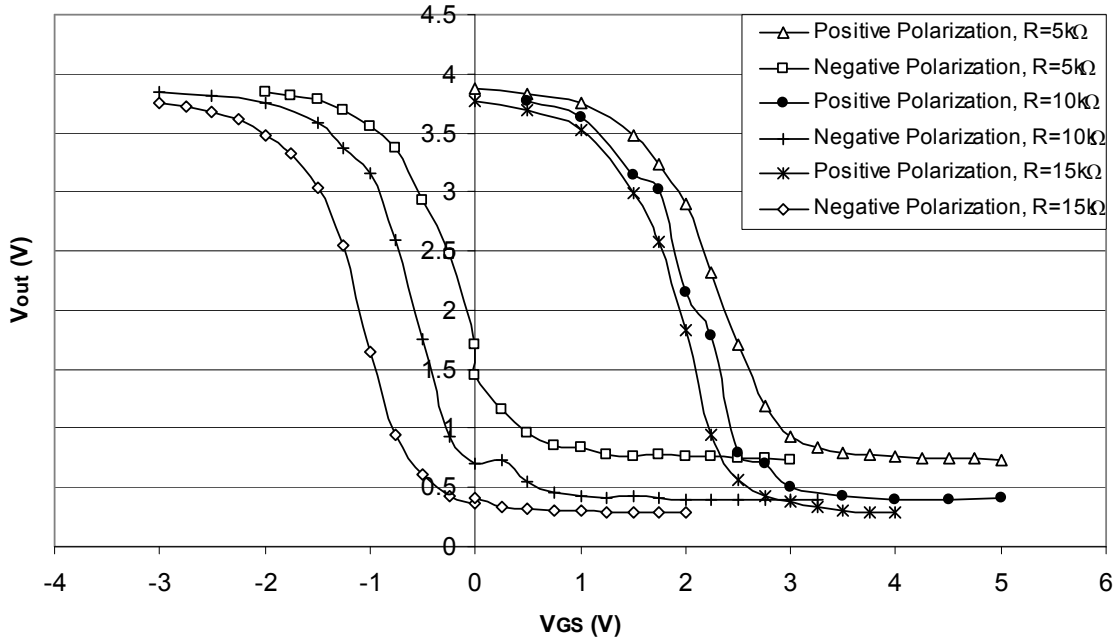

Figure 3.11 Plot of output voltage vs. dc input voltage for V_{DD} = 4V

The most notable feature of the plot of Figure 3.11 is its hysteretic shape, which closely resembles that of the FeFET's modeled I_D vs. V_{GS} characteristic plot when the gate voltage is off, as was shown in Figure 1.8. This is expected since I_D is related to V_{out} of the CS amplifier by the following simple linear equation:

$$(V_{DD} - V_{out})/R = I_D. \tag{3.1}$$

This relationship leads to the following equation for V_{out} in terms of I_D:

$$V_{out} = - I_D*R + V_{DD}. \tag{3.2}$$

The negative sign preceding I_D explains the plot's resemblance to the I-V characteristic hysteresis plot when the gate voltage is off, rather than when the gate voltage is on.

Closer examination of the plot of Figure 3.11 reveals more interesting elements of the relationship between output voltage and dc input voltage. At all V_{GS} values under both positive and negative polarization, the output voltage decreases with increasing load resistance. For each resistance value, the negative and positive polarization portions of the plot tend to level off at the top and bottom of the plot to approximately the same value for V_{out}. This further helps to achieve the hysteretic shape of each resistance plot.

The relationship between I_D and V_{GS} was next examined. Again, v_{gs} was set to 0V, and the FeFET was both positively and negatively polarized as was done for the V_{out} vs. V_{GS} relationship for each of the 5kΩ, 10kΩ, and 15kΩ load resistances. For each resistance, at each value of V_{GS}, the drain current was calculated using Equation (3.1) based on the value of V_{out} at that point. Figure 3.12 shows the data points obtained from the measurements.

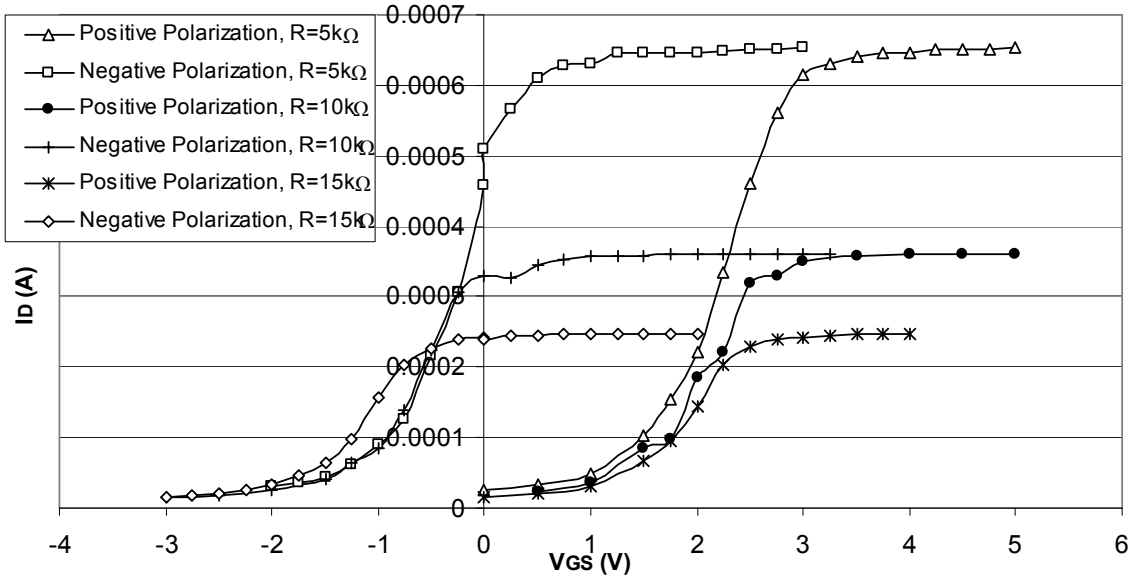

Figure 3.12 Plot of drain current vs. dc input voltage for V_{DD} = 4V

The plot of Figure 3.12 is characterized by a distinct hysteretic shape that is very similar to that of the I-V plot for a FeFET when the gate voltage is on, as was shown in Figure 1.7. This is as expected since there is no negative sign preceding I_D as was the case in Equation (3.2) for the previous relationship examined.

The trends portrayed by the data of the plot of Figure 3.12 are very similar to those shown in Figure 3.11 as a result of the two plots' correlation. In fact, Equation (3.1) describes the relationship between the two plots. Thus, the plot of I_D vs. V_{GS} has the same shape of the plot of V_{out} vs. V_{GS} but flipped across the y-axis. Also, the I_D vs. V_{GS} plot displays the trend of decreasing drain current as the load resistance is increased for most of the data points, similar to the previous plot's trend of decreasing output voltage with increasing resistance. Moreover, for each resistance value, the positively and negatively polarized portions of the plot of Figure 3.12 tend to level off to the same value, as was the case for the V_{out} vs. V_{GS} plot.

Finally, the effect of the output voltage on the drain current was examined. The calculated values of I_D were plotted against the measured values of V_{out} for each of the three resistance values under both positive and negative polarization. The plot is shown in Figure 3.13.

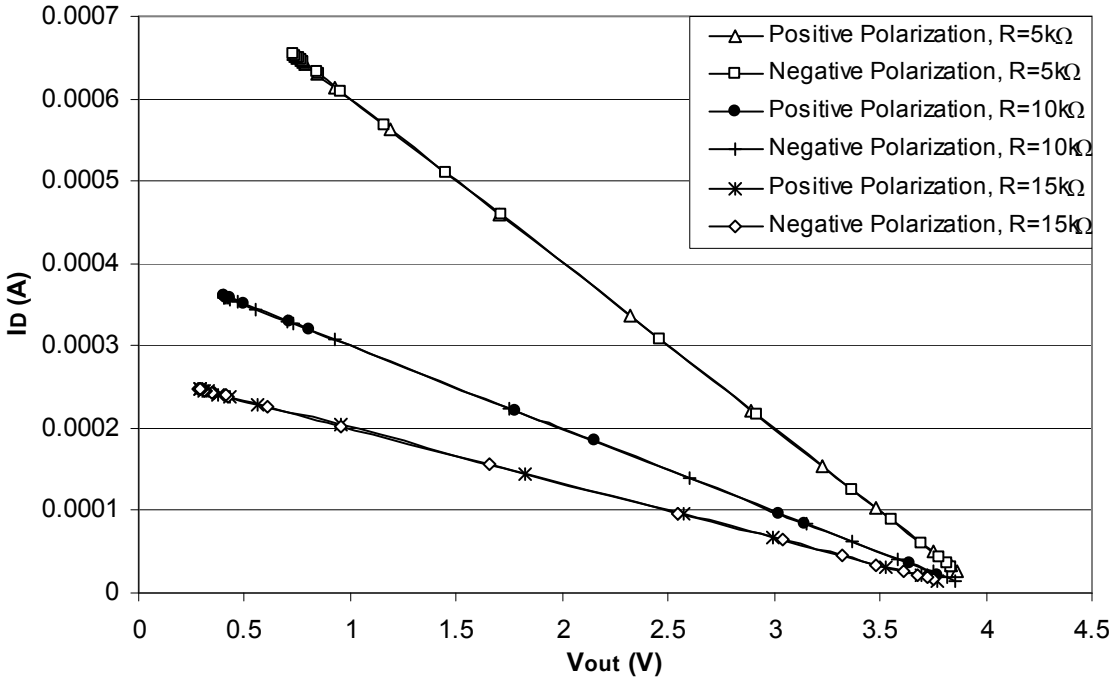

Figure 3.13 Plot of drain current vs. output voltage for $V_{DD} = 4V$

Again, the plot follows the expected trends. The relationship between I_D and V_{out} is linear, as shown in Equation (3.1). Also, as the resistance increases, the drain current decreases. Furthermore, the drain current decreases with increasing output voltage for all the resistance values. As shown in the plot, the type of polarization induced on the gate of the FeFET had no effect on the I_D-V_{out} relationship. This fact can be attributed to the absence of the gate voltage variable, V_{GS}, in the equation relating I_D and V_{out}. Finally, all the data lines of the plot tend toward the same value.

d. Quiescent Point Calculation

In MOSFET electronics, the quiescent point, Q, is the point on the I-V characteristic plot that is near the middle of the saturation portion of the curve. This point provides a good estimate of an effective biasing point for the transistor to ensure operation in the saturation region [1]. A similar definition was used in this study to determine the Q point for the FeFET-based CS amplifier. Using the I_D vs. V_{GS} curves, the effective biasing point, i.e., the best value for the dc offset voltage, was estimated to be the value for V_{GS} at which I_D is approximately equal to half of its average value for each case. So, for example, from Figure 3.12, the Q points under negative polarization are about -0.15V, -0.625V, and -1.12V for 5kΩ, 10kΩ, and 15kΩ load resistances, respectively. Several such measurements were taken for various values of V_{DD} and at different load resistances. An important similarity among all the measurements was the relative closeness of the estimated Q point to the empirical value for the offset voltage at which the most gain was achieved when the FeFET was negatively polarized. However, under positive polarization, the estimated value for the offset voltage was not as close to its empirically-derived value. Future work with the FeFET-based CS amplifier can determine the relationship between polarization and the accuracy of the Q point.

e. Power Dissipated by the FeFET in the CS Amplifier Configuration

The last parameter examined is the power dissipated by the FeFET, P_{diss}, in the CS amplifier configuration. Here, V_{DD} was 4V, v_{gs} was set to 0V, and the FeFET was positively and negatively polarized for each of the resistance values of 5kΩ, 10kΩ, and 15kΩ. At each value of V_{GS} tested, the power dissipated was calculated based on the following equation:

$$P_{diss} = I_D * V_{out}. \tag{3.3}$$

The plot of P_{diss} vs. V_{GS} is shown in Figure 3.14.

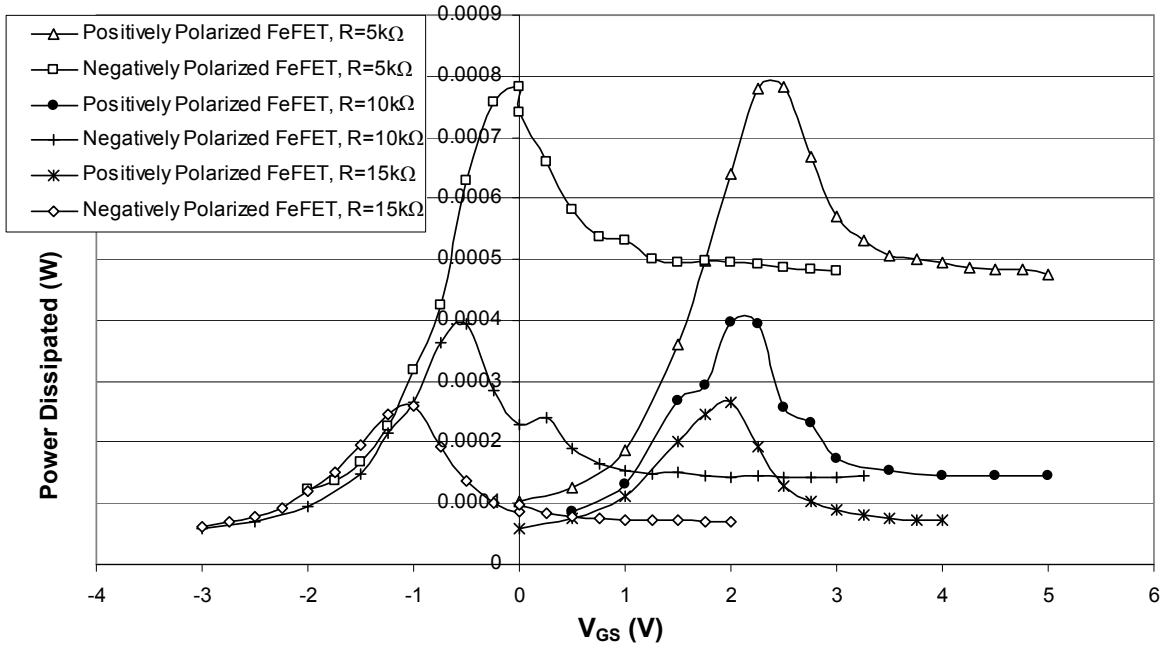

Figure 3.14 Plot of power dissipated vs. dc input voltage for V_{DD} = 4V

This plot shows that the relationship between power dissipated by the FeFET and the dc gate voltage exhibits a distinct trend. All curves have a similar shape and have a peak that occurs at or near the midpoint of V_{GS} for each case. For example, V_{GS} ranges from 0V to 5V for the 5kΩ case under positive polarization, so the peak of this curve should, and does, occur around V_{GS} = 2.5V. For almost all points, the power dissipated decreases with increasing resistance. This is due to the fact that the drain current decreases with increasing resistance, as was shown in Figure 3.12.

C. Comparison of the Voltage Gain and Phase Shift of the FeFET and MOSFET CS Amplifiers

As the most commonly used type of single-stage MOSFET amplifier, the CS amplifier is characterized by high gain [1]. Comparing the data obtained from the FeFET-based CD, CS, and CG amplifiers, it was found that the CS amplifier configuration provided the most gain. Table 3.1 below shows the values of the gain obtained from comparable CS and CG amplifier configurations at input frequencies ranging from 1Hz to 2.3MHz. For the tested CS amplifier circuit, V_{DD} was 4V, the amplitude of the input voltage was 1V, the offset voltage was 1.45V, and the load resistor was 10kΩ. The corresponding parameters in the CG amplifier circuit had the same values, except the offset voltage was 2V and the gate of the transistor was positively polarized with 6V.

Table 3.1 Comparison of voltage gain values of FeFET CS and CG amplifiers

Frequency	CS Amplifier Voltage Gain (V/V)	CG Amplifier Voltage Gain (V/V)
1Hz	2.23	1.979
10Hz	2.213	1.962
100Hz	2.201	1.945
1kHz	2.172	1.919
10kHz	2.092	1.873
100kHz	1.76	1.413
250kHz	1.03	0.727
500kHz	0.6	0.373
1MHz	0.29	0.192
2.3MHz	0.185	0.08

The table shows that the CS amplifier resulted in higher gain at every frequency value. Although the gain of the FeFET CS amplifier was not as high as its MOSFET counterpart, significant gain was achieved when V_{DD} was increased to 6V.

In a MOSFET CS amplifier with a limited supply voltage, high gain is achieved using a large load resistance [64]. However, examining the plot of Figure 3.10 showing the voltage gain vs. the logarithm of resistance for the FeFET CS amplifier, it can be seen that the highest gain was not achieved using the highest load resistance. A resistance range of 5kΩ to 250kΩ was examined, and the highest gain was achieved at 15kΩ or 30kΩ.

The MOSFET CS amplifier displays an inherent phase shift of 180°. Examining the phase shift vs. logarithm of frequency plots of the FeFET CS amplifier shows that at lower frequencies, this amplifier also has a phase shift magnitude of about 180°. At higher frequencies, the FeFET CS amplifier's phase shift tends toward 0°.

D. The Frequency Response

The frequency response of the FeFET CS amplifier differs drastically from that of its MOSFET counterpart. This great divergence is shown in the frequency response plot of Figure 3.15, where the voltage gain in decibels is plotted against the input frequency. The frequency ranges from 1Hz to 2.3MHz, which covers the low-, mid-, and high-frequency ranges. The plot looks like a reflection along the x-axis of the low- and mid-frequency response of the MOSFET CS amplifier. Instead of a logarithmic increase of the voltage gain at the low-frequency portion of the plot, as would be seen in the MOSFET amplifier, the FeFET amplifier’s frequency response shows a nearly linear decrease in gain. Moreover, the mid-frequency portion of the plot of Figure 3.15 does not display a constant value for the gain, unlike that of the MOSFET response. In fact, the mid-band portion of the plot of Figure 3.15 also shows an almost linear decrease in gain. At frequencies higher than 1MHz, the gain decreases at a slower rate; however, due to the

function generator's frequency limit, data could not be collected at frequency values over 2.3MHz. Future work on the FeFET CS amplifier can focus on the very high-frequency response of the amplifier in order to determine the frequency value at which the voltage gain levels off.

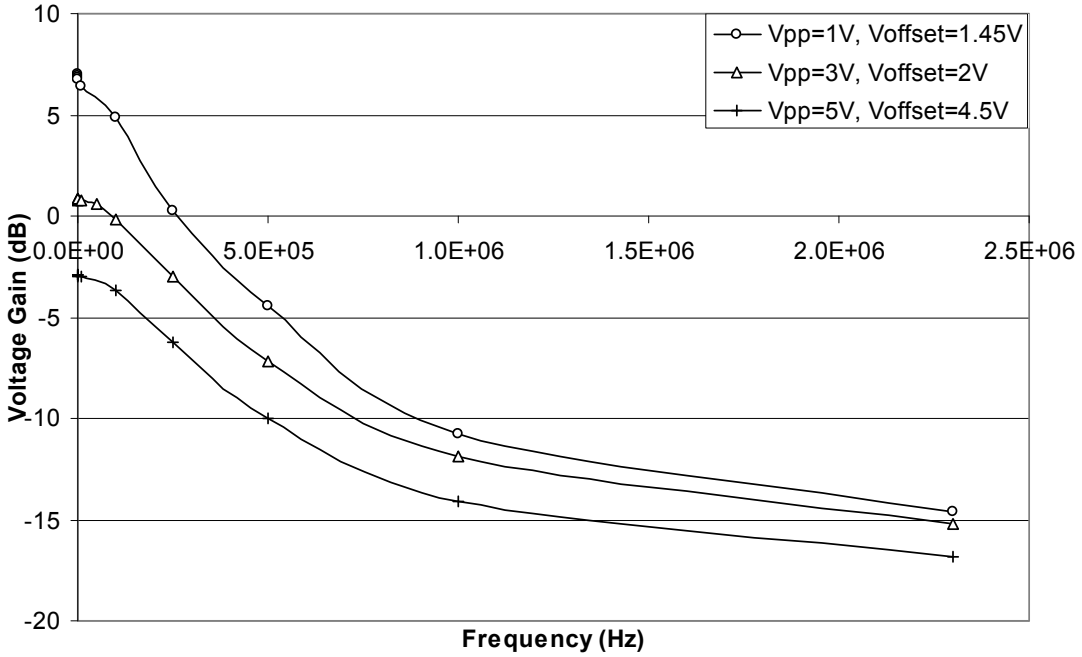

Figure 3.15 FeFET CS amplifier frequency response

E. Conclusion of Experimental Results

The FeFET CS amplifier displays numerous unique characteristics that can have many useful applications. The first interesting observation is the logarithmic relationship between the phase shift and each of the low and high frequency ranges and between the voltage gain and these frequency ranges. Also, the nearly perfectly logarithmic relationship between the phase difference and the load resistance and unique shape of the voltage gain vs. logarithm of resistance plots are all distinct characteristics of the FeFET

CS amplifier. The hysteretic relationship describing the output voltage vs. dc input voltage and the drain current vs. dc input voltage is not seen in this amplifier's MOSFET counterpart. Another interesting characteristic of this amplifier is the almost perfectly linear relationship between the drain current and the output voltage. Furthermore, the distinct shape of the curves relating the power dissipated by the amplifier to its dc input voltage may prove to be of use in certain circuit configurations. The difference between the FeFET CS amplifier's frequency response and that of the MOSFET CS amplifier may shed more light on the physical operation of the FeFET in this amplifier configuration. Future work can focus on the operation of the FeFET CS amplifier with different types of loads, including a MOSFET load and a FeFET load.

F. Nonquasi-Static FeFET CS Amplifier Model

The physically-derived NQS MATLAB® model created to simulate the behavior of the FeFET CD amplifier was altered to model the FeFET CS amplifier. All the physics-based equations given by Equations (2.1) through (2.29) that describe the ferroelectric transistor operation still apply. The drain current is determined by substituting Equations (2.24)-(2.29) into Equation (2.23). However, in order to reflect the change in the circuit configuration, the output voltage is found using voltage division on the load resistance and the FeFET's equivalent resistance (RQ), which is estimated by dividing V_{DD} by the calculated drain current. Thus, V_{out} is given by

$$V_{out} = V_{DD} \frac{RQ}{RQ + R}. \tag{3.4}$$

a. Simulation Steps

The FeFET CS amplifier was simulated in MATLAB® as described in the following simulation steps. A flowchart of the detailed simulation steps is shown in Figure 3.16.

1. Enter fabrication parameters (L, W, N_A, t_f, μ, etc.), simulation time interval, amplifier parameters (V_{DD}, input frequency, amplitude of input signal, load resistance, etc.), dc terminal voltages (V_D, V_G, V_S, and V_B), and number of channel partitions (N).
2. Define the sinusoidal input signals v_{gs} and v_{gb} using the amplifier parameters entered and the current time step.
3. Rewrite the input signals using their phasor representations.
4. Calculate the surface potential at the source ($\psi_{s0}(t)$) and the surface potential at the drain ($\psi_{sL}(t)$) using Newton's method.
5. For each channel partition, calculate the surface potential at both edges of the partition using Newton's method. Then, determine the surface potential across the partition by averaging the potentials at the edges and plugging this value into Equation (2.13) to obtain the most accurate surface potential value.
6. Propagate through a function for polarization and electric field calculations for each partition based on Equations (2.14)-(2.21).
7. Calculate the total ferroelectric charge per unit area, q'_F, by summing each partition's polarization and dividing by the number of partitions.
8. Determine the threshold voltage using Equation (2.22).

9. Use the y-parameter model to calculate the drain current as described in Equations (2.23)-(2.29).
10. Determine an initial value for the FeFET's equivalent resistance, RQ, by dividing V_{DD} by the calculated drain current.
11. Multiply RQ by a scaling factor.
12. Determine an initial value for the output voltage, V_{out}, using voltage division on the load resistance and the scaled RQ, as shown in Equation (3.4).
13. Multiply V_{out} by a scaling factor.
14. Update the value of the drain current using Equation (2.23) with V_{ds} being replaced with the value for V_{out} just calculated.
15. Multiply RQ by the same scaling factor used earlier for the initial value of RQ.
16. Recalculate V_{out} using voltage division on the last RQ value and the load resistance.
17. Multiply V_{out} by the same scaling factor used earlier for the initial value of V_{out}.
18. Increment the simulation time by one time step.
19. If the incremented time is less than or equal to the final time step, go to Step 4. Otherwise, plot the output voltage with respect to ωt.

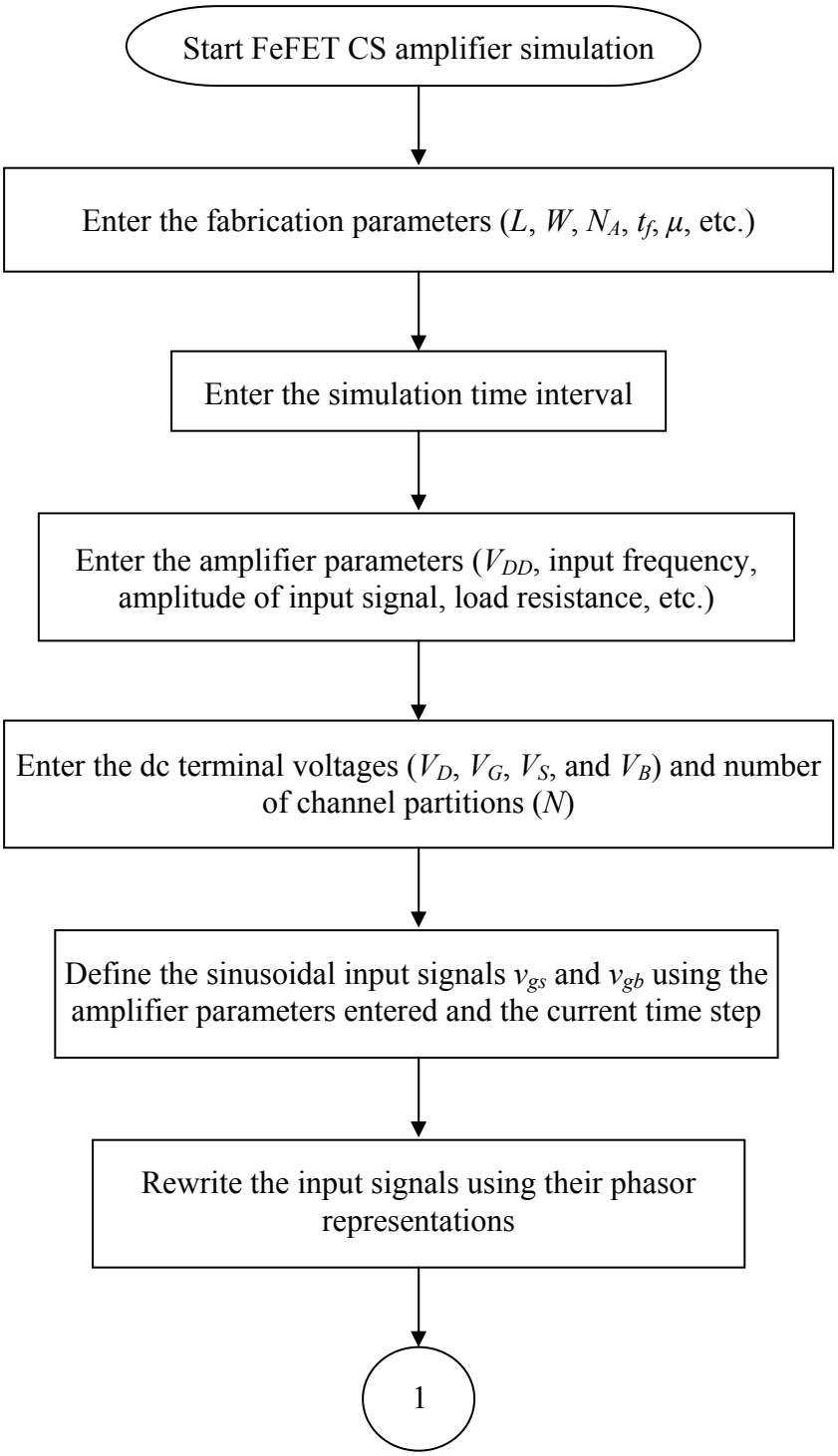

Figure 3.16 FeFET CS amplifier simulation steps

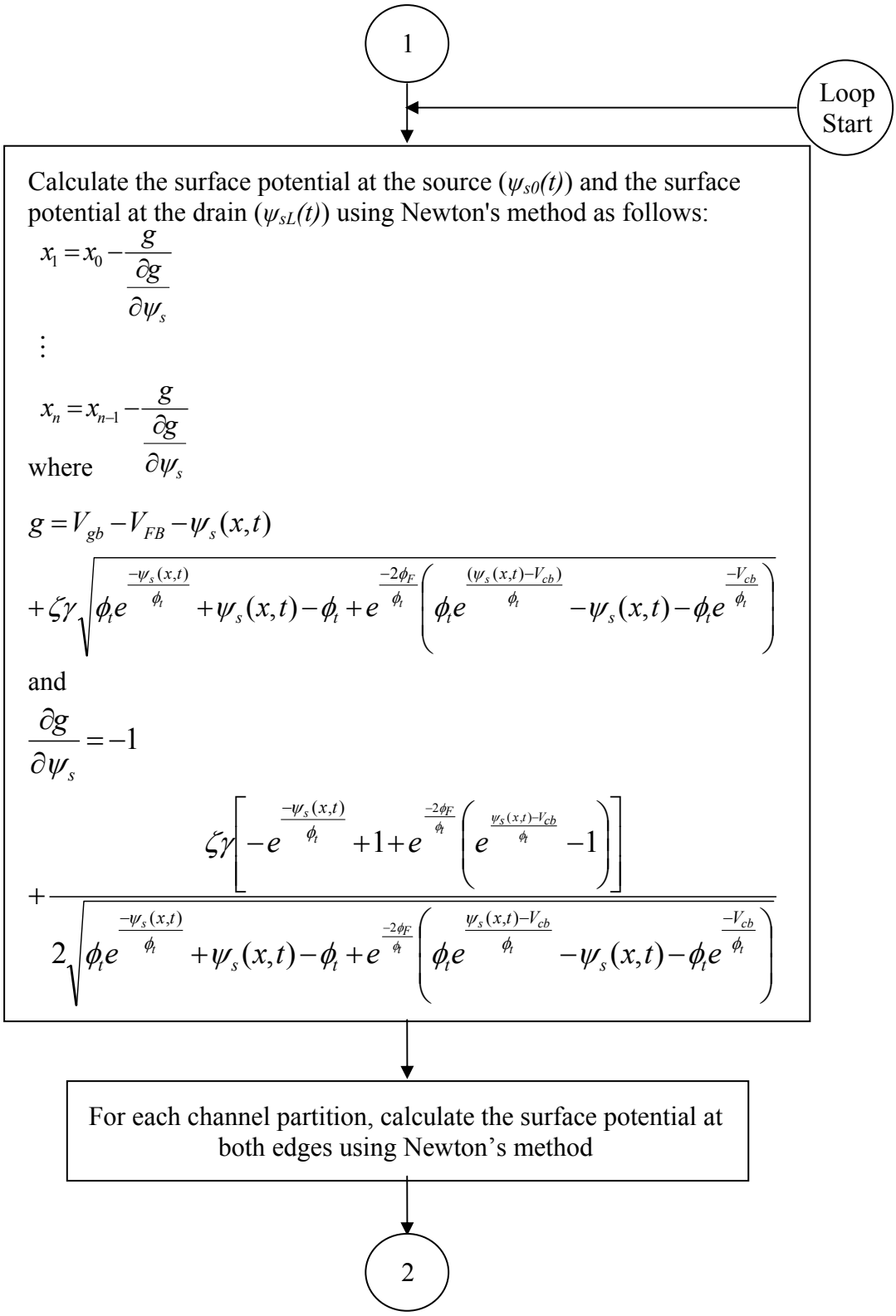

Figure 3.16 FeFET CS amplifier simulation steps (continued)

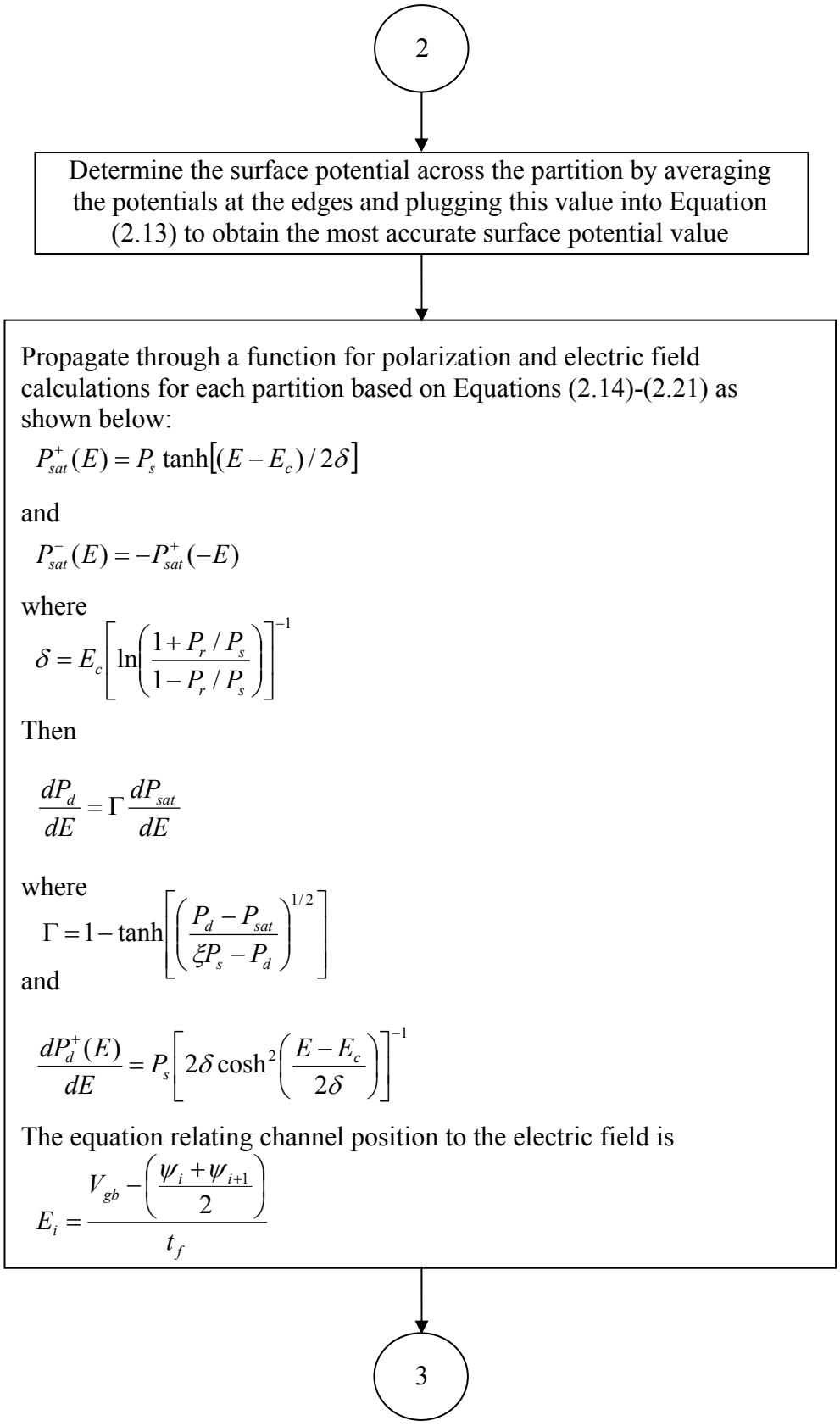

Figure 3.16 FeFET CS amplifier simulation steps (continued)

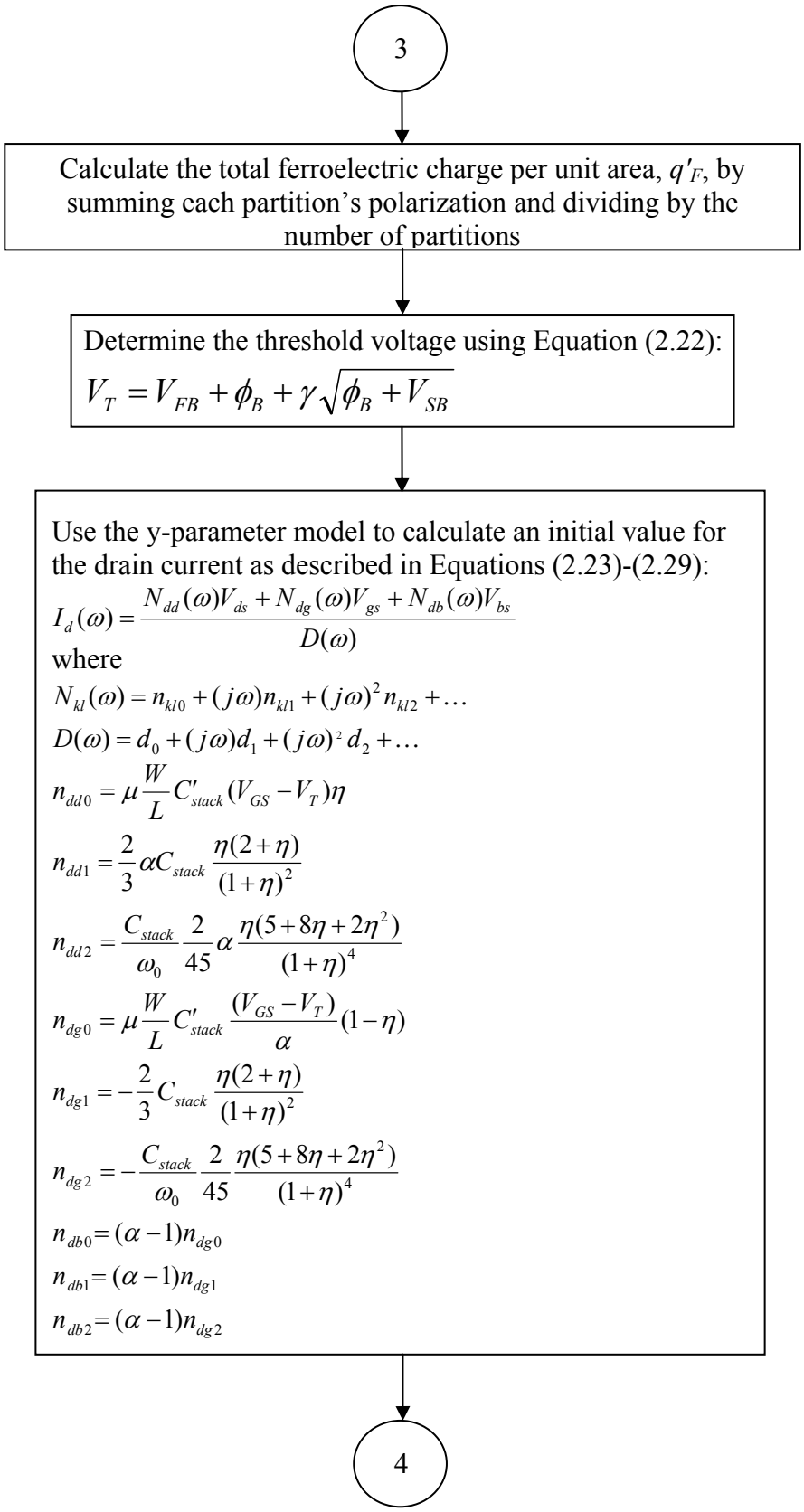

Figure 3.16 FeFET CS amplifier simulation steps (continued)

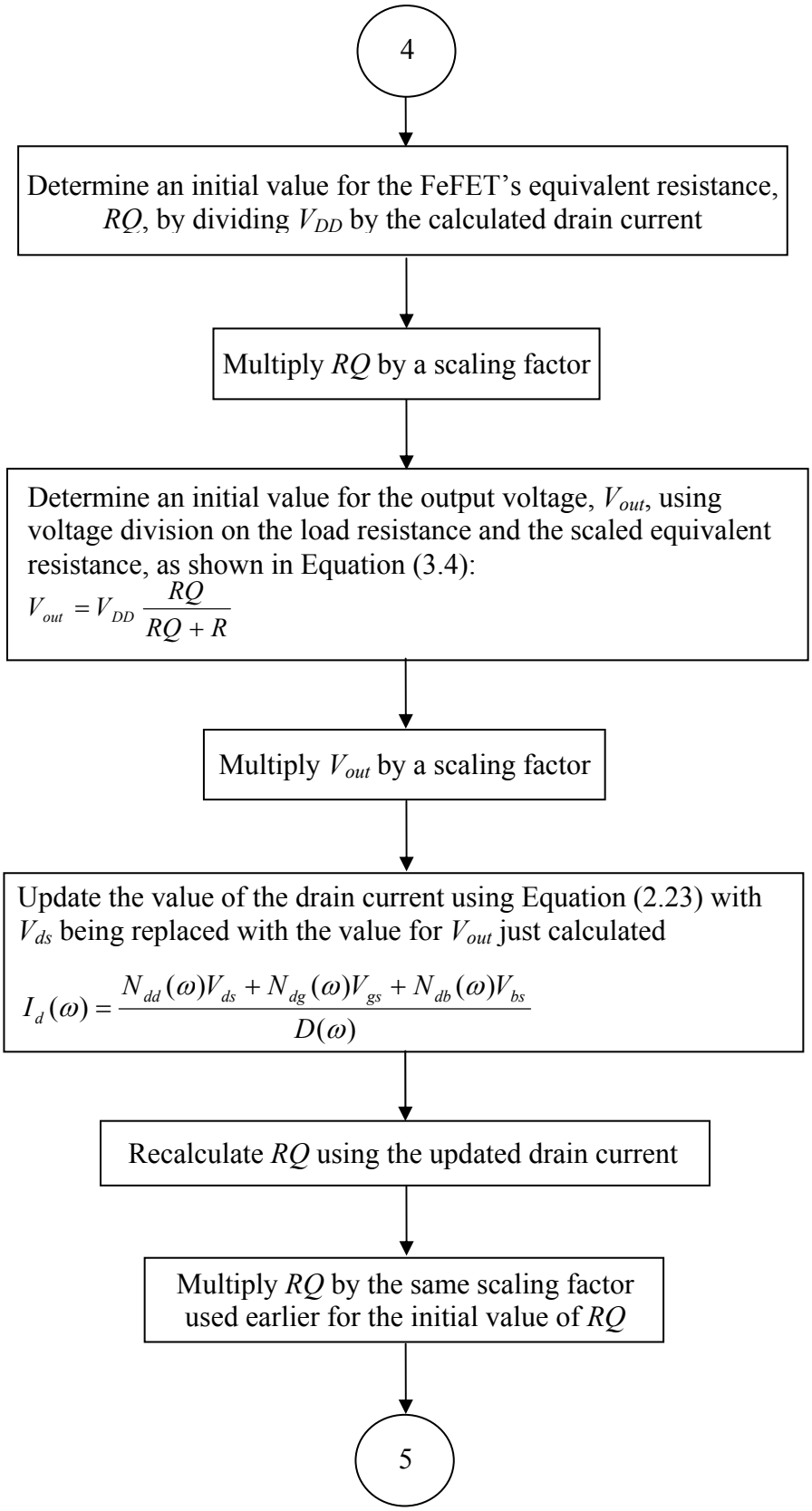

Figure 3.16 FeFET CS amplifier simulation steps (continued)

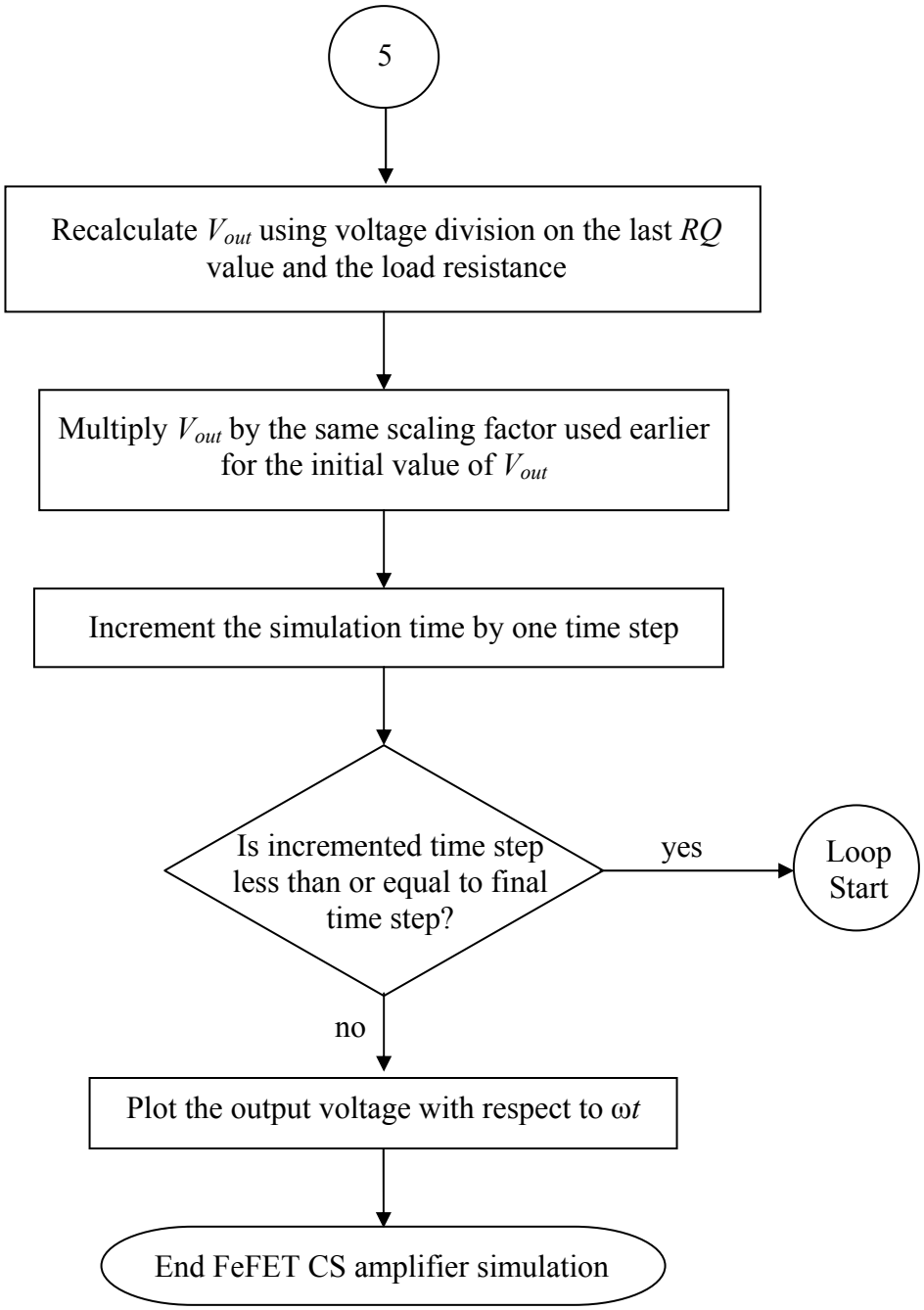

Figure 3.16 FeFET CS amplifier simulation steps (continued)

b. Model Results

Two test cases were carried out to corroborate the model's accuracy and efficiency with empirical results. Given the user-defined parameters, the model calculates the output voltage as described above and plots the input and output signals (denoted by V_{in} and V_{out} on the plots) with respect to ωt. In the first test case, V_{DD} was set to 3.9V, the amplitude of the input signal was 2.5V, an offset voltage of 4.5V was added, the input frequency was 1MHz, and the load resistance was 10kΩ. *RQ*'s scaling factor was selected to be 1.9×10^2, and the output voltage's scaling factor was 3. The oscilloscope output of this test case is shown in Figure 3.17, and the modeled output is given in Figure 3.18.

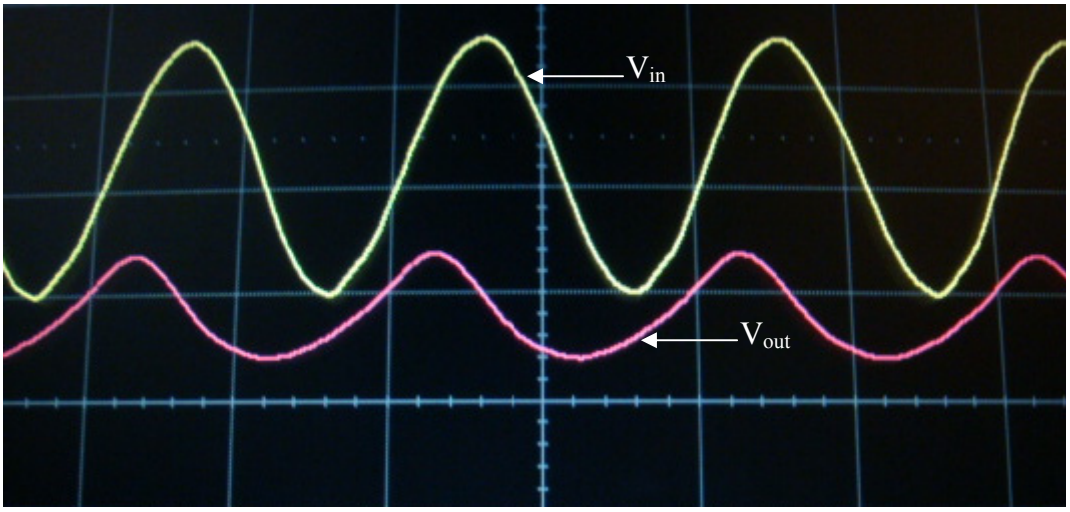

Figure 3.17 Oscilloscope output for the first test case with a scale of 2V per division for V_{in} and 1V per division for V_{out}

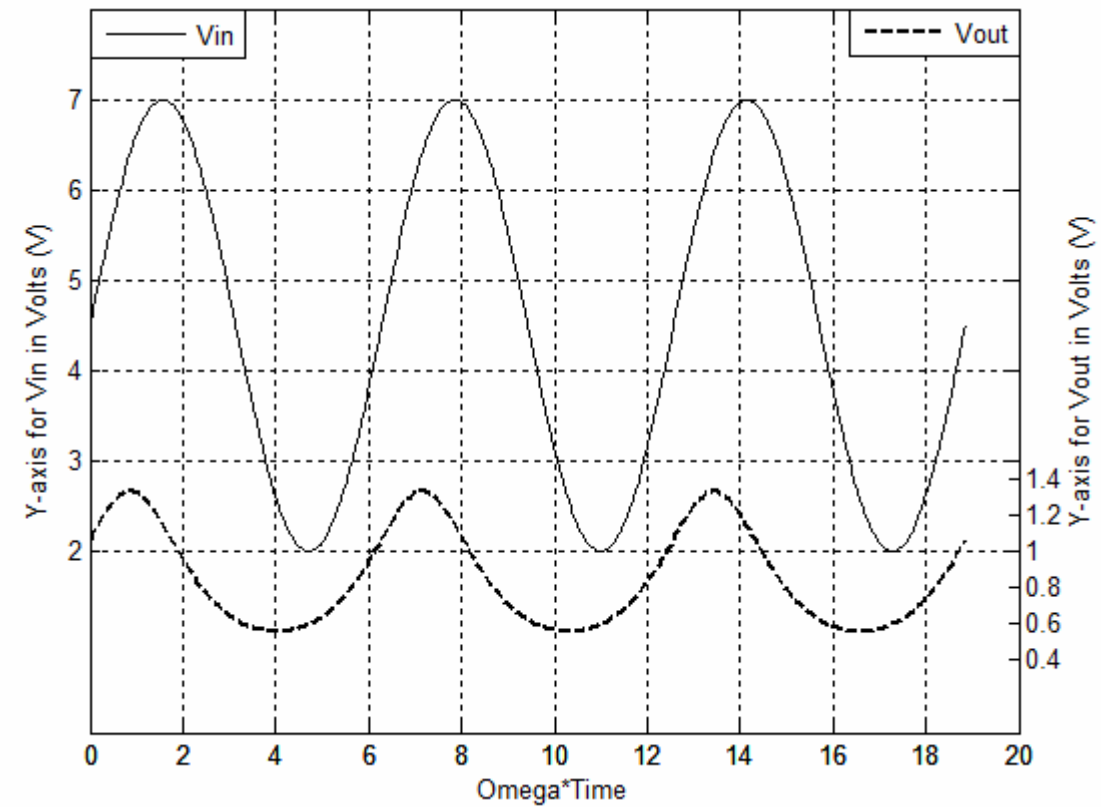

Figure 3.18 Modeled output for the first test case

Comparing the modeled plot with the oscilloscope plot shows that the model produces a voltage plot that is very similar in shape and value to the oscilloscope output. The modeled output voltage plot displays the same characteristics as the oscilloscope plot as is shown by the wide troughs and narrow peaks of the V_{out} line. In all the modeled CS amplifier plots, it was noticed that the modeled output signal had an inherent phase shift of around -90°, so the value of the phase shift parameter of the modeled input signal was adjusted accordingly in order to produce a phase difference that is similar to that of the oscilloscope plot. The maximum and minimum values of the simulated output voltage signal and the oscilloscope output signal for the two test cases are given in Table 3.2. Examining the table shows the closeness of the simulation and oscilloscope results.

For the second test case, V_{DD} was increased to 6V, the input amplitude was lowered to 1V, the offset voltage was 0.9V, the frequency was set to 2.3MHz, the load resistance was 10kΩ, *RQ*'s scaling factor was 3.6×10^3, and the output voltage's scaling factor was 0.42. Figures 3.19 and 3.20 show the oscilloscope and modeled plots, respectively.

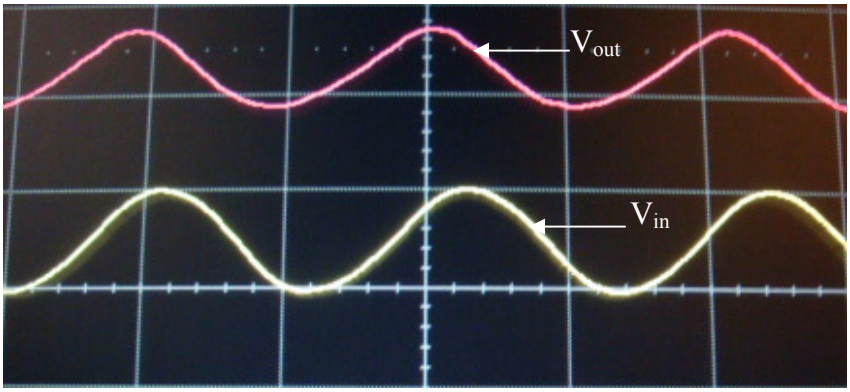

Figure 3.19 Oscilloscope output for the second test case with a scale of 2V per division for V_{in} and 1V per division for V_{out}

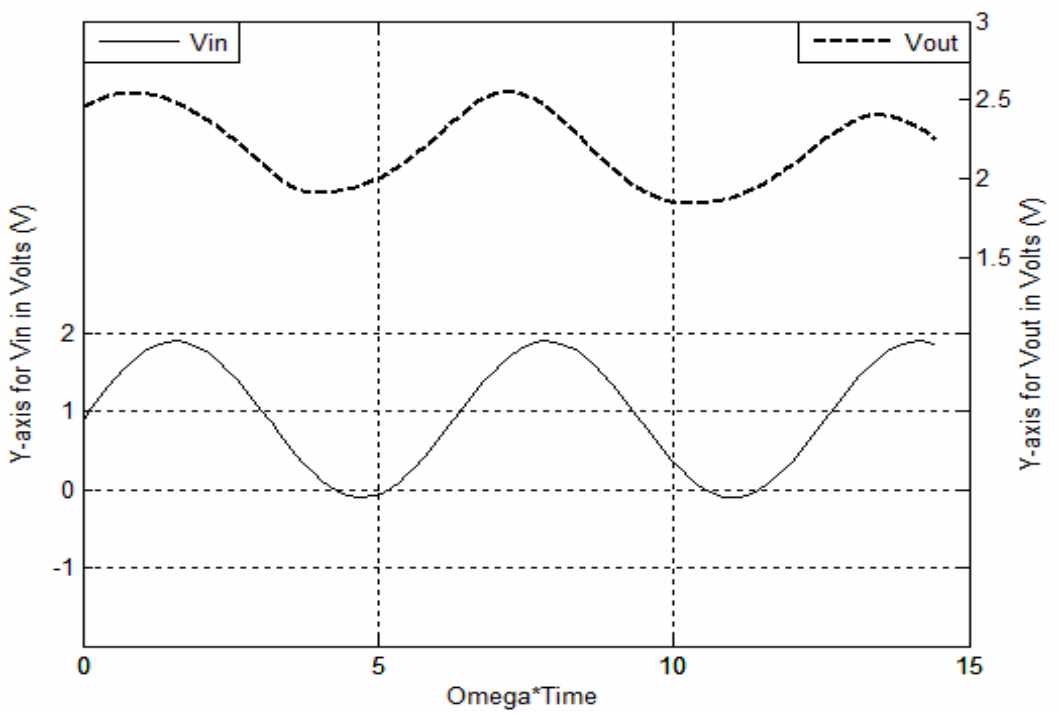

Figure 3.20 Modeled output for the second test case

As was noted in one of the FeFET CD amplifier test cases, fluctuations in ferroelectric polarization resulted in drain current, and therefore output voltage, fluctuations early in the plot. However, these instabilities were smoothed out as the polarization reached a stable value a few seconds later. Despite these fluctuations, the oscilloscope and modeled plots are clearly similar in both shape and values. When the polarization stabilized, the values and shape of the modeled output voltage signal were very close to those of the oscilloscope plot. The test cases clearly depict the accuracy and efficiency of the model. Table 3.2 further proves the accuracy of the simulation results.

Table 3.2 Oscilloscope and simulation results for FeFET CS amplifier

	Test Case I		Test Case II	
	Max. value	Min. value	Max. value	Min. value
Oscilloscope Results	1.37	0.387	2.35	1.927
Simulation Results	1.334	0.559	2.349	1.814

G. Conclusion of Modeled Data Analysis

Due to the model's versatility and ease of use, the physics-based NQS model created for the FeFET CD amplifier has been easily altered to describe the behavior of the FeFET CS amplifier. The modeled plots showed great similarity to the oscilloscope plots in both shape and measurements. As with the FeFET CD amplifier, the model's efficiency and physical accuracy has been displayed.

CHAPTER IV

CHARACTERIZATION AND MODELING OF THE FeFET COMMON-GATE AMPLIFIER

The remaining basic amplifier configuration, the CG amplifier, was examined using ferroelectric technology. The basic characteristics of the FeFET CG amplifier were noted and discussed. Also, a model was developed in MATLAB® to simulate this amplifier's behavior based on its physical and empirical characteristics.

A. Basic Structure

Similar to the FeFET CS amplifier, the FeFET CG amplifier is built using a FeFET and a resistor. However, the CG amplifier configuration, shown in Figure 4.1, requires the ac input voltage, v_{in}, to be provided at the source, while the dc biasing voltage, V_{bias}, is provided at the gate of the FeFET. The output voltage, v_{out}, is again taken at the drain. A load resistor, R, is connected to the drain of the transistor. V_{DD} is the voltage from the drain of the transistor, above R, to ground.

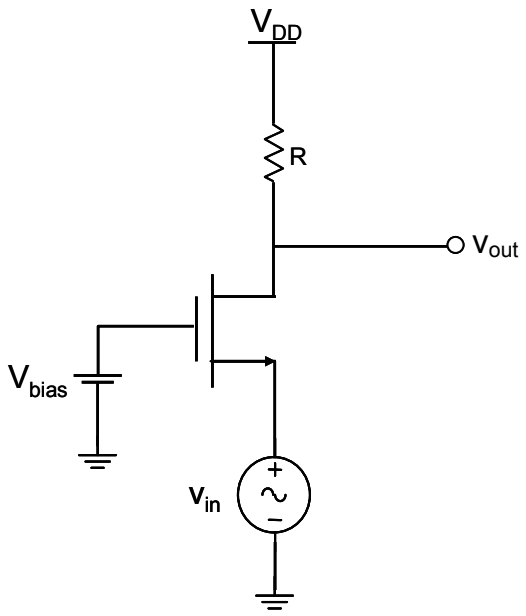

Figure 4.1 FeFET common-gate amplifier circuit configuration

B. Empirical Measurements of the FeFET CG Amplifier

As with the two previous amplifiers, the effect of the frequency of the input signal on each of the phase shift of the output signal, output voltage, and voltage gain was examined. The relationship between the load resistance and each of these three parameters was also studied. Furthermore, the effect of applying a polarization voltage to the gate on the voltage gain was analyzed.

a. Effect of Frequency on Phase Shift, Output Voltage, and Voltage Gain

The effect of the input frequency on the phase shift of the output signal was the first relationship examined. Excepting the amplitude of the input signal and its offset, all parameters were held constant. Thus, V_{DD} was set to 6V and the load resistance was held at 10kΩ. The gate of the FeFET was negatively polarized by applying a negative polarization voltage $V_{p,neg}$ of -6V. The phase shift of the output signal was measured at

input frequencies of 1, 10, 100, 1k, 10k, 50k, 100k, 250k, 500k, and 1MHz for V_{in} of 1V with V_{bias} of -2V, -1V, and no V_{bias}, and for V_{in} of 4V with V_{bias} of -1V and -0.5V. For the CG amplifier measurements, V_{in} is the peak-to-peak value of the input signal v_{in}. The amplitude and offset of the input signal were chosen to ensure that the peak-to-peak value of the input voltage does not exceed 8V so as not to rupture the gate. The degree values of the phase shifts were plotted against the logarithm of frequency, as shown in Figure 4.2. As aforementioned, negative values of phase shift indicate that the output signal is lagging the input signal, whereas positive values of phase shift mean that the output signal is leading the input signal. Also, all logarithms in these measurements are of base 10.

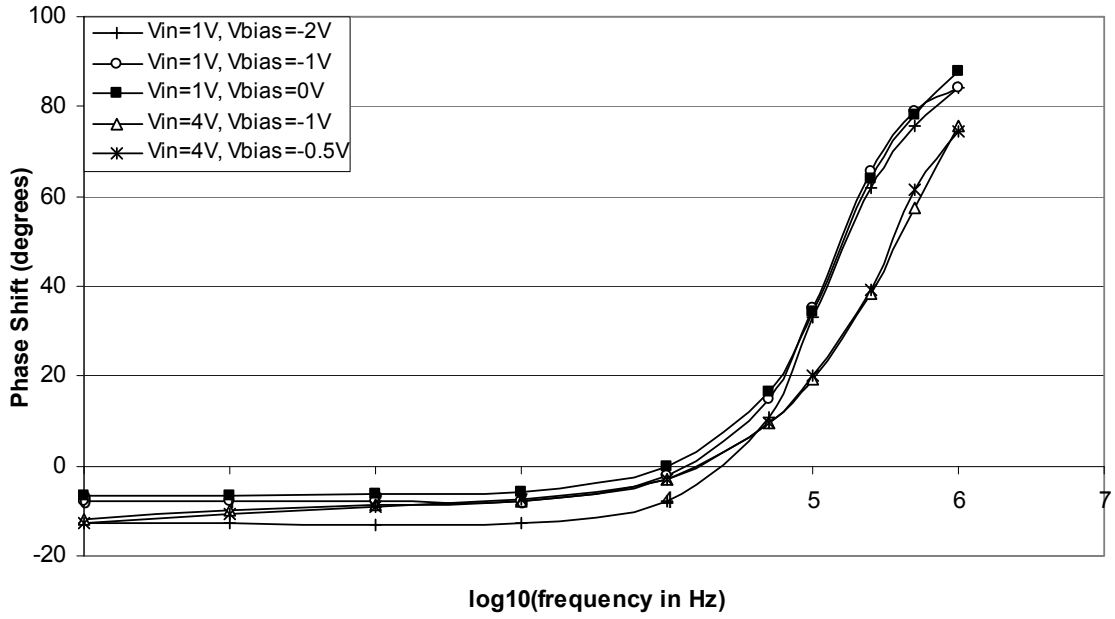

Figure 4.2 Plot of phase shift vs. logarithm of frequency for five input signals

The plot of Figure 4.2 shows that for all input signals, the relationship between the phase shift and frequency follows a similar trend. For input frequencies whose logarithm is less than or equal to four, the phase shift is linearly related to the logarithm of

frequency; therefore, the phase shift and input frequency are logarithmically related. The same relationship is observed for data points at frequency values whose logarithm is higher than four. The linear relationships between the phase shift and logarithm of frequency, the trend lines that best fit them, and the equations describing these trend lines are shown in Figure 4.3.

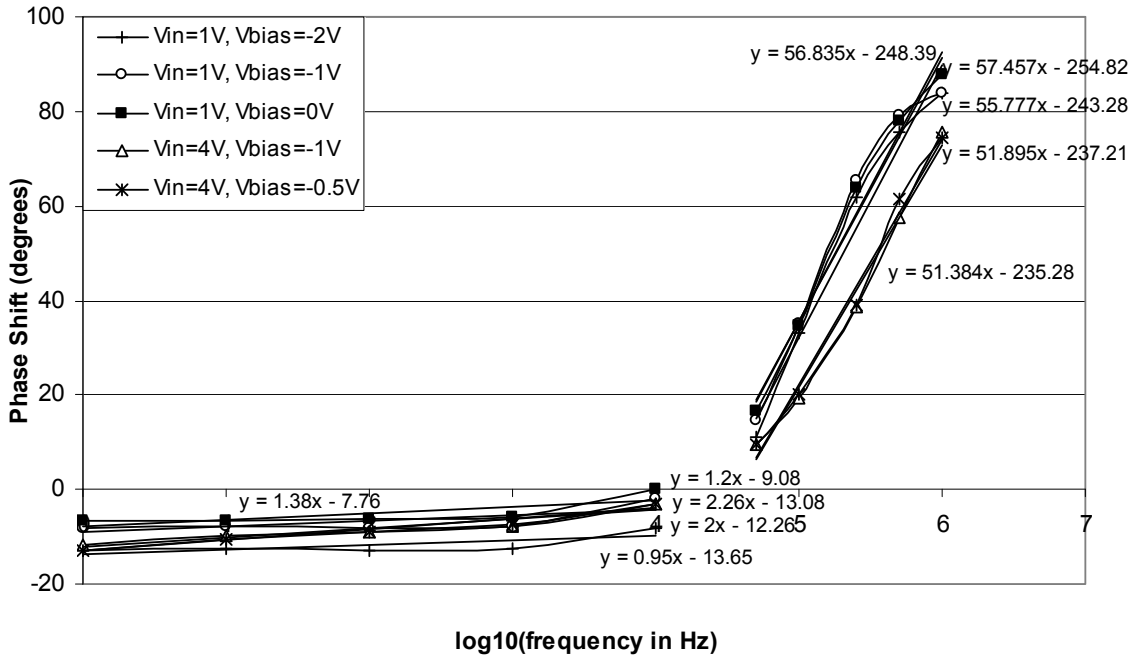

Figure 4.3 Plot of phase shift vs. logarithm of frequency for five input signals with trend lines

As can be seen from the plot, the data lines for frequencies at or below 10kHz are very similar and have almost parallel trend lines. For the higher frequencies, the trend lines fitting the data lines are also nearly parallel. Examining the data points at the higher frequencies, it is noted that the higher the magnitude of the biasing voltage, the lower the phase difference between the input and output signals.

The next relationship examined was the effect of frequency on the output voltage. Again, all parameters were kept constant so as to independently determine this relationship. The peak-to-peak value of the output signal was measured at the aforementioned input frequencies and at 2.3MHz. Figure 4.4 depicts the plot of the peak-to-peak output voltage vs. the logarithm of frequency.

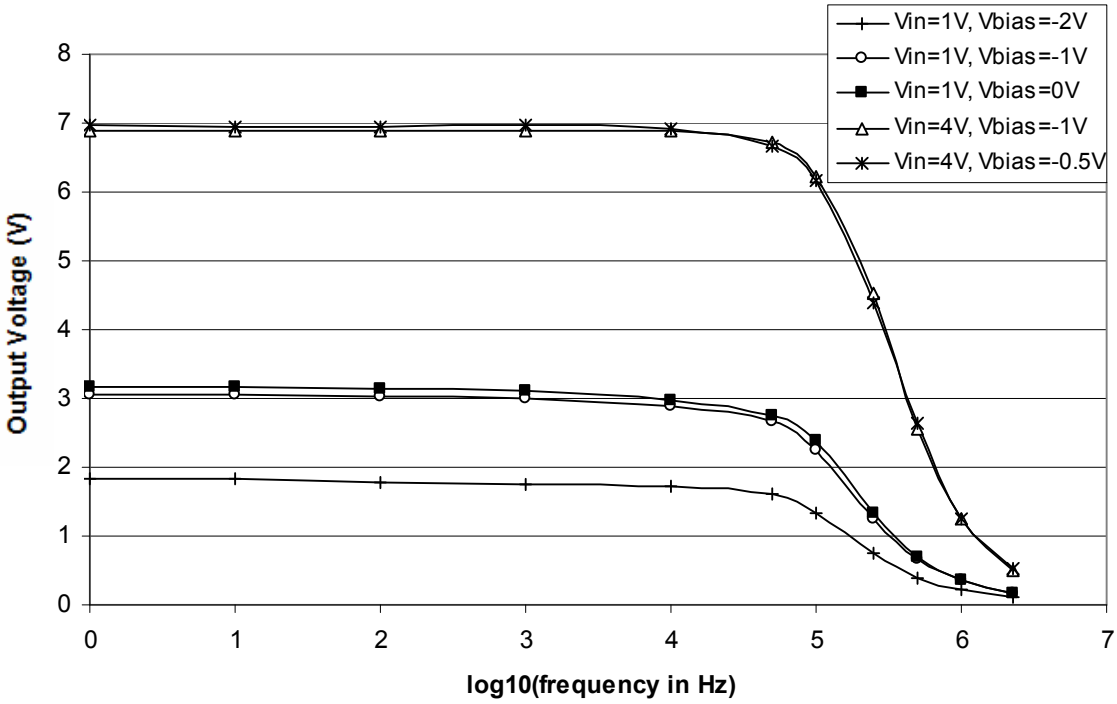

Figure 4.4 Plot of output voltage vs. logarithm of frequency for five input signals

Several characteristics are noted from examining the plot of Figure 4.4. First, the output voltage increases with an increase in the amplitude of the input voltage. Moreover, the output voltage increases as the biasing voltage becomes less negative. As was noted in the phase shift plots, the relationship between the input frequency and the output voltage for frequencies at or below 10kHz is nearly linear. The same holds true for frequencies of 50kHz and higher. Another observation is that the all the data lines for V_{in} of 1V tend

toward one value and the data lines for V_{in} of 4V level off to another value at very high frequencies. It is apparent that at frequencies higher than 2.3MHz, the amplitude of the output voltage tends to level off. Figure 4.5 shows the output voltage vs. logarithm of frequency plot with the linear trend lines and their governing equations. This figure shows that for frequencies up to 10kHz, all the trend lines are nearly horizontal and very closely fit the actual data lines. At the higher frequencies, the trend lines are linear.

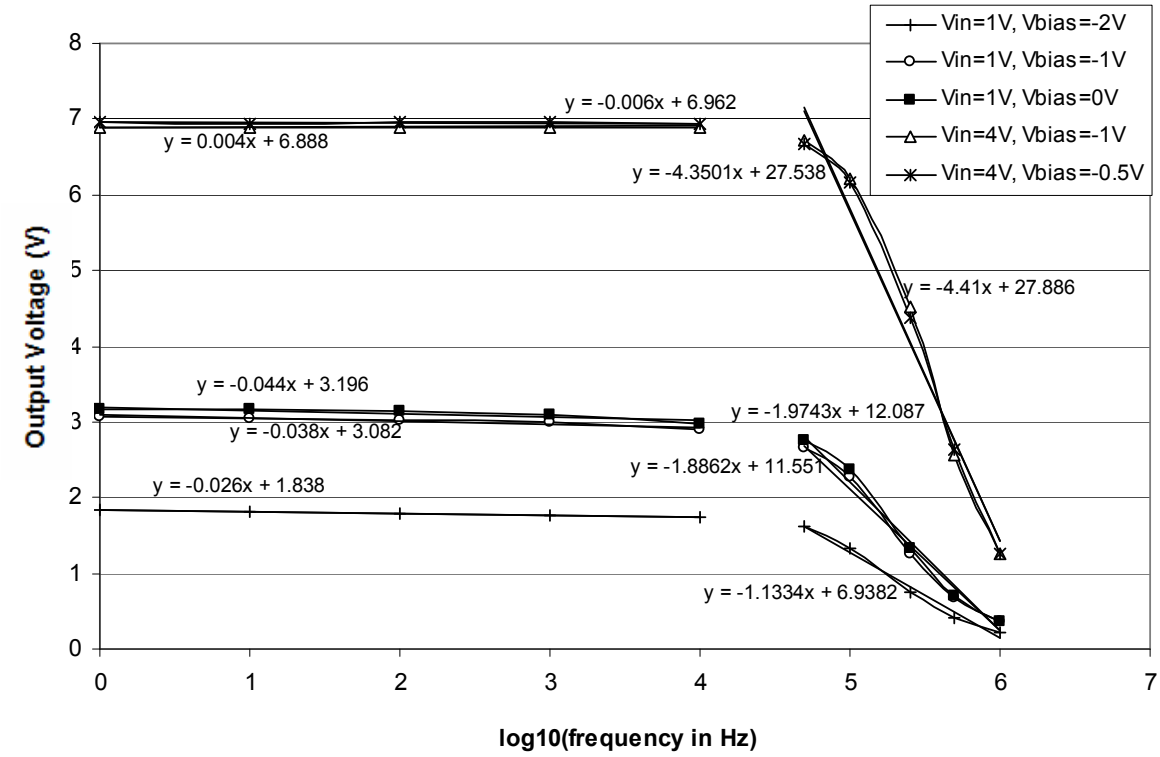

Figure 4.5 Plot of output voltage vs. logarithm of frequency for five input signals with trend lines

Lastly, the effect of the input frequency on the voltage gain was examined. Again, all parameters remained constant while the frequency was varied in the range previously used. The plot of Figure 4.6 shows the voltage gain in V/V vs. the logarithm of frequency.

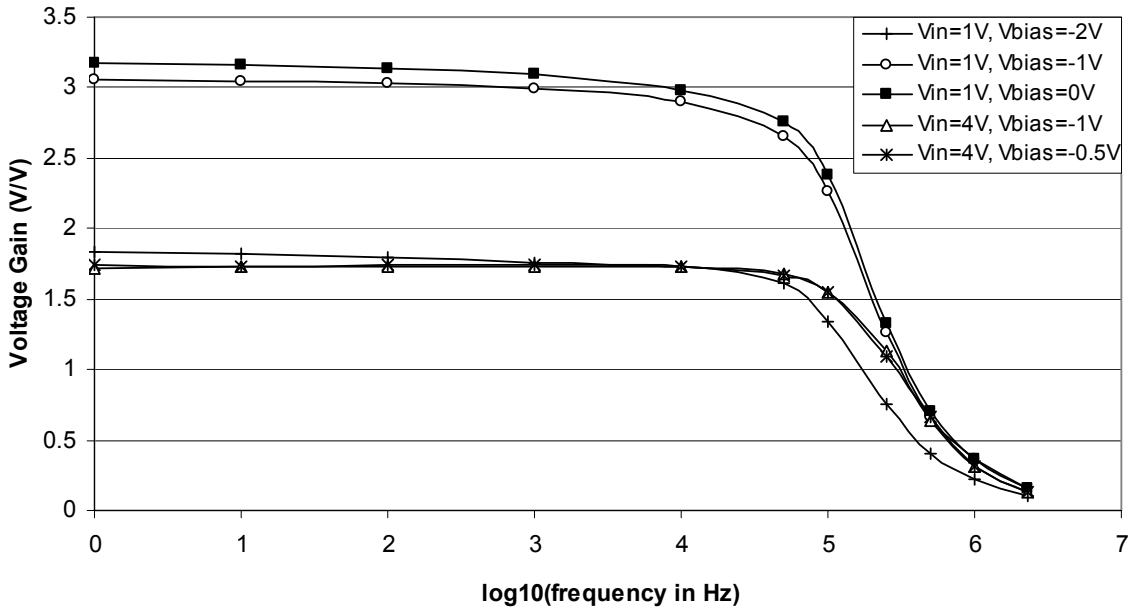

Figure 4.6 Plot of voltage gain vs. logarithm of frequency for five input signals

The voltage gain plot is similar in shape to the output voltage plot since the voltage gain is the amplitude of the output signal divided by the amplitude of the input signal. The leveling-off effect of the voltage gain at high frequencies is also seen in this plot; however, all the data lines tend toward a single value rather than a value for each data line, as was seen in the output voltage plot. Moreover, the data lines' trend lines, which are shown in Figure 4.7, illustrate the linearity of the voltage gain-logarithm of frequency relationship displayed in this amplifier. However, a significant difference between the output voltage plot and the voltage gain plot is that the voltage gain is lower for higher input voltages. This is due to the fact that the voltage gain is the output voltage divided by the ac input voltage without the biasing voltage.

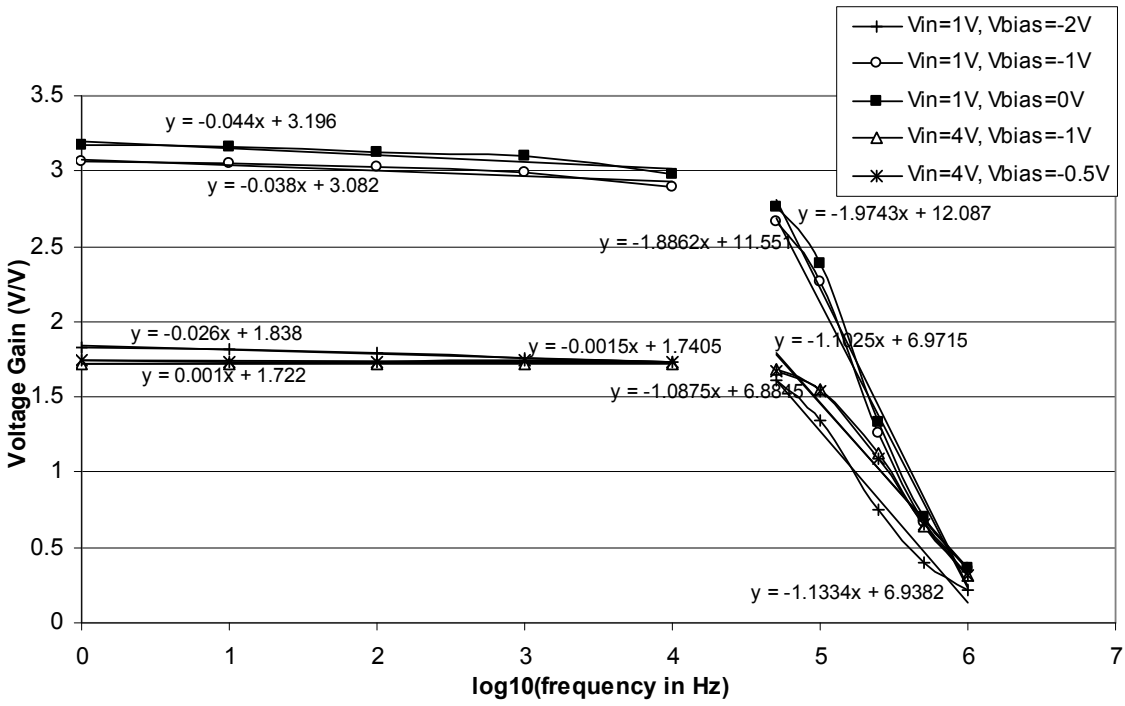

Figure 4.7 Plot of voltage gain vs. logarithm of frequency for five input signals with trend lines

b. Effect of Load Resistance on Phase Shift, Output Voltage, and Voltage Gain

The effect of altering the load resistance on the phase shift, output voltage, and voltage gain was next examined. At three different input frequencies, 100Hz, 1kHz, and 10kHz, the load resistance was varied from 5kΩ to 250kΩ. V_{DD} was set to 4V, the peak-to-peak input voltage was 2V, and a positive polarization voltage $V_{p,pos}$ of 6V was applied at the gate. The biasing voltage at each frequency was chosen to obtain the highest voltage gain. Thus, V_{bias} was 1V, 2V, and 1.5V for the data at 100Hz, 1kHz, and 10kHz, respectively. Figure 4.8 shows the plot of the phase shift vs. the logarithm of resistance.

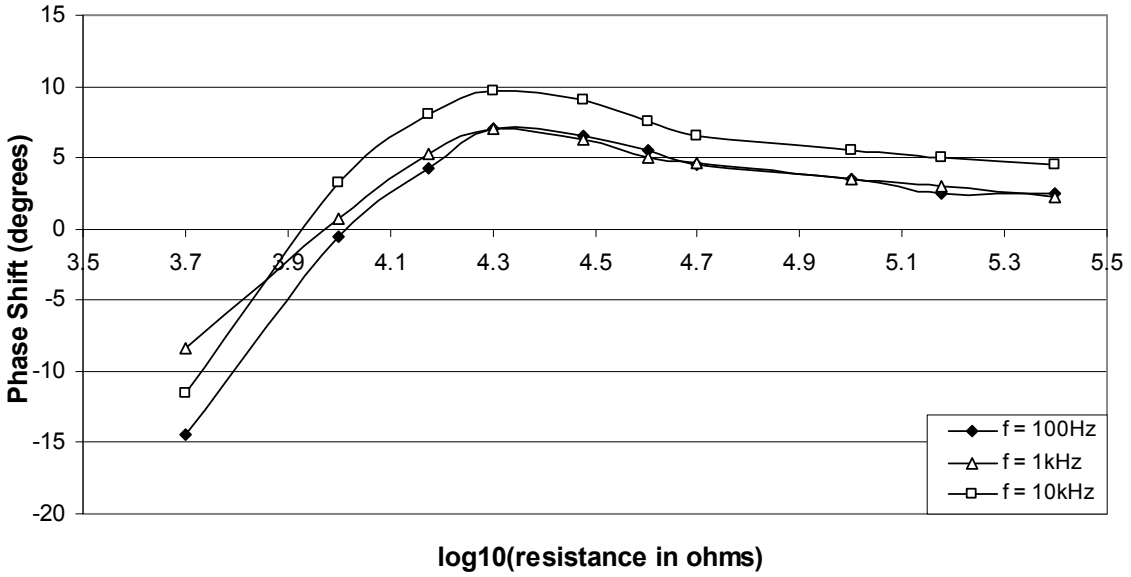

Figure 4.8 Plot of phase shift vs. logarithm of resistance for three frequencies

As can be seen from the plot, the relationship between the phase shift and the logarithm of resistance follows a characteristic trend and all the data lines are similar in shape. At most of the resistance values, the phase shift increases with an increase in the input frequency. Next, the output voltage was plotted against the logarithm of resistance as shown in Figure 4.9.

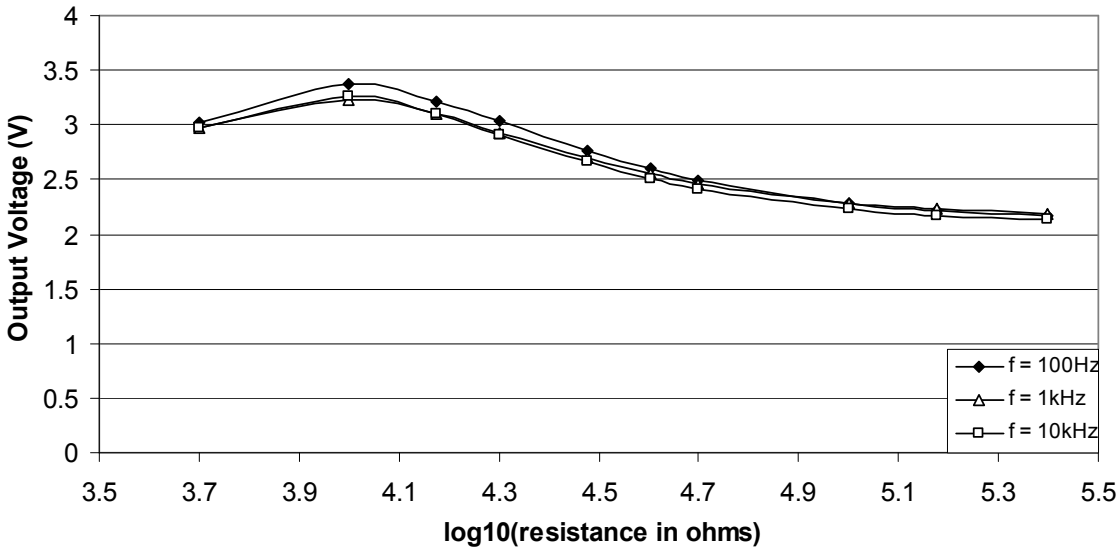

Figure 4.9 Plot of output voltage vs. logarithm of resistance for three frequencies

Again, all the data lines display a unique trend and are very similar. In this plot, the output voltage increases as the input frequency decreases. This is seen in the voltage gain plot of Figure 4.10, which is the same as the output voltage plot but with values divided by the input voltage of 2V.

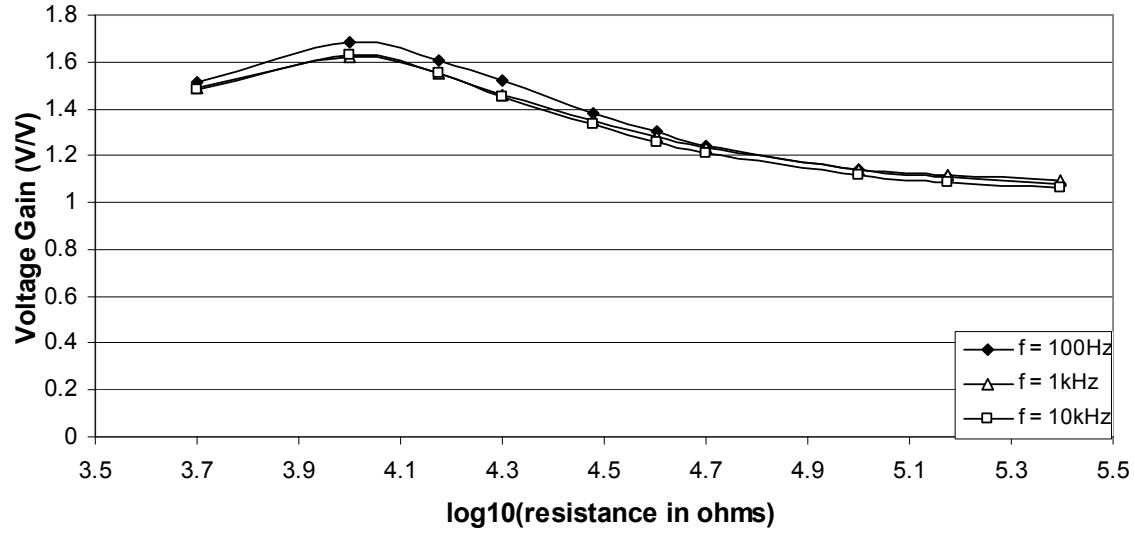

Figure 4.10 Plot of voltage gain vs. logarithm of resistance for three frequencies

c. Effect of Polarization on Voltage Gain

Another aspect of the FeFET CG amplifier studied was the effect of polarization on the voltage gain. For this analysis, data was collected with no applied polarization voltage and with positive or negative polarization voltage. Then, the voltage gain was compared. For the data in Figure 4.11, V_{DD} was set to 2V, V_{in} was 1V, V_{bias} was 0V, and the load resistance was 10kΩ. The voltage gain was measured when no polarization voltage was applied and when a negative polarization voltage, $V_{p,neg}$, of -6V was applied at the gate. The same was done for V_{bias} of -2V, and this data is shown in Figure 4.12.

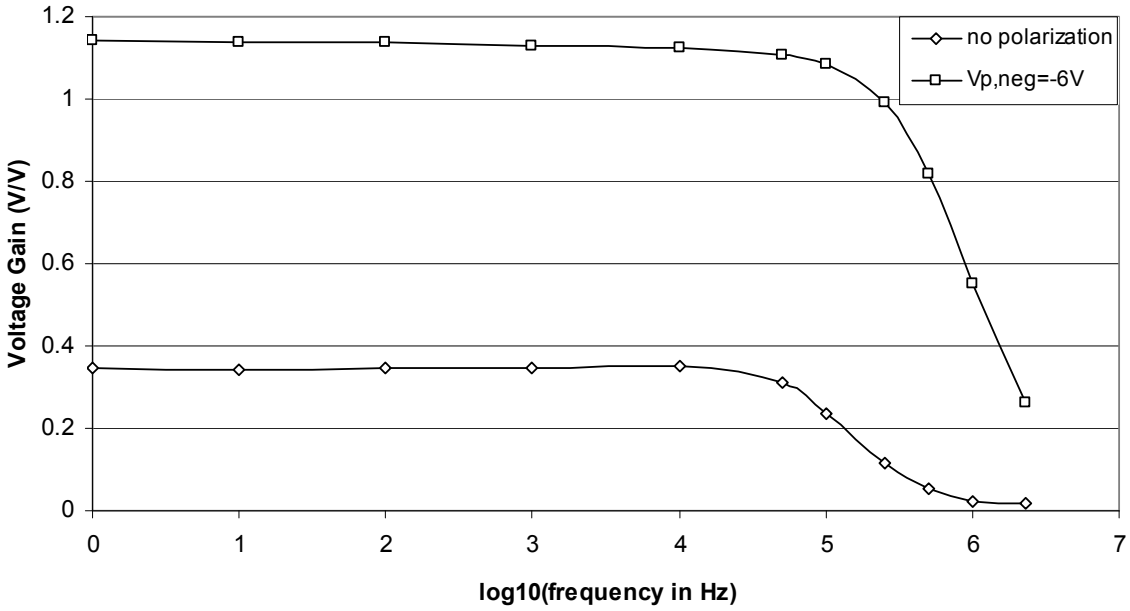

Figure 4.11 Plot of voltage gain vs. logarithm of frequency for no polarization and negative polarization with V_{bias} of 0V

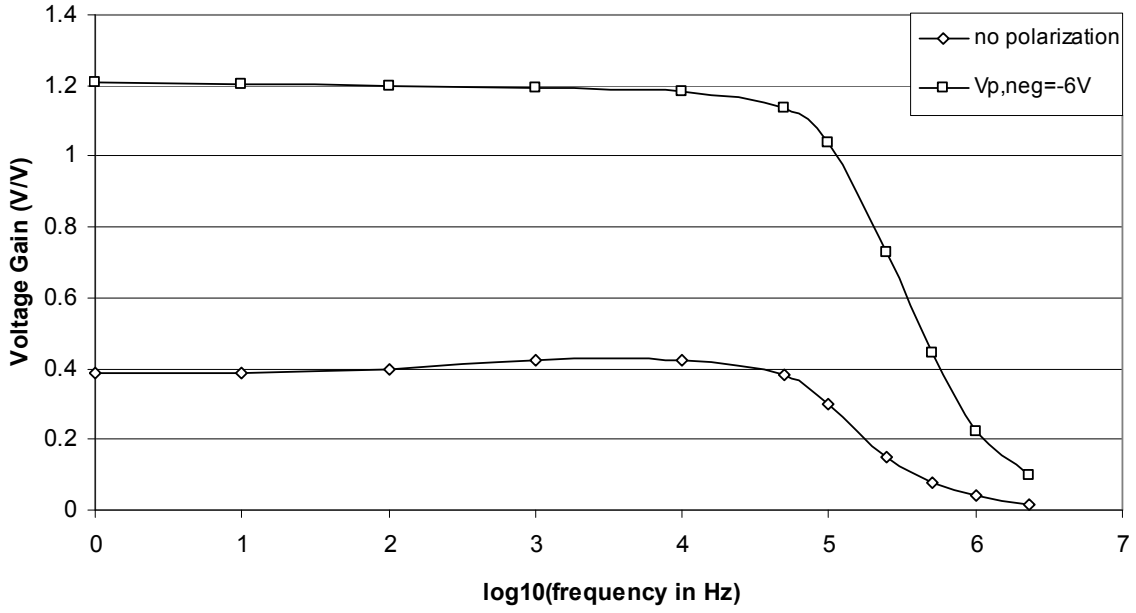

Figure 4.12 Plot of voltage gain vs. logarithm of frequency for no polarization and negative polarization with V_{bias} of -2V

The plots clearly show that applying a negative polarization voltage at the gate greatly enhances the voltage gain of the amplifier. This behavior was noted throughout much of the data collected. The effect of a positive polarization voltage was next examined with V_{DD} of 4V, V_{in} of 1V, a load resistance of 10kΩ, and a positive polarization voltage, $V_{p,pos}$, of 7.5V. In Figure 4.13, V_{bias} was set to 5V, while V_{bias} was set to 7.5V in Figure 4.14.

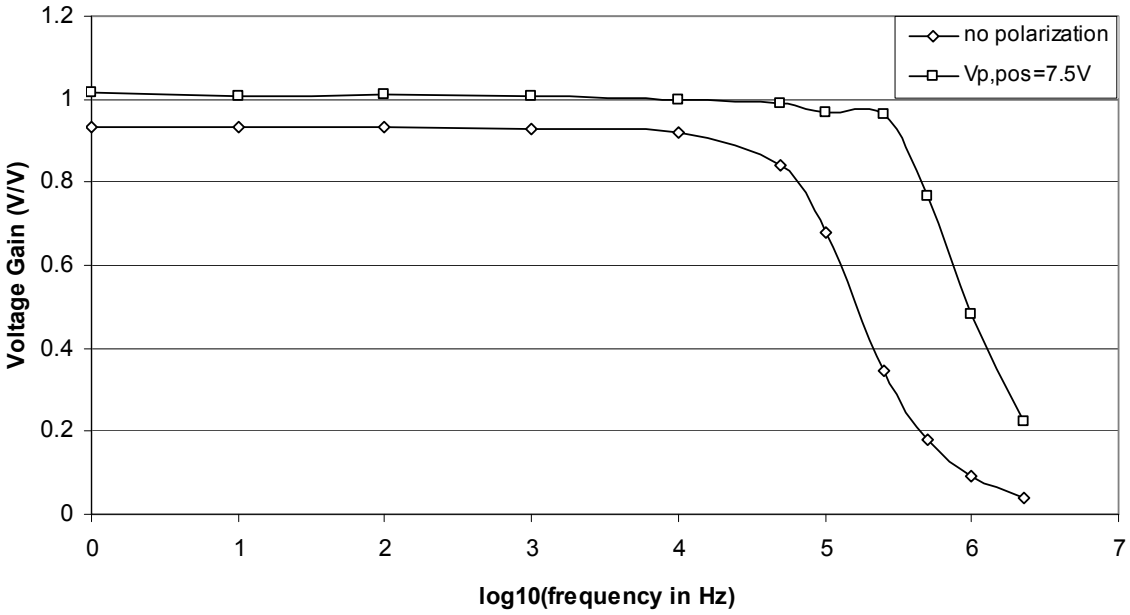

Figure 4.13 Plot of voltage gain vs. logarithm of frequency for no polarization and positive polarization with V_{bias} of 5V

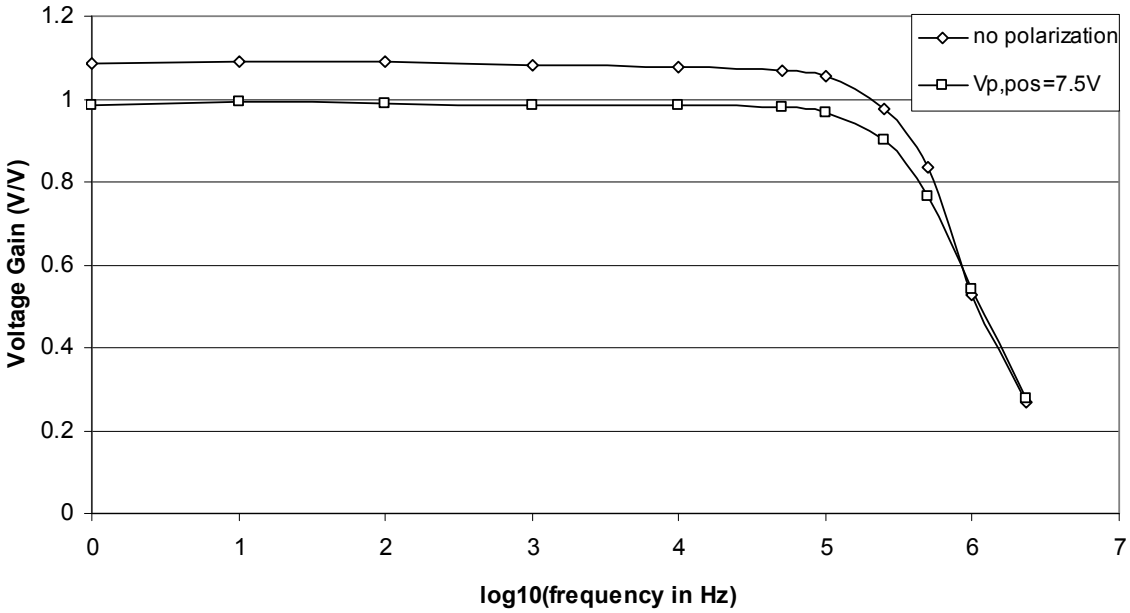

Figure 4.14 Plot of voltage gain vs. logarithm of frequency for no polarization and positive polarization with V_{bias} of 7.5V

As shown in these plots, applying a positive polarization voltage either decreases the voltage gain or slightly increases it, but the large increase in gain resulting from applying a negative polarization voltage was not seen here. It was noted that for most of the data, negatively polarizing the gate of the FeFET resulted in higher voltage gain. This phenomenon can be attributed to the fact that negatively polarizing the gate of the FeFET results in the accumulation of minority carriers at the ferroelectric-substrate interface, which means the transistor is operating in depletion mode [18]. Conversely, when the gate of the FeFET is positively polarized, majority carriers accumulate at the ferroelectric-substrate interface, and the transistor is then in accumulation [18].

C. Comparison of the Voltage Gain and Phase Shift of the FeFET and MOSFET CG Amplifiers

The MOSFET CG amplifier is not characterized by its voltage gain; however, its gain is slightly smaller than that of the CS amplifier due to the CG amplifier's low input resistance [1]. The FeFET CG amplifier's gain was also slightly lower than that of the FeFET CS amplifier, as was shown in Table 3.1. Since the MOSFET CG amplifier is usually used in the cascade circuit configuration, future work on the FeFET CG amplifier can examine the FeFET cascade circuit.

The phase shift of the MOSFET CG amplifier has a magnitude of about 0° at low frequencies and 90° at high frequencies. This was also noted in the FeFET CG amplifier's phase shift vs. logarithm of frequency plots.

D. The Frequency Response

The frequency response of the FeFET CG amplifier is similar to that of the FeFET CS amplifier and is therefore different from that of the FeFET CD amplifier and from any

MOSFET amplifier's frequency response. Figure 4.15 plots the voltage gain in decibels vs. the input frequency in Hz for several input signals. The frequency response of Figure 4.15 shows the frequency range of 1Hz to 2.3MHz, which covers the low- to high-frequency ranges. Like the FeFET CS amplifier's frequency response plot, this plot looks like a reflection along the x-axis of the low- and mid-frequency response of the MOSFET CG amplifier. Again, a nearly linear decrease in voltage gain is seen in the low-frequency portion of the plot. The mid-frequency response is also almost linearly decreasing rather than remaining at a constant value, as would be seen in the MOSFET CG amplifier. The gain in this plot does not begin to level off as quickly as was seen in the FeFET CS amplifier plot. Further work on the FeFET CG amplifier frequency response should examine the very high-frequency response and determine the frequency at which the voltage gain levels off.

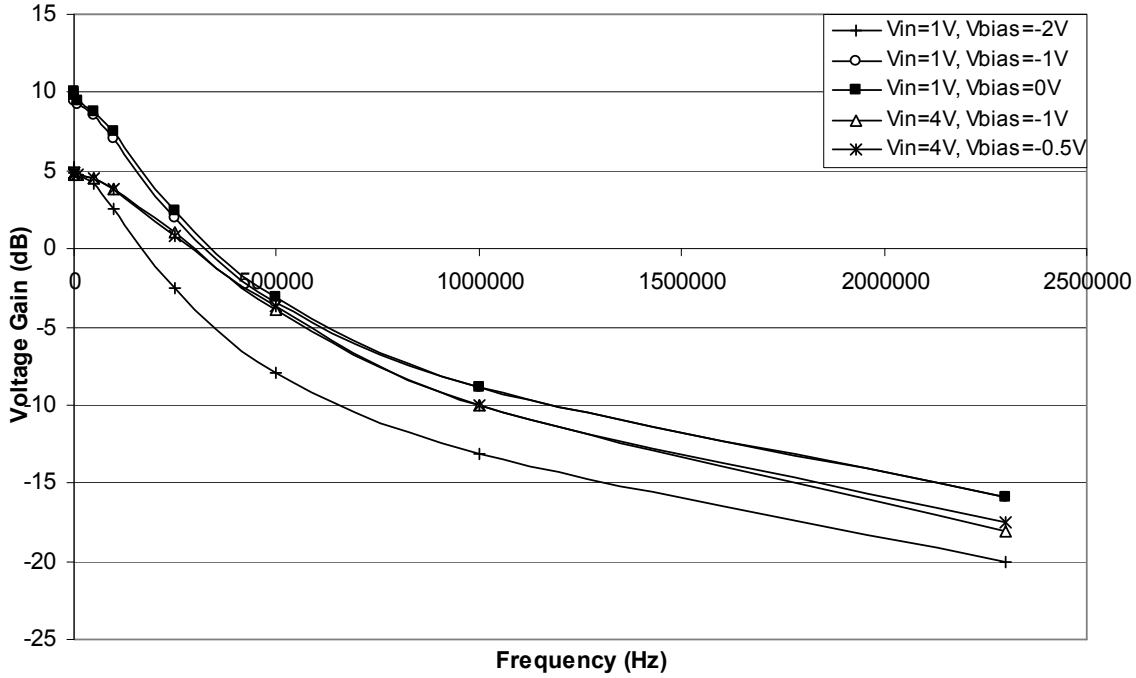

Figure 4.15 FeFET CG amplifier frequency response

E. Conclusion of Experimental Results

The FeFET CG amplifier displays unique characteristics not seen in its MOSFET counterpart. The logarithmic relationship between the phase shift and each of the low and high input frequency ranges and the voltage gain and these frequency ranges may prove very useful in numerous electronics applications. Moreover, the distinctive shape of the plots of phase shift vs. logarithm of resistance and voltage gain vs. logarithm of resistance can be studied further to realize its full effect. Another interesting factor of the FeFET CG amplifier is the effect of positive and negative gate polarization on the voltage gain and the increase in voltage gain that was observed when negative polarization was applied. The full potential of the FeFET CG amplifier is yet to be realized.

F. Nonquasi-Static FeFET CG Amplifier Model

The NQS model created to describe the behavior of the FeFET CG amplifier is based on the physically-derived equations given by Equations (2.1) through (2.29). The drain current is derived using the same method as was done for the CD and CS amplifiers. However, as was the case with the CS amplifier, the output voltage equation was altered according to the CG amplifier circuit configuration. Thus, the output voltage is given by

$$V_{out} = V_{DD} - I_d * R. \tag{4.1}$$

a. Simulation Steps

As with the previous two amplifiers, the FeFET CG amplifier was also simulated in MATLAB®, and the simulation steps are listed below. A flowchart of the detailed simulation steps is shown in Figure 4.16.

1. Enter fabrication parameters (L, W, N_A, t_f, μ, etc.), simulation time interval, amplifier parameters (V_{DD}, input frequency, amplitude of input signal, load resistance, etc.), dc terminal voltages (V_D, V_G, V_S, and V_B), and number of channel partitions (N).
2. Define the sinusoidal input signals v_{gs} and v_{gb} using the amplifier parameters entered and the current time step.
3. Rewrite the input signals using their phasor representations.
4. Calculate the surface potential at the source ($\psi_{s0}(t)$) and the surface potential at the drain ($\psi_{sL}(t)$) using Newton's method.
5. For each channel partition, calculate the surface potential at both edges of the partition using Newton's method. Then, determine the surface potential across the partition by averaging the potentials at the edges and plugging this value into Equation (2.13) to obtain the most accurate surface potential value.
6. Propagate through a function for polarization and electric field calculations for each partition based on Equations (2.14)-(2.21).
7. Calculate the total ferroelectric charge per unit area, q'_F, by summing each partition's polarization and dividing by the number of partitions.
8. Determine the threshold voltage using Equation (2.22).
9. Use the y-parameter model to calculate the drain current as described in Equations (2.23)-(2.29).
10. Multiply the drain current by a scaling factor.
11. Determine an initial value for V_{out} using Equation (4.1).
12. Multiply V_{out} by a scaling factor.

13. Update the value of the drain current using Equation (2.23) with V_{ds} being replaced with the difference of the value for V_{out} just calculated and the source voltage, V_s.
14. Multiply the drain current by the same scaling factor used earlier for the initial value of the current.
15. Recalculate V_{out} using the last value obtained for the drain current.
16. Multiply V_{out} by the same scaling factor used earlier for the initial value of V_{out}.
17. Increment the simulation time by one time step.
18. If the incremented time is less than or equal to the final time step, go to Step 4. Otherwise, plot the output voltage with respect to ωt.

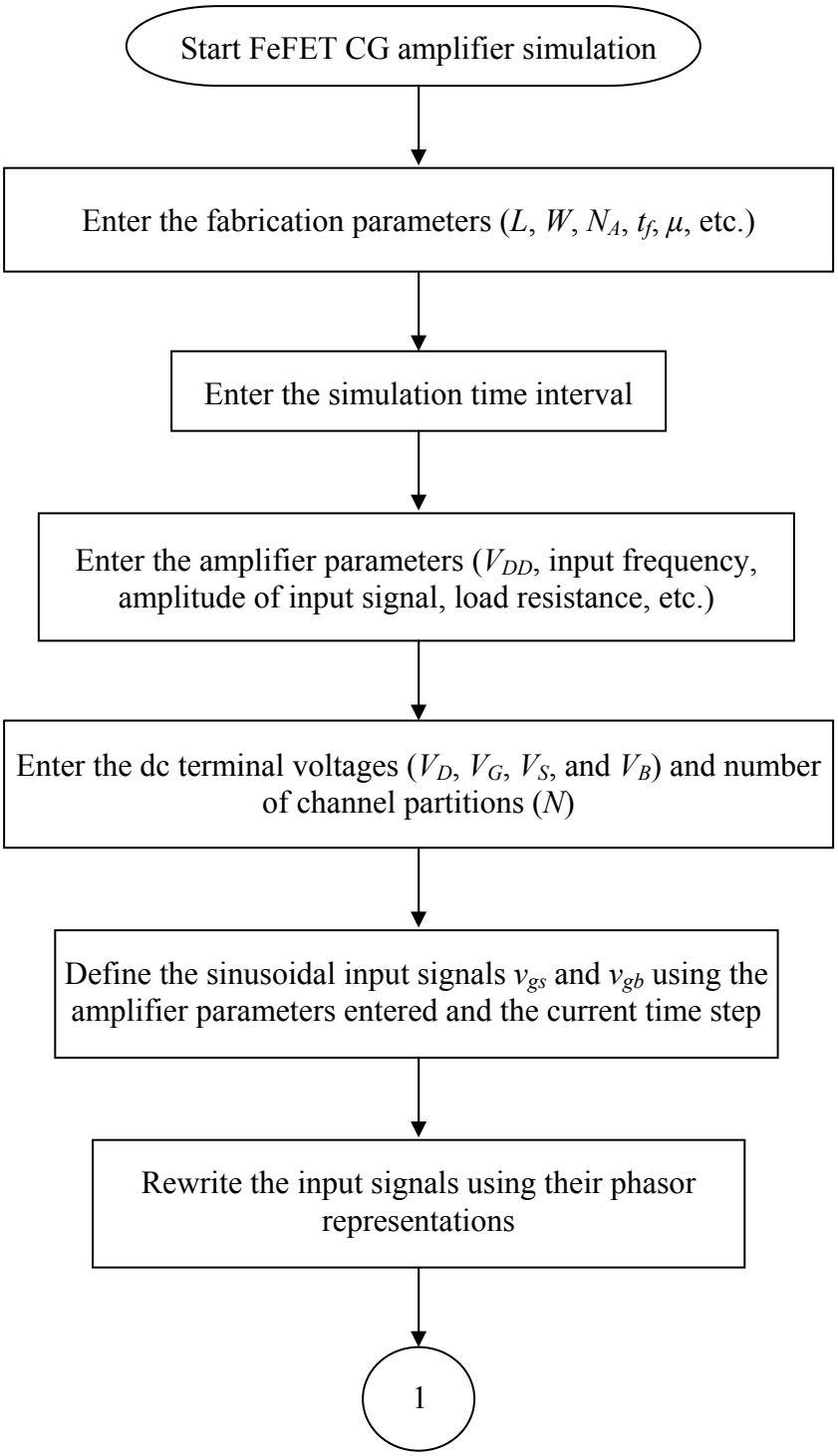

Figure 4.16 FeFET CG amplifier simulation steps

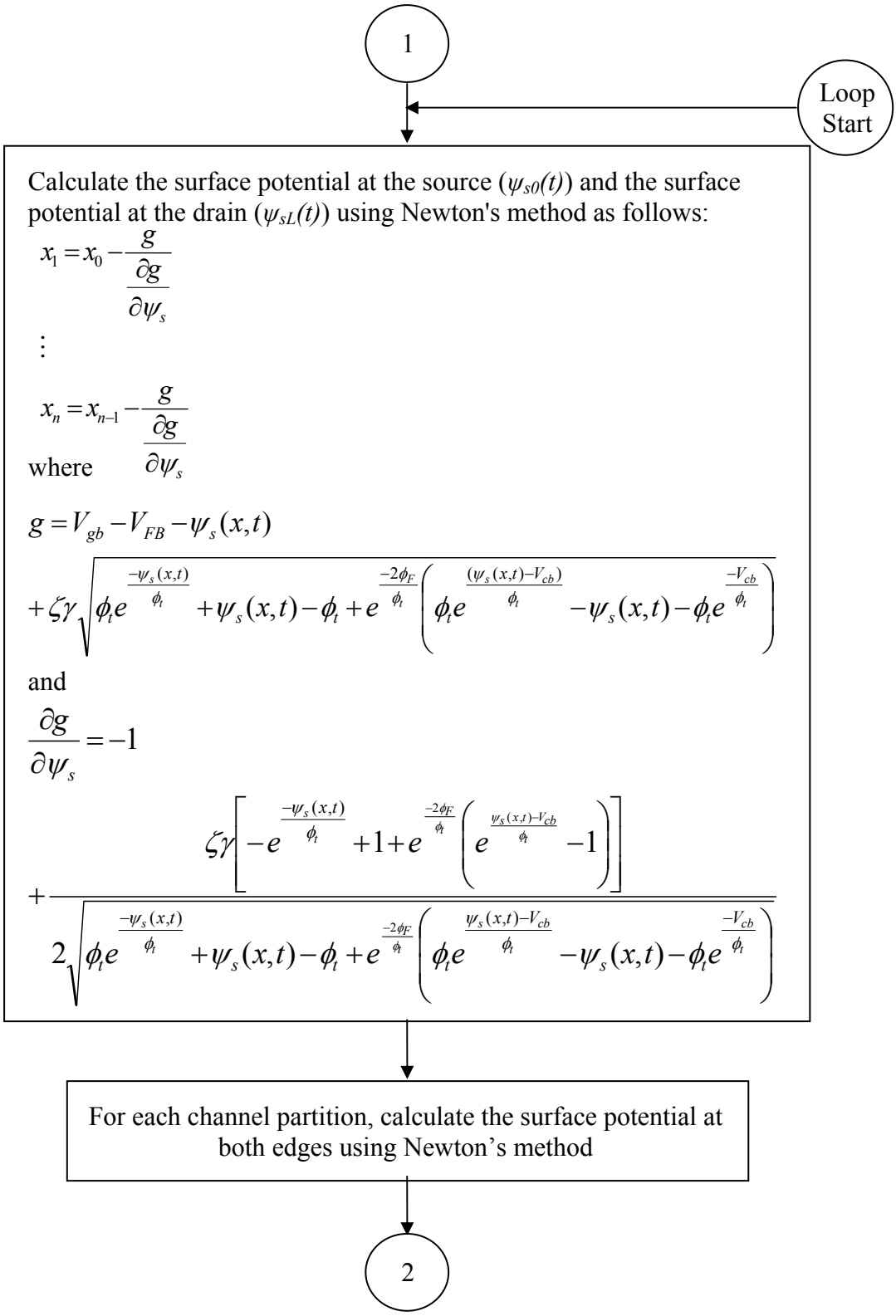

Figure 4.16 FeFET CG amplifier simulation steps (continued)

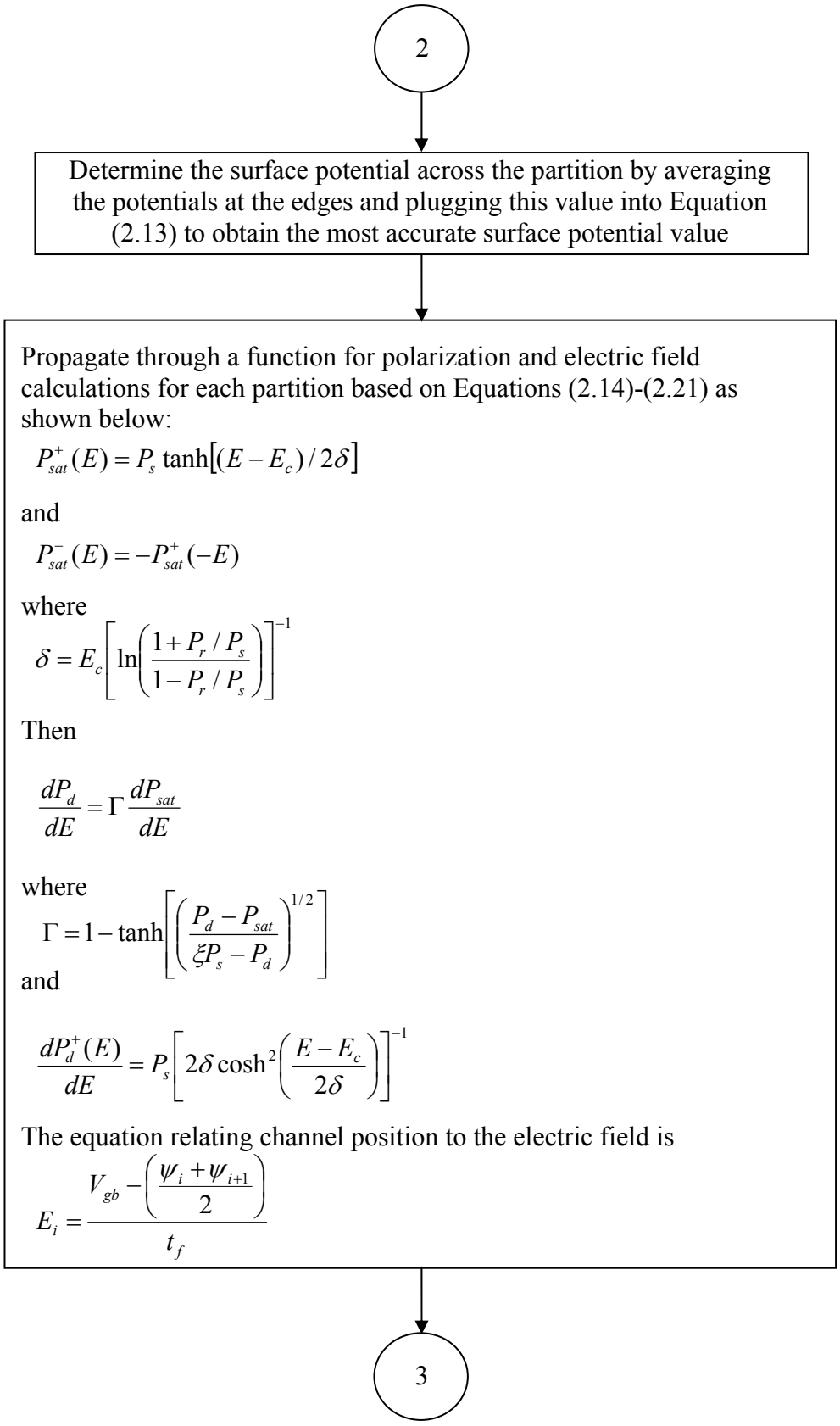

Figure 4.16 FeFET CG amplifier simulation steps (continued)

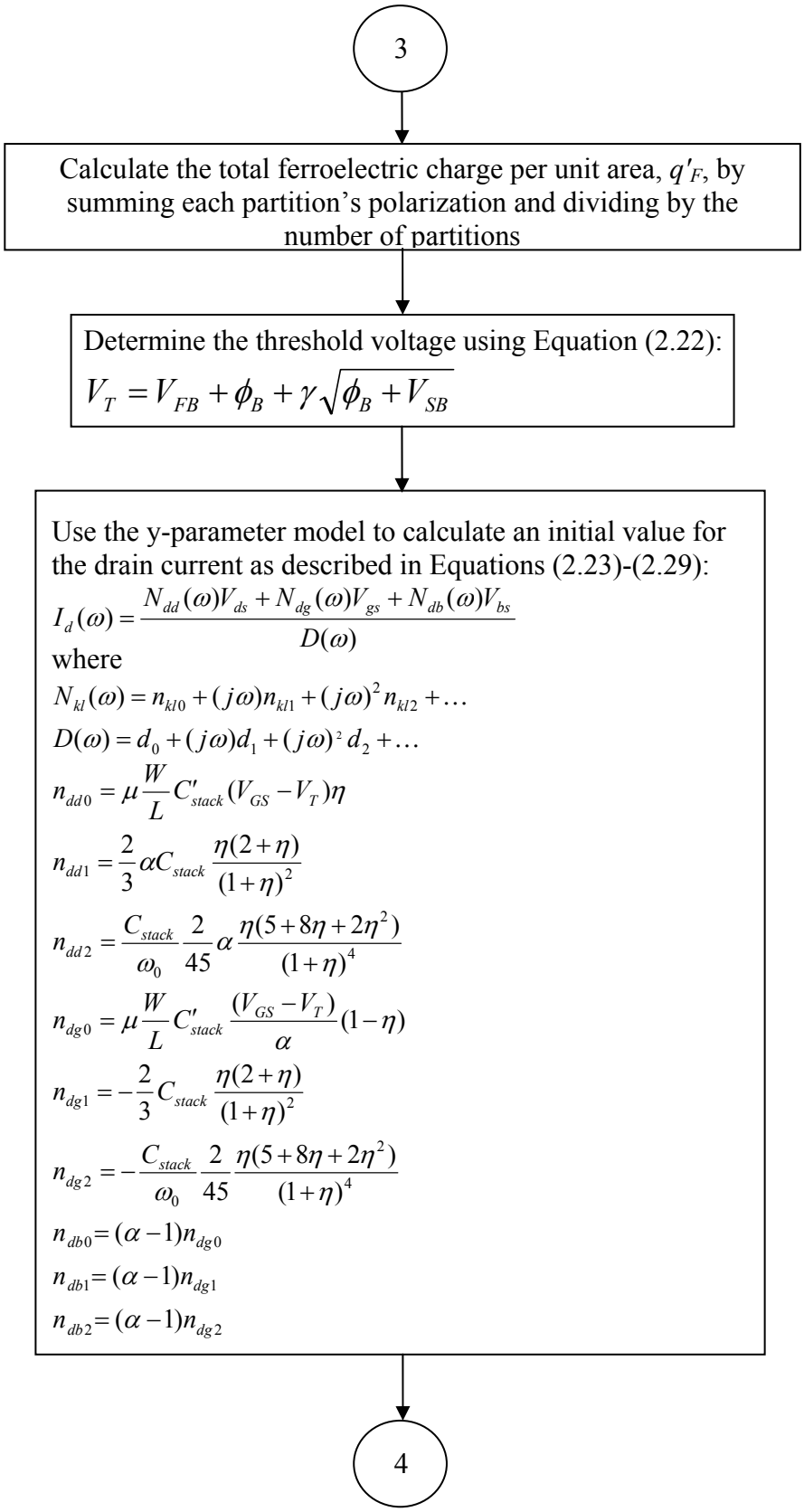

Figure 4.16 FeFET CG amplifier simulation steps (continued)

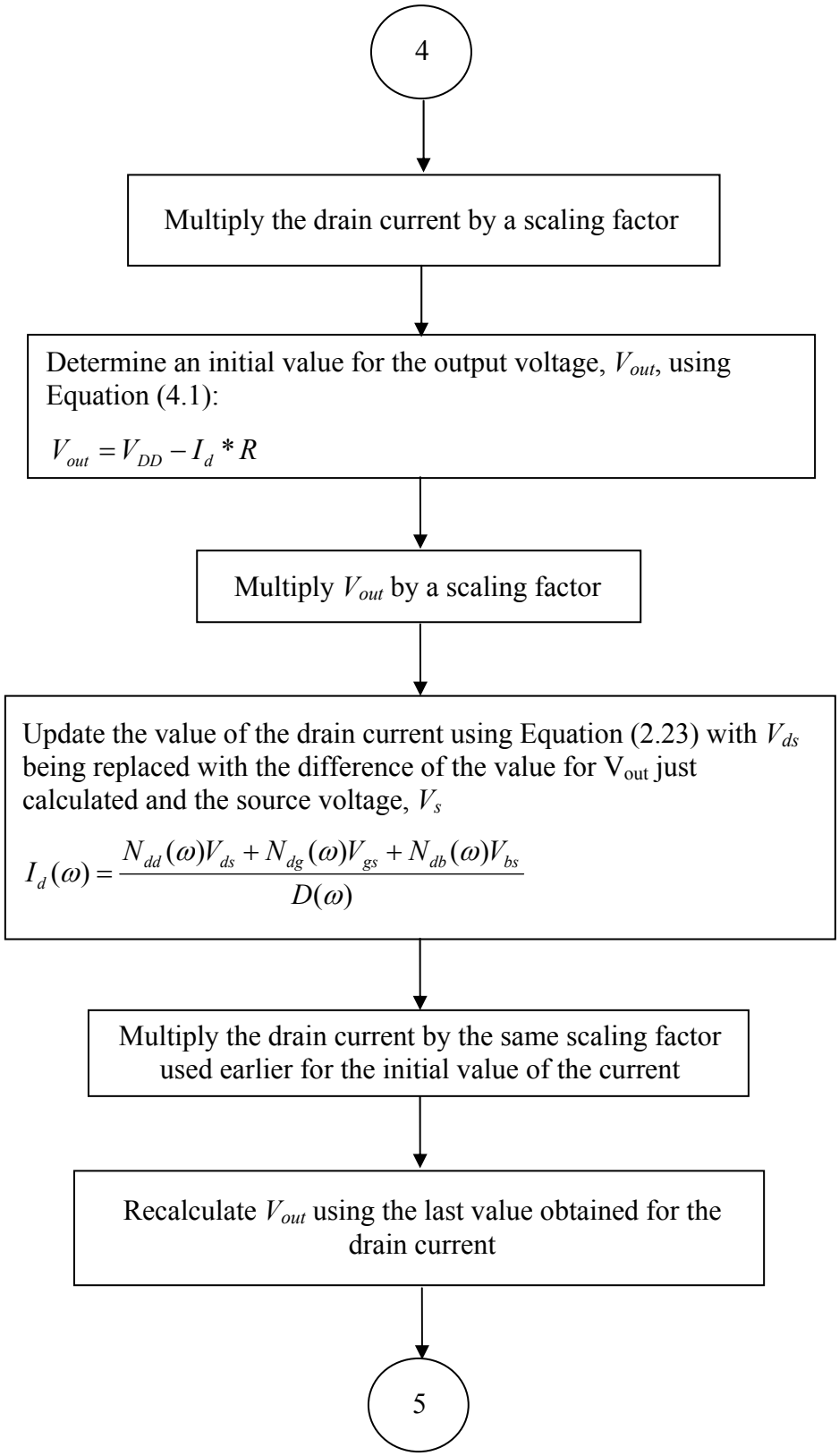

Figure 4.16 FeFET CG amplifier simulation steps (continued)

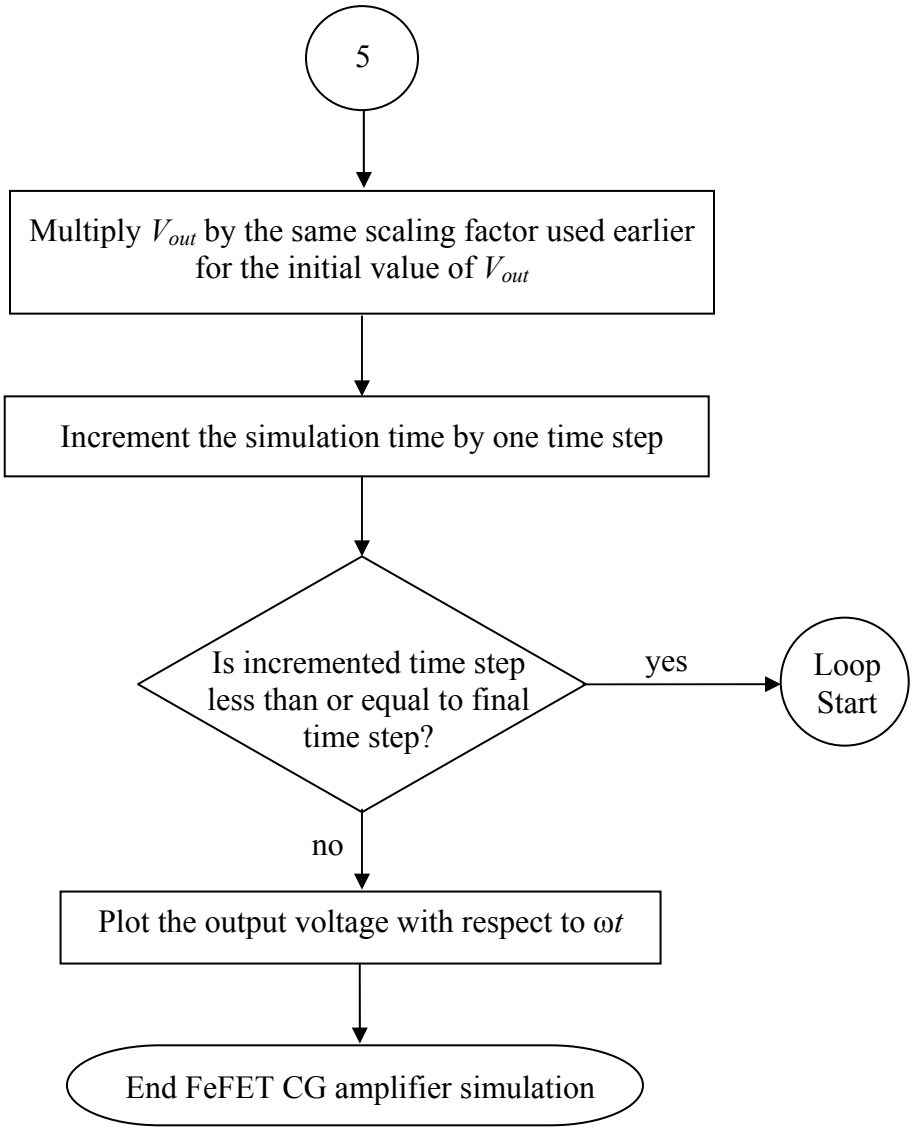

Figure 4.16 FeFET CG amplifier simulation steps (continued)

b. Model Results

Two test cases were conducted to verify the model's results. For the first test case, V_{DD} was set to 4V, the amplitude of the input signal was 0.5V, an offset voltage of 6.5V was included, the input frequency was selected to be 1MHz, the load resistor was 10kΩ, the drain current's scaling factor was chosen to be 1.445×10^{-4}, and the output

voltage's scaling factor was 0.2835. Figures 4.17 and 4.18 depict the oscilloscope and modeled plots, respectively.

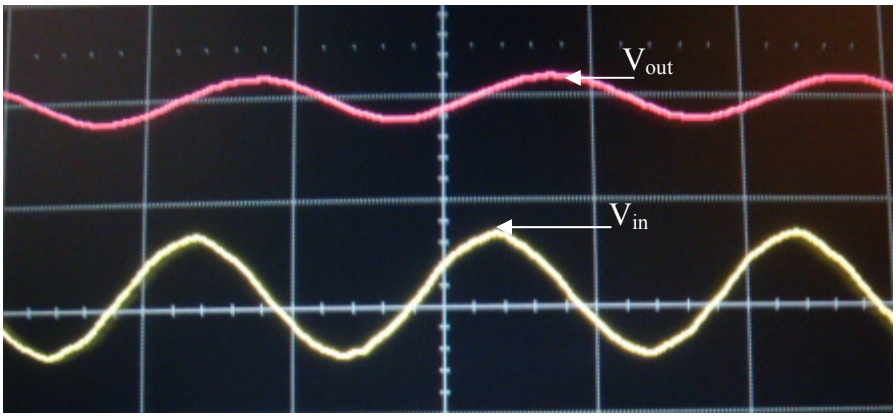

Figure 4.17 Oscilloscope output for the first test case with a scale of 1V per division for V_{in} and V_{out}

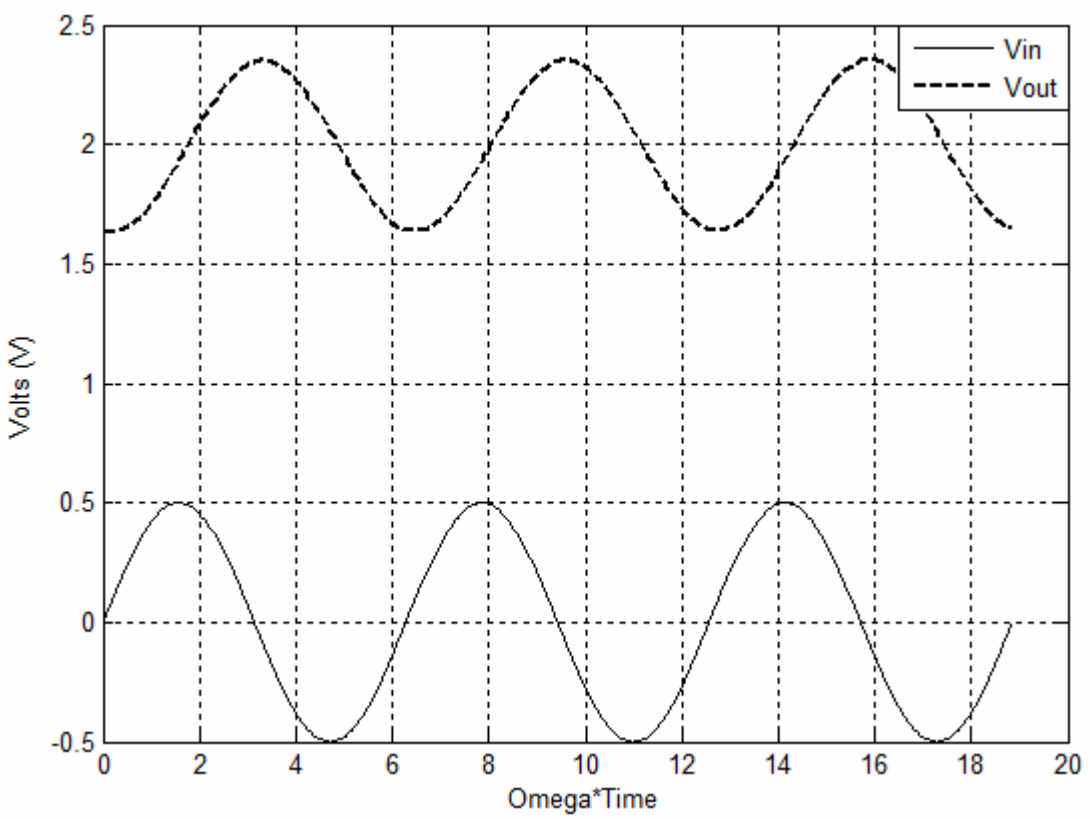

Figure 4.18 Modeled output for the first test case

Comparing the modeled plot with the oscilloscope plot illustrates the model's efficiency in reproducing the output voltage signal's shape and values. As with the two previous amplifiers, the modeled output plot always displayed an inbuilt phase shift. For this test case, 70° of inherent phase shift were noted in the modeled plot, so the modeled input signal was adjusted accordingly to produce the correct phase shift. Table 4.1 shows the maximum and minimum values of the simulated and measured output signals. It can be seen from the table that the modeled values are very close to the empirical values.

For the second test case, V_{DD} was 8V, the input amplitude was 1V, an offset voltage of -1V was added, the frequency was 2.3MHz, the load resistance was 10kΩ, the drain current's scaling factor was -1.198×10^{-3}, and the output voltage's scaling factor was 0.22. Since the input signal was very small, a negative polarization voltage, $V_{p,neg}$, of -6V was added to the gate to ensure that the FeFET operates in saturation. Figures 4.19 and 4.20 are the oscilloscope and modeled plots, respectively.

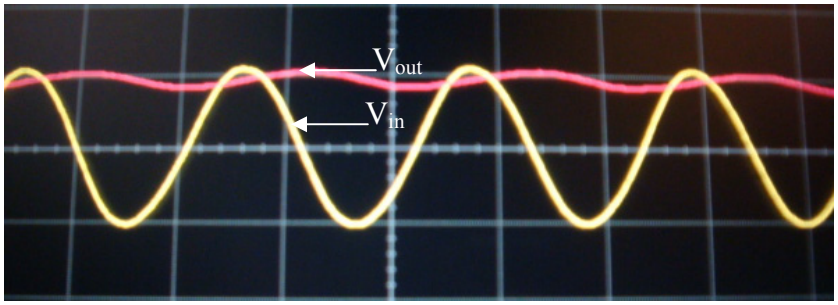

Figure 4.19 Oscilloscope output for the second test case with a scale of 1V per division for V_{in} and 2V per division for V_{out}

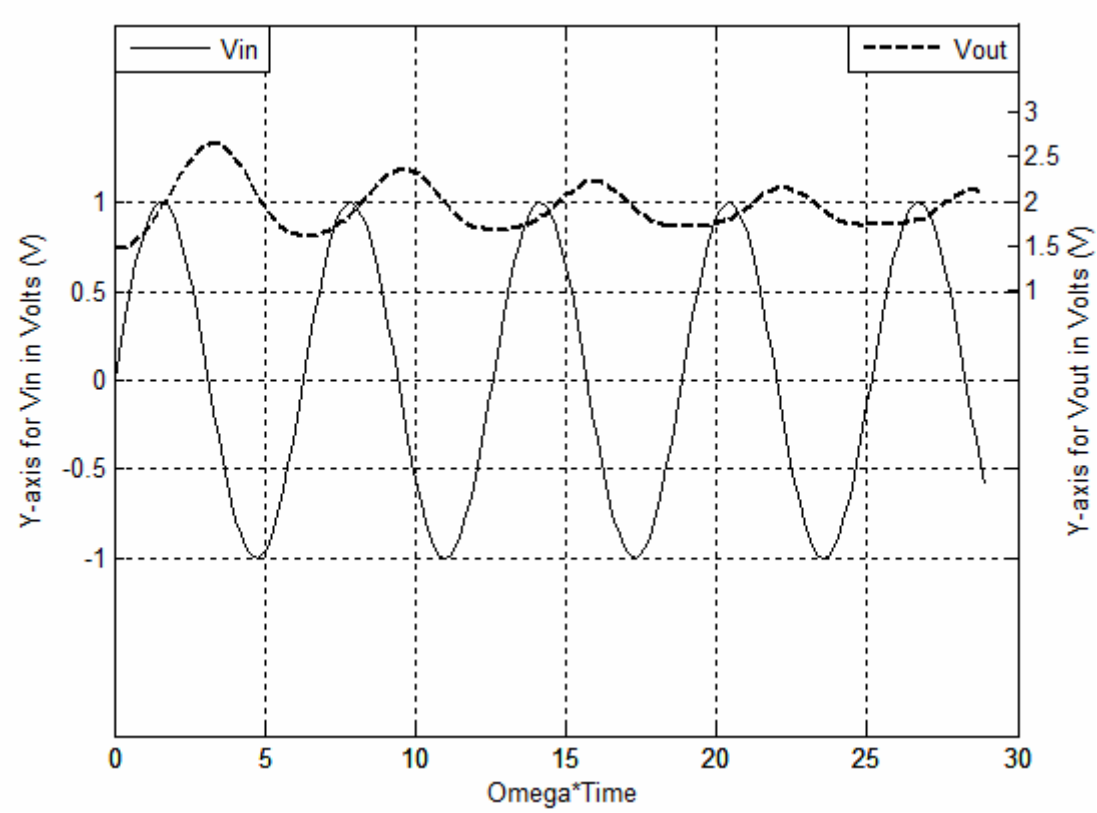

Figure 4.20 Modeled output for the second test case

As was seen with one of the CD amplifier test cases and one of the CS amplifier test cases, polarization fluctuations caused the output voltage to fluctuate for a few seconds, which were then smoothed out as the polarization stabilized. Despite these fluctuations, the oscilloscope and modeled plots are clearly similar in both shape and values. Table 4.1 further proves the accuracy of the simulated plots. Again, there was an inherent phase shift in the modeled signal, which was 110° for this test case, so the input signal's phase shift parameter was adjusted to compensate for it.

Table 4.1 Oscilloscope and simulation results for FeFET CG amplifier

	Test Case I		Test Case II	
	Max. value	Min. value	Max. value	Min. value
Oscilloscope Results	2.20	1.774	2.11	1.68
Simulation Results	2.355	1.639	2.122	1.730

G. Conclusion of Modeled Data Analysis

A physically-derived NQS model was created to accurately model the empirical behavior of the FeFET CG amplifier. As has been shown with the two previous amplifier types, the voltage plots generated by the model have the same shape and exhibit the same trends as the oscilloscope plots. It can be seen that this model is effective and accurate.

CHAPTER V

CHARACTERIZATION AND MODELING OF THE FeFET DIFFERENTIAL AMPLIFIER

The differential amplifier "is the most widely used building block in analog integrated-circuit design" [1]. As such, the study of FeFET analog circuitry would not be complete without an examination of the characteristics of the FeFET differential amplifier. As with the previous three amplifiers, a model was created to simulate the behavior of this FeFET-based amplifier in order to facilitate further study in the field.

A. Basic Structure

The FeFET differential amplifier examined in this work is built using two FeFETs and three resistors as shown in the circuit configuration of Figure 5.1. The simplest differential amplifier configuration was researched since FeFET differential amplifier behavior has not been extensively studied, and this work presents the first physics-based model of this circuit. A sinusoidal input signal v_{in1} was applied to the gate of the left FeFET along with a dc offset voltage V_{offset} if it exists. At the gate of the other FeFET, a dc input voltage V_{IN2} was applied. However, as will be seen in later measurements, data was collected for the case where the input signal applied to the right FeFET was also sinusoidal. The first output signal v_{out1} was taken at the drain of the left FeFET, whereas the second output signal v_{out2} was measured at the drain of the right FeFET. The load

resistors R_1 and R_2 were placed between V_{DD} and the drains of the left and right FeFETs, respectively. The source terminals of both transistors were connected, and a source resistor R_3 was placed at that node.

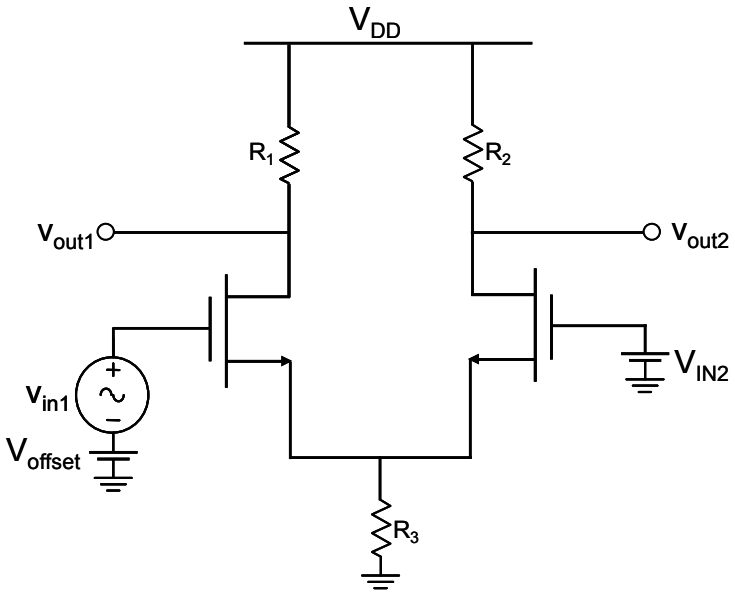

Figure 5.1 FeFET differential amplifier circuit configuration

B. Empirical Measurements of the FeFET Differential Amplifier

Due to this circuit's complexity, as compared to the previous circuits examined in this work, many more measurements were carried out for this amplifier. As with the other amplifiers, the effect of frequency on the phase shift and voltage gain was examined; however, each output signal, namely v_{out1}, v_{out2}, and the differential output, was studied independently. Moreover, the presence of two input signals led to the examination of the effect of varying the load resistors and source resistor on the phase shift and voltage gain of the three output signals for two input cases: when the first input signal was sinusoidal and the other was dc and when both input signals were sinusoidal.

a. Effect of Frequency on Individual and Differential Phase Shifts and Voltage Gains

The first relationship studied in the FeFET differential amplifier circuit was the effect of the input frequency on the phase shift of each of the individual output signals and the differential output signal. For this analysis, V_{DD} was set to 8V, R_1 and R_2 were set to 10kΩ, R_3 was 5kΩ, and the frequency ranged from 1Hz to 2.3MHz. Both FeFETs were positively polarized with a polarization voltage $V_{p,pos}$ of 6V. Three input signals were tested. In the first case, v_{in1} was set to 1.5*sin(ωt)+4.24 and V_{IN2} was 3.7V. For the second data set, the sinusoidal input was 2.5*sin(ωt)+3 and the dc input was 3V. For the final test case, v_{in1} was 3.5*sin(ωt)+4.16 and V_{IN2} was 2.9V. Figures 5.2, 5.3, and 5.4 are plots of the phase shift vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output, respectively. As with the previous amplifier measurements, all logarithms are of base 10.

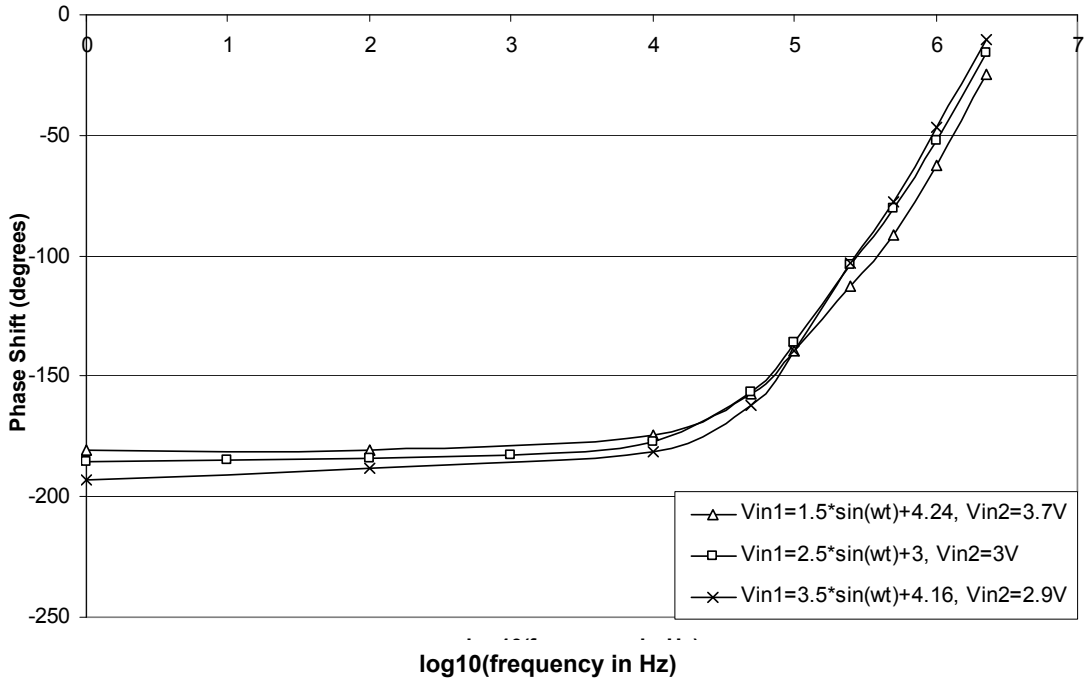

Figure 5.2 Plot of phase shift of v_{out1} vs. logarithm of frequency for three input signals

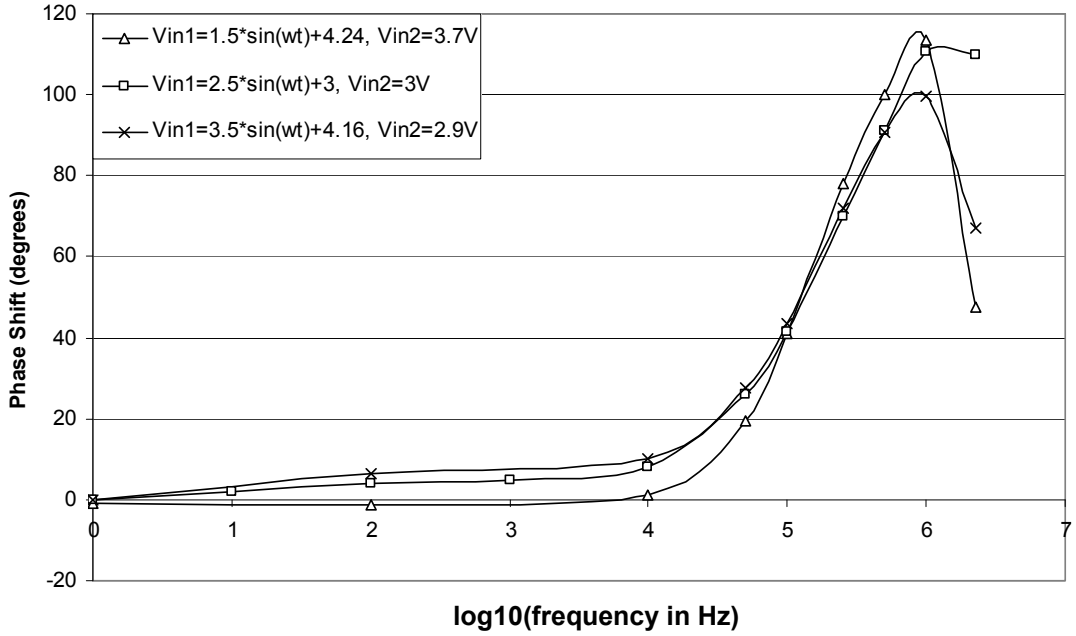

Figure 5.3 Plot of phase shift of v_{out2} vs. logarithm of frequency for three input signals

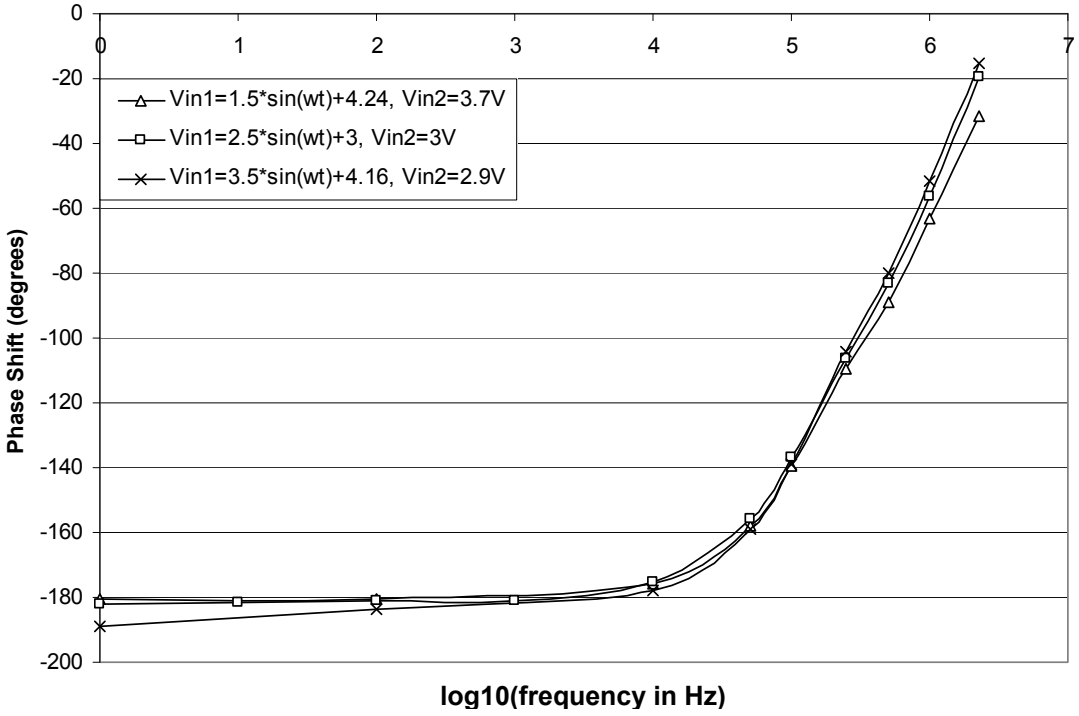

Figure 5.4 Plot of phase shift of differential output vs. logarithm of frequency for three input signals

Examining the phase shift plots shows that the phase shift vs. frequency relationship of the differential amplifier displays several characteristics. The magnitude of the phase shift of the output signal v_{out1} increases with the increasing amplitude of the input signal v_{in1} for frequencies up to 50kHz. At higher frequencies, the larger the amplitude of the input signal, the less negative the phase shift of v_{out1} becomes. The increasing amplitude of v_{in1} also increases the magnitude of the phase shift for frequencies up to 50kHz for v_{out2}. At higher frequencies, the phase shift tends to decrease with increasing input amplitude. Similarly, for the differential output signal, the magnitude of the phase shift increases with increasing input amplitude for frequencies at or below 50kHz. For higher frequencies, the phase shift's magnitude decreases with increasing v_{in1}. These characteristics are further illustrated in the plots of Figures 5.5 through 5.7, which show the phase shift vs. logarithm of frequency for v_{out1}, v_{out2}, and the differential output, respectively, with trend lines.

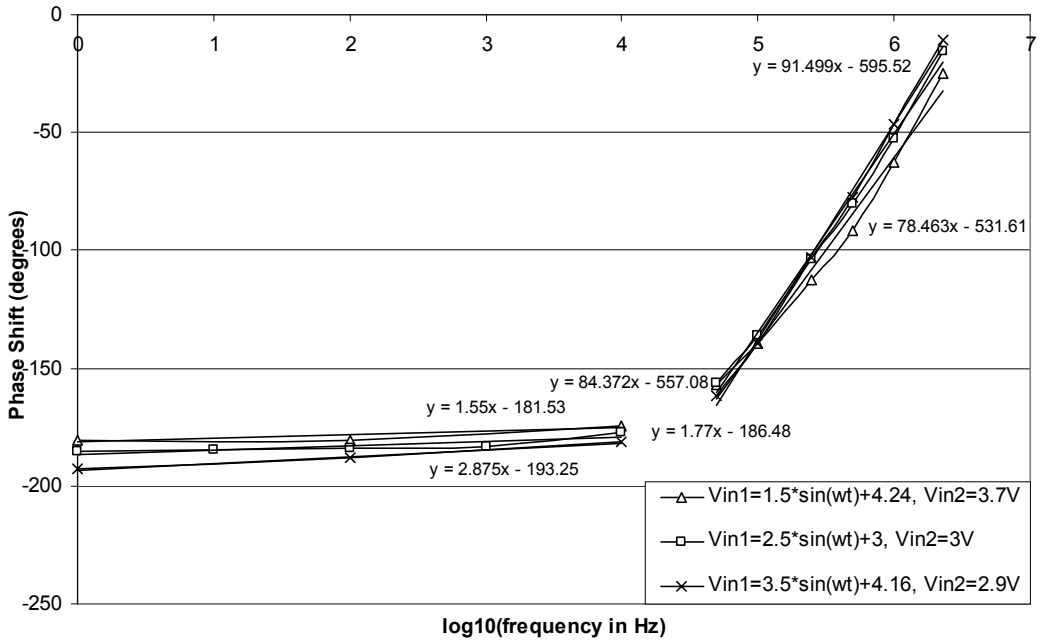

Figure 5.5 Plot of phase shift of v_{out1} vs. logarithm of frequency for three input signals with trend lines

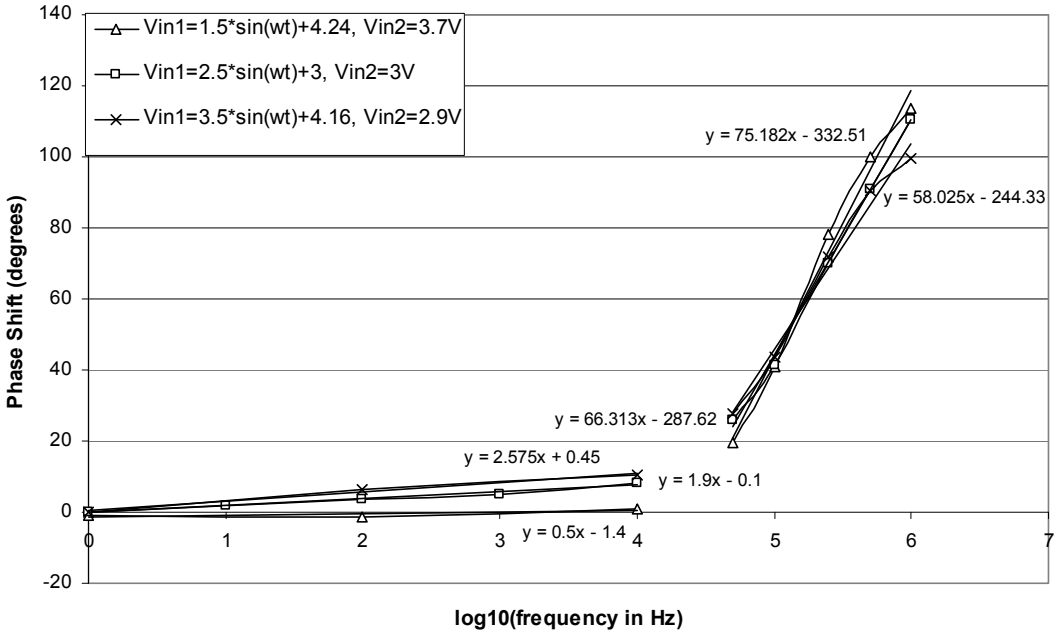

Figure 5.6 Plot of phase shift of v_{out2} vs. logarithm of frequency for three input signals with trend lines

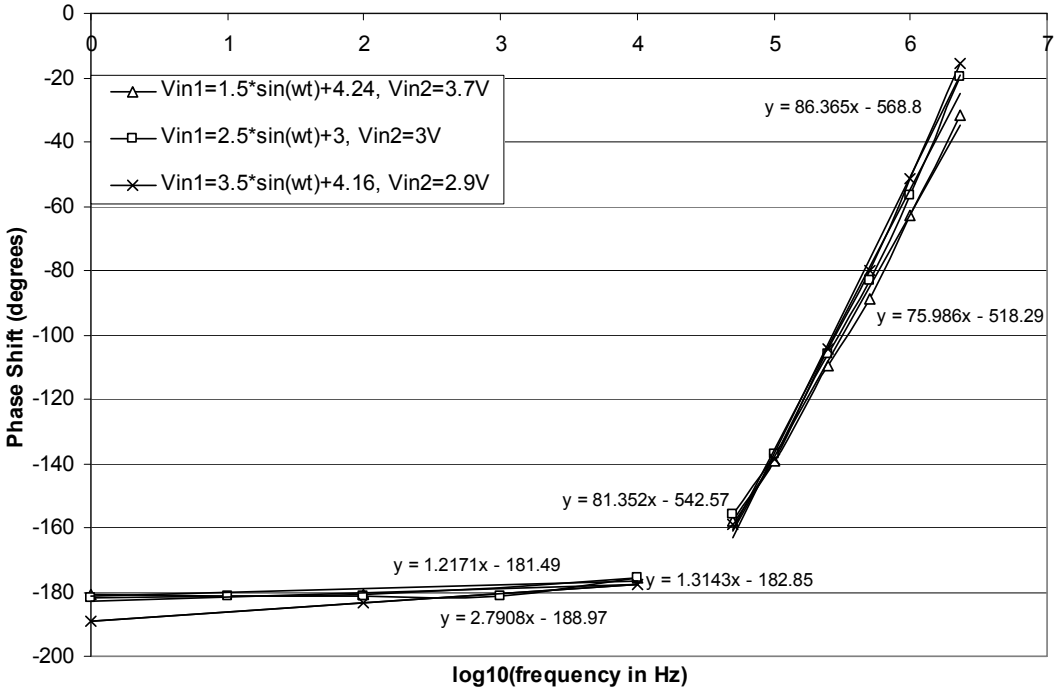

Figure 5.7 Plot of phase shift of differential output vs. logarithm of frequency for three input signals with trend lines

All the trend lines on the three plots indicate that the phase shift of each of the output signals is linearly related to the logarithm of the input frequency. For the phase shift plot of v_{out1}, the trend lines for data points at or below 10kHz are nearly parallel. The same is true for the trend lines describing the data points at higher frequencies. For the plot of the phase shift of v_{out2}, the linear trend lines almost exactly describe the data lines for frequencies at or below 10kHz. The data lines for the higher frequencies are very close together and have similar slopes. Finally, for the differential output phase shift, the data lines and their respective trend lines are very close for frequencies at or below 10kHz and for frequencies higher than 10kHz.

The next relationship studied in the differential amplifier was the effect of the input frequency on the voltage gain. Again, V_{DD} was set to 8V, R_1 and R_2 were set to 10kΩ, R_3 was 5kΩ, $V_{p,pos}$ was 6V, and the frequency ranged from 1Hz to 2.3MHz. The same three input signals were applied. Figures 5.8, 5.9, and 5.10 show the plots of the voltage gain vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output signal, respectively.

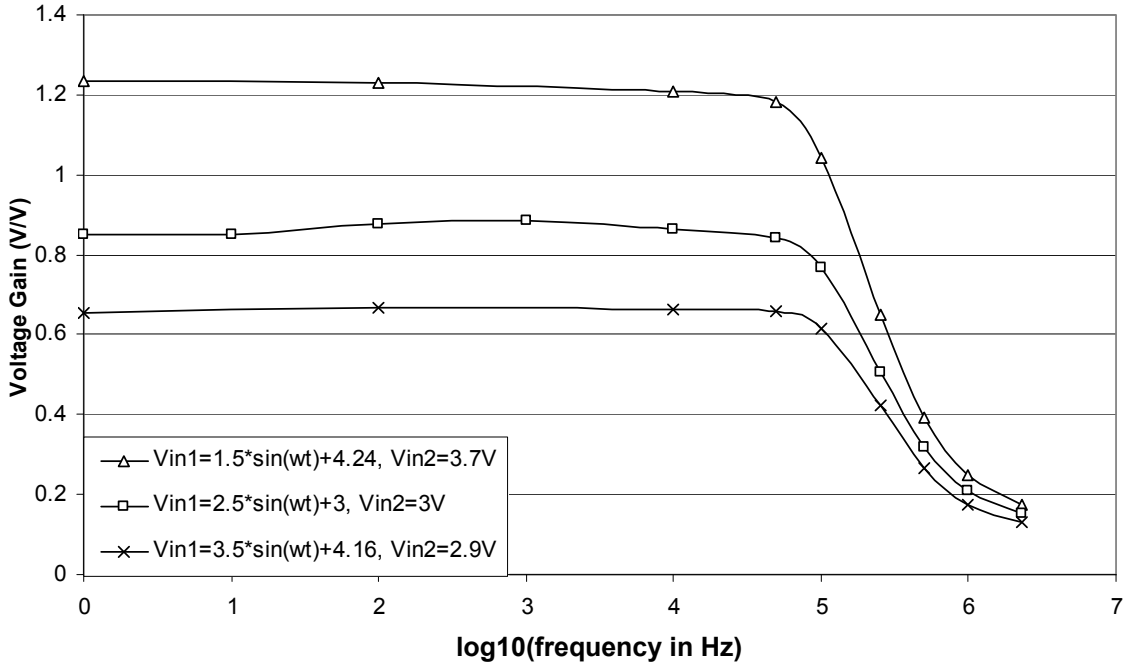

Figure 5.8 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three input signals

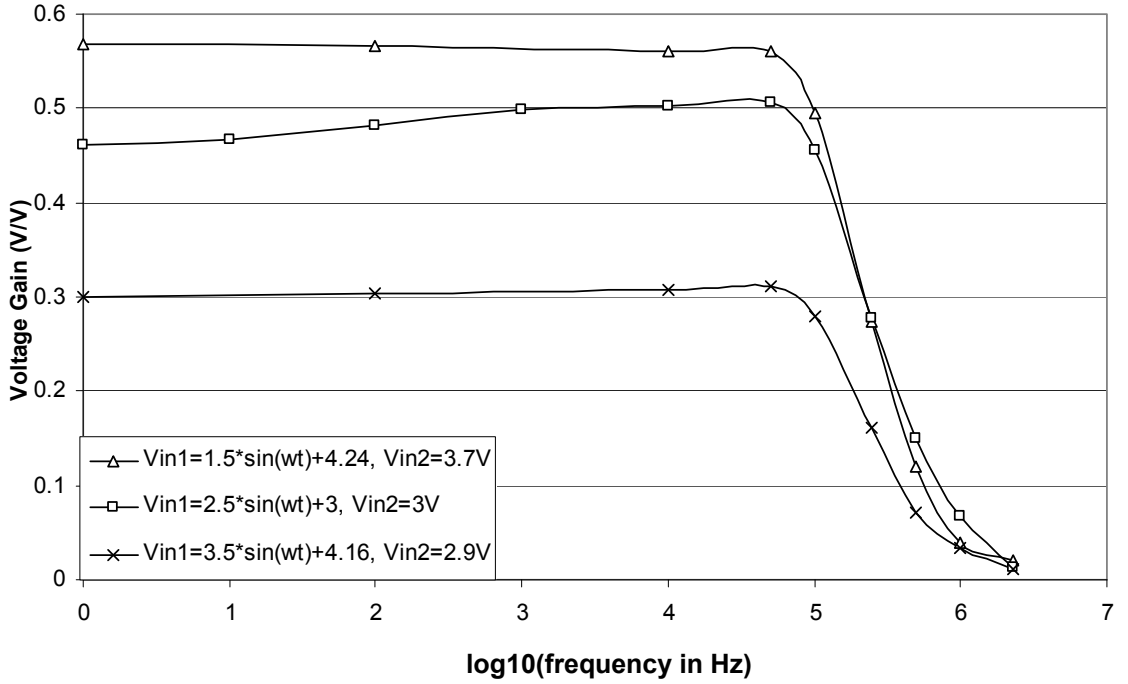

Figure 5.9 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three input signals

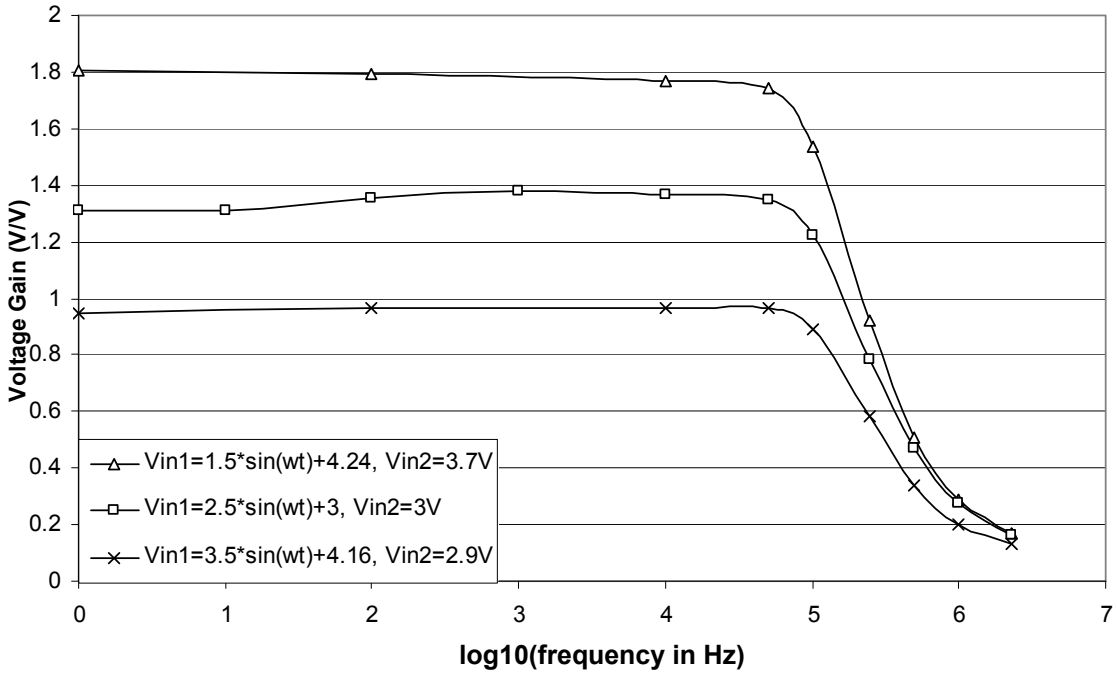

Figure 5.10 Plot of voltage gain of differential output vs. logarithm of frequency for three input signals

The previous three figures share several characteristics. First, it is noted that the voltage gain decreases with increasing v_{in1} amplitude. This is due to the fact that the voltage gain was calculated by dividing the amplitude of the output signal by the amplitude of v_{in1}. Moreover, the plots show that the voltage gain remains linear and almost constant, except for the plot of v_{in1}=2.5*sin(ωt)+3, for frequencies up to 50kHz. At higher frequencies, the voltage gain is almost linear and tends toward a single value for each plot. These characteristics are further shown in Figures 5.11, 5.12, and 5.13, which include the trend lines that best describe the data lines of Figures 5.8, 5.9, and 5.10, respectively.

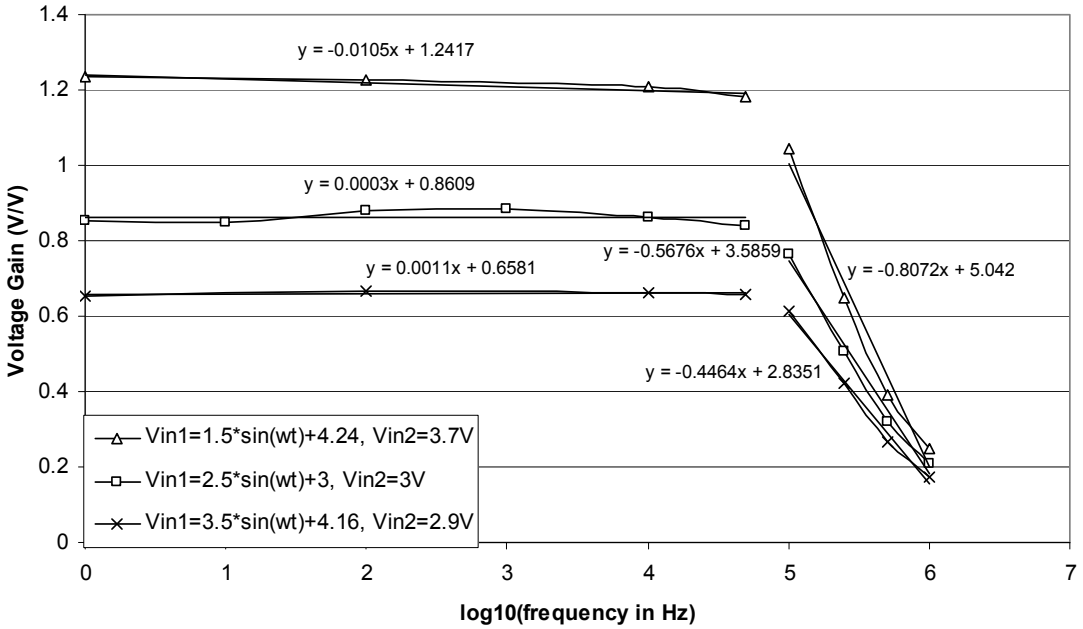

Figure 5.11 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three input signals with trend lines

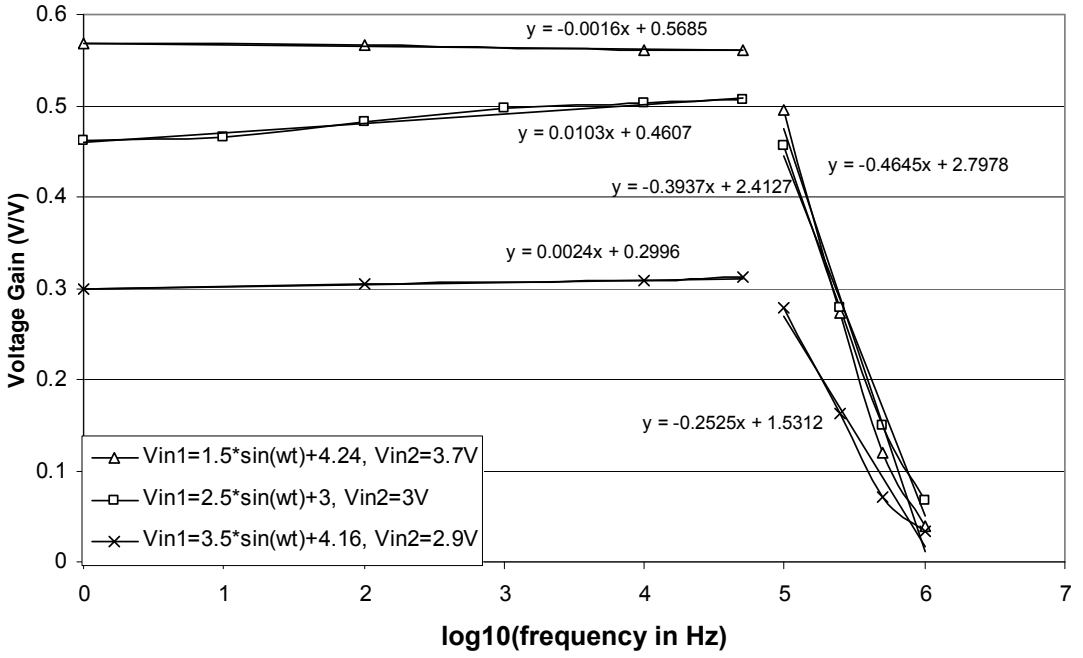

Figure 5.12 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three input signals with trend lines

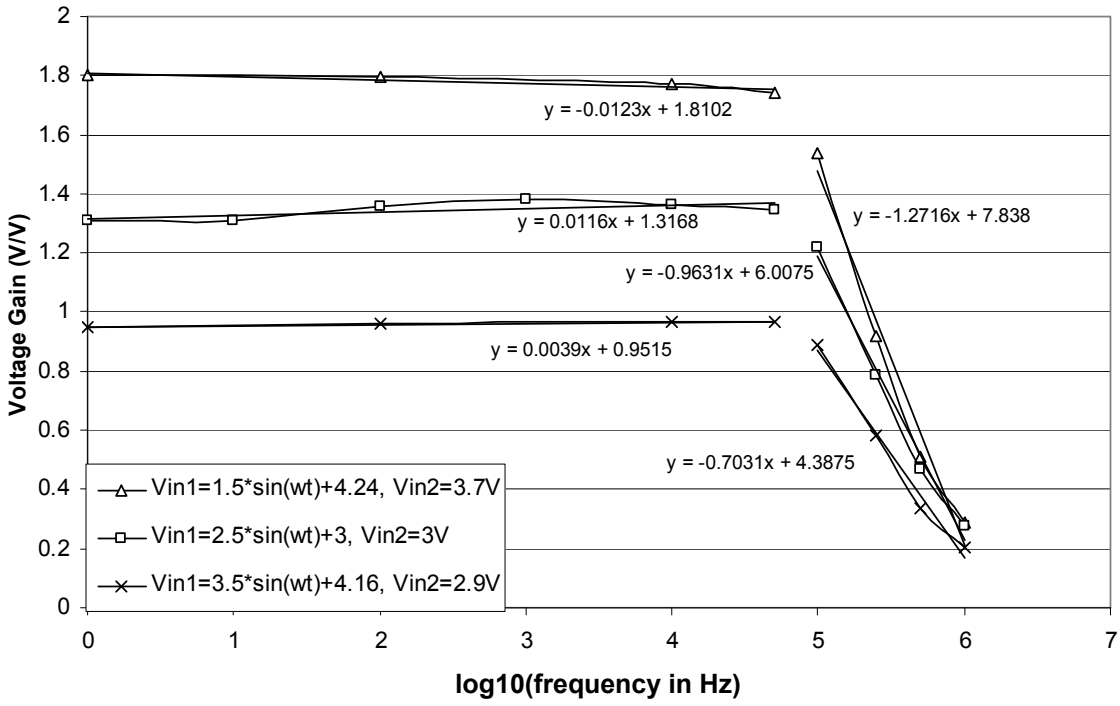

Figure 5.13 Plot of voltage gain of differential output vs. logarithm of frequency for three input signals with trend lines

The voltage gain plots with their trend lines confirm the already noted characteristics. Furthermore, these plots show that for the lower frequencies, the data lines are nearly parallel horizontal lines for v_{out1} and the differential output signal. For v_{out2}, the data lines for v_{in1}=1.5*sin(ωt)+4.24 and v_{in1}=3.5*sin(ωt)+4.16 are nearly horizontal, whereas, the data line for v_{in1}=2.5*sin(ωt)+3 has a visibly increasing slope. At higher frequencies, the trend lines are straight lines with negative slopes.

b. Effect of Resistance on Individual and Differential Phase Shifts and Voltage Gains

The effect of varying the load resistors R_1 and R_2 and the source resistor R_3 of the differential amplifier configuration shown in Figure 5.1 on the phase shift and voltage

gain of the output signals was next examined. Two cases were analyzed for the variation of each of the load and source resistors. First, a sinusoidal signal was applied at v_{in1} and V_{IN2} was a dc signal. In the second case, both input signals were sinusoidal.

i. The First Input Signal is Sinusoidal and the Second Input Signal is DC

In the first case, when R_1 and R_2 were varied, R_3 was set to 5kΩ, V_{DD} was 6V, and $V_{p,pos}$ of 6V was applied at the gates of both FeFETs. The input frequency was varied from 1Hz to 2.3MHz. Measurements were taken at R_1 and R_2 of 5kΩ, 10kΩ, and 15kΩ. When the load resistors were 5kΩ, v_{in1} was 1*sin(ωt)+4.10 and V_{IN2} was 4.5V. The input signal v_{in1} was 1*sin(ωt)+1.85 and V_{IN2} was 2.5V when R_1 and R_2 were 10kΩ. Finally, when the load resistors were 15kΩ, v_{in1} was 1*sin(ωt)+2.8 and V_{IN2} was 2.4V. The values of the offset voltage of v_{in1} and the values of V_{IN2} were selected so as to achieve the highest gain at the chosen value for the load resistors. Figures 5.14, 5.15, and 5.16 are plots of phase shift vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output, respectively.

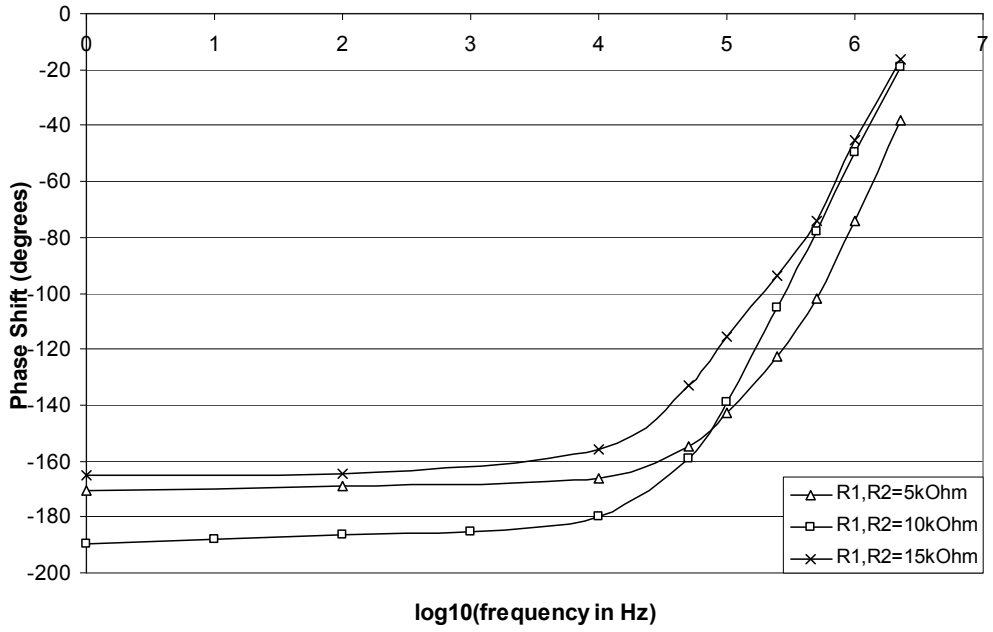

Figure 5.14 Plot of phase shift of v_{out1} vs. logarithm of frequency for three load resistors values

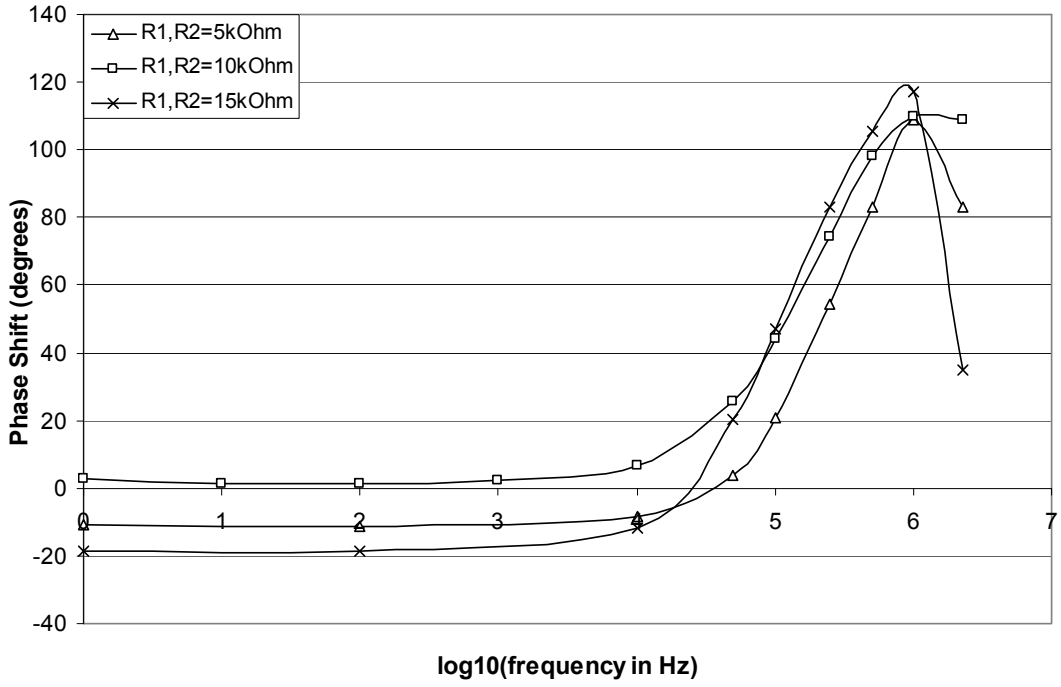

Figure 5.15 Plot of phase shift of v_{out2} vs. logarithm of frequency for three load resistors values

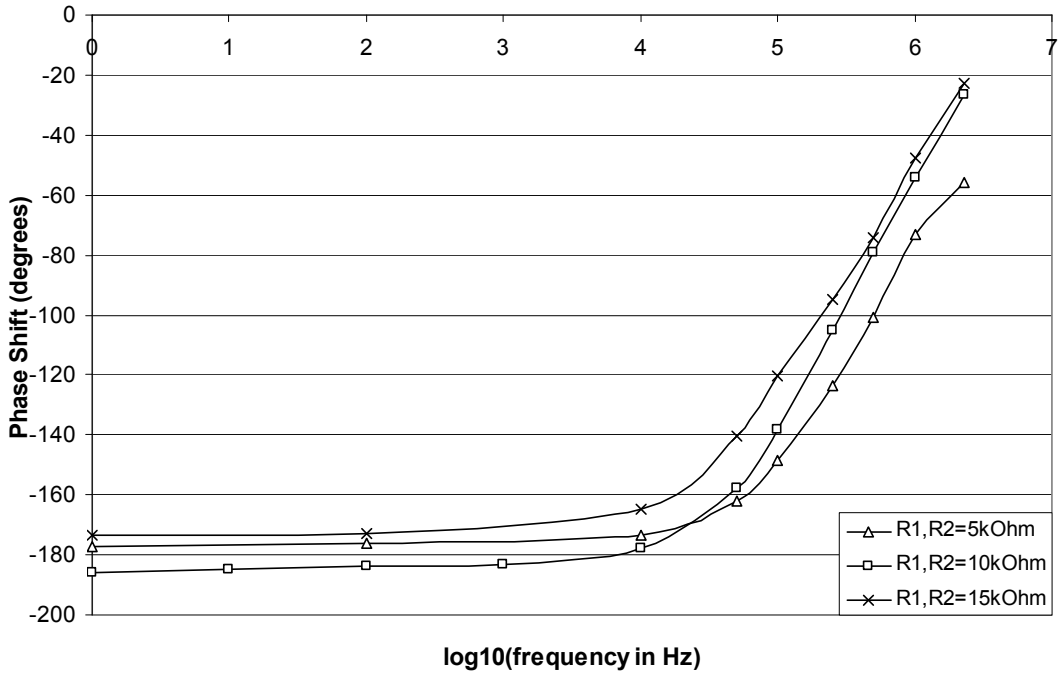

Figure 5.16 Plot of phase shift of differential output vs. logarithm of frequency for three load resistors values

The previous three plots do not display a particular trend between the magnitude of the phase shift and the value of the load resistors. However, the plots show that up to an input frequency of 10kHz, the data lines are nearly linear with a slightly increasing slope, whereas at the higher frequencies, the data lines have significant positive slopes. The only exception to this trend is the final value of the phase shift of the output signal v_{out2}. All the data lines of the plot of v_{out2}'s phase shift drop at an input frequency of 2.3MHz. These characteristics are reiterated in the plots of Figures 5.17 through 5.19, which show the phase shift vs. the logarithm of frequency plots with trend lines.

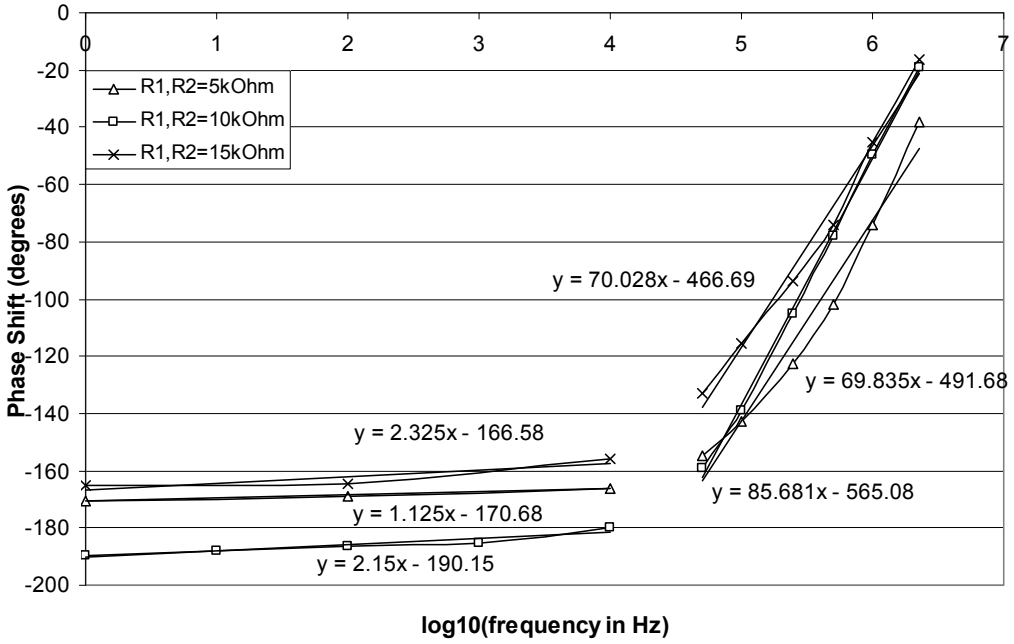

Figure 5.17 Plot of phase shift of v_{out1} vs. logarithm of frequency for three load resistors values with trend lines

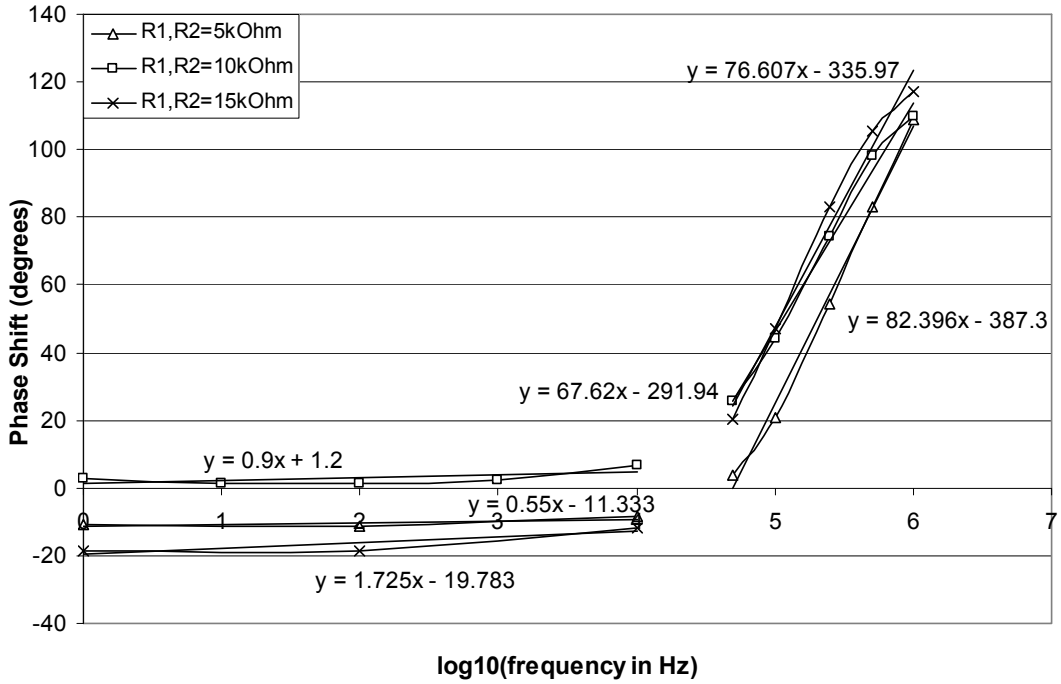

Figure 5.18 Plot of phase shift of v_{out2} vs. logarithm of frequency for three load resistors values with trend lines

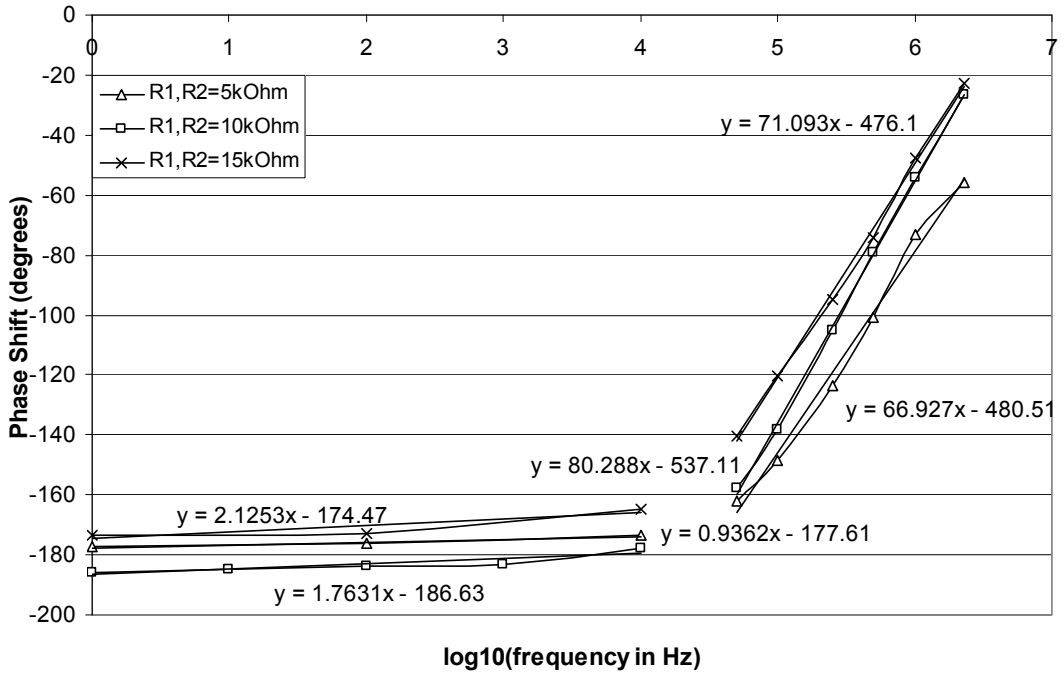

Figure 5.19 Plot of phase shift of differential output vs. logarithm of frequency for three load resistors values with trend lines

As seen from these plots, the trend lines confirm the characteristics displayed in the original plots. Figures 5.17 through 5.19 show that the trend lines for the lower frequencies are almost parallel. The same is true for the higher frequencies. Figure 5.18 shows that the data lines at high frequencies are almost linear if the phase shift value at 2.3MHz is ignored.

Next, the effect of varying the load resistors on the voltage gain was examined. All parameter values remained the same as before. Figures 5.20, 5.21, and 5.22 are plots of the voltage gain vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output signal, respectively.

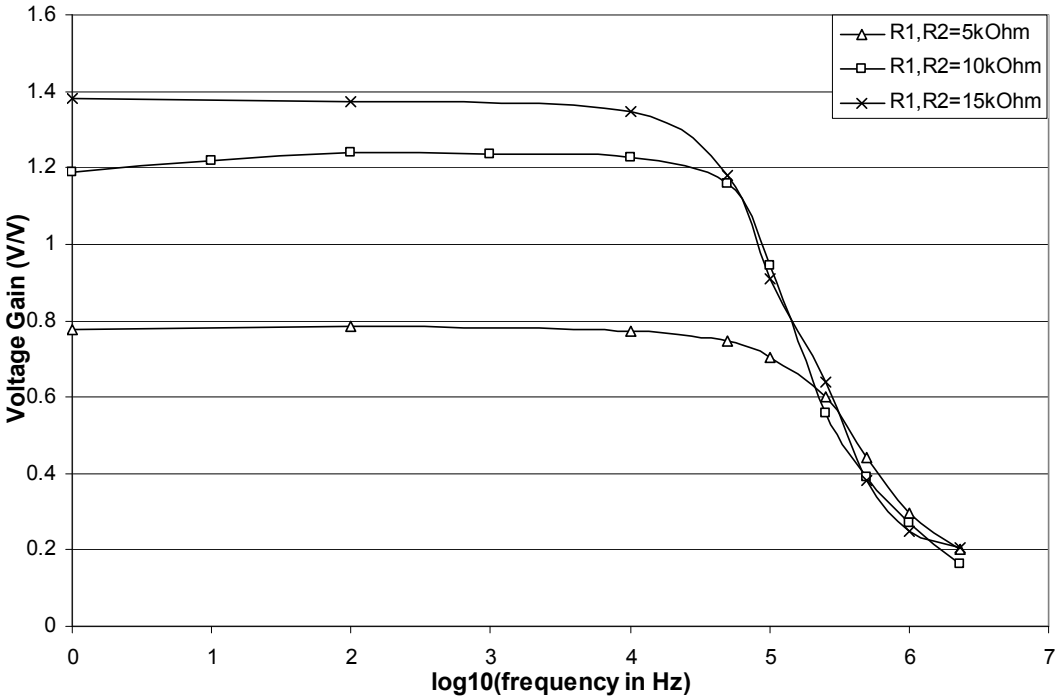

Figure 5.20 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three load resistors values

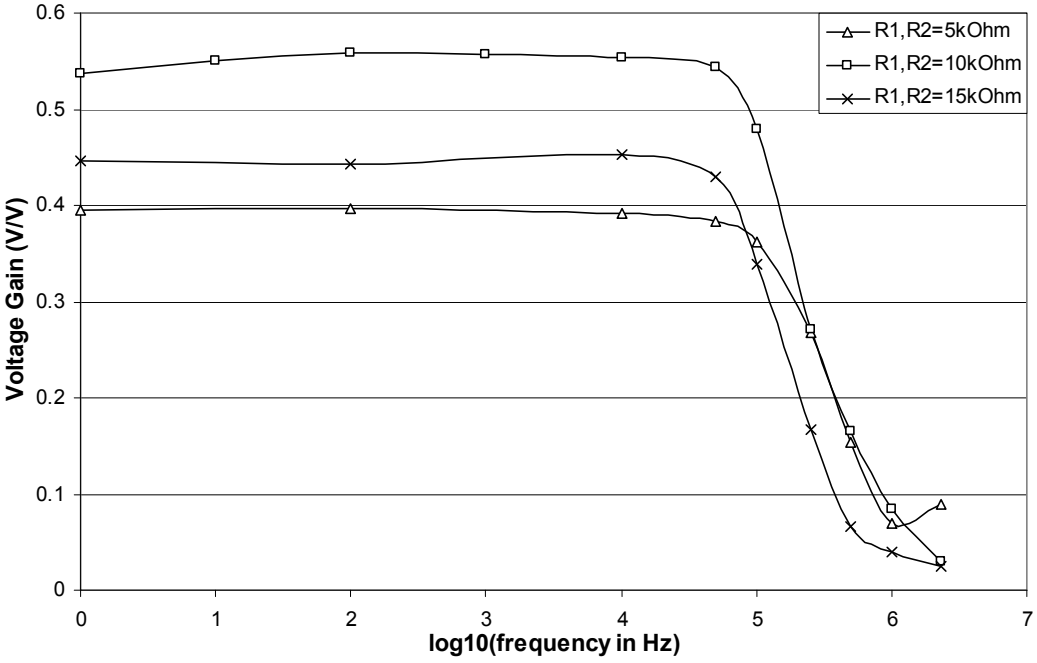

Figure 5.21 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three load resistors values

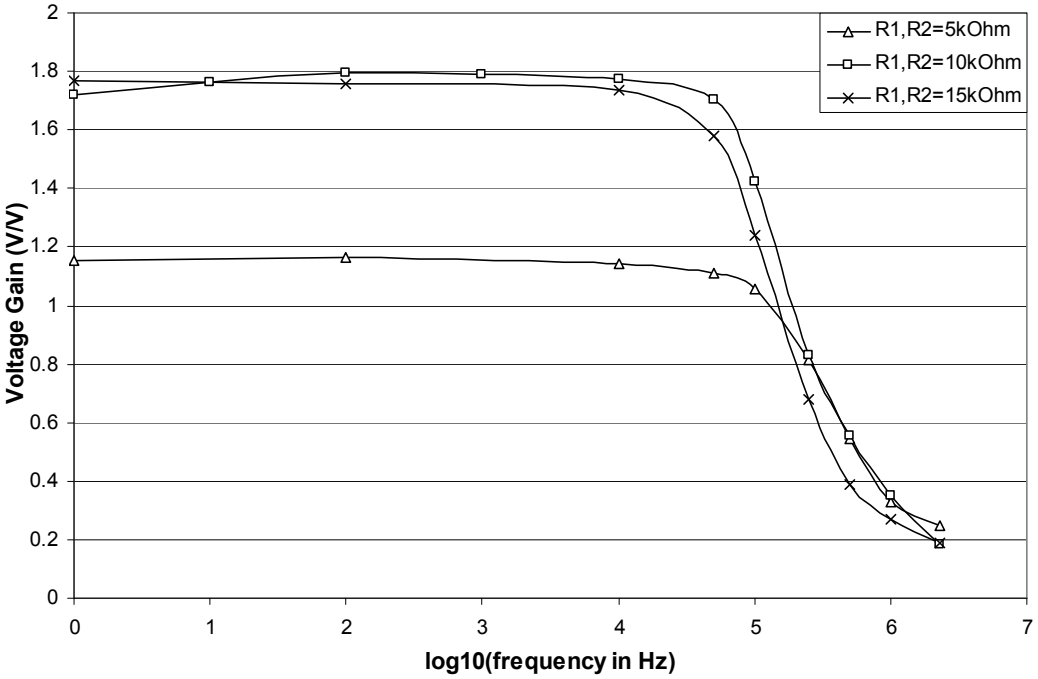

Figure 5.22 Plot of voltage gain of differential output vs. logarithm of frequency for three load resistors values

The plot of v_{out1}'s voltage gain shows that the voltage gain tends to increase with increasing load resistances. In the plot of the voltage gain of v_{out2}, the data line for the lowest load resistors has the lowest voltage gain at lower frequencies, but the voltage gain of the 15kΩ data is lower than that of the 10kΩ data. At higher frequencies, the data for the highest load resistors has the lowest voltage gain. Similarly, for the differential output plot, the lowest load resistances result in the lowest voltage gain at the lower frequencies, while the highest load resistances produce the lowest voltage gain at the higher frequencies. All the plots show that the data lines are nearly linear and horizontal at frequencies up to 10kHz and are almost straight lines with negative slopes at higher frequencies. Figures 5.23, 5.24, and 5.25 are the plots of the voltage gain vs. the logarithm of frequency with trend lines for v_{out1}, v_{out2}, and the differential output.

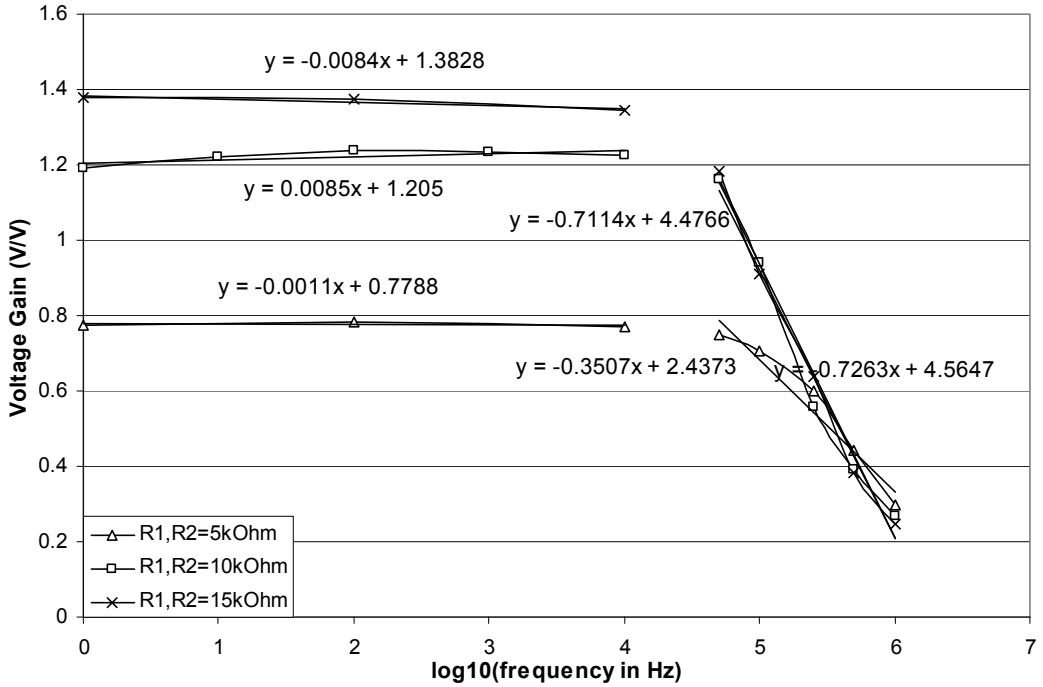

Figure 5.23 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three load resistors values with trend lines

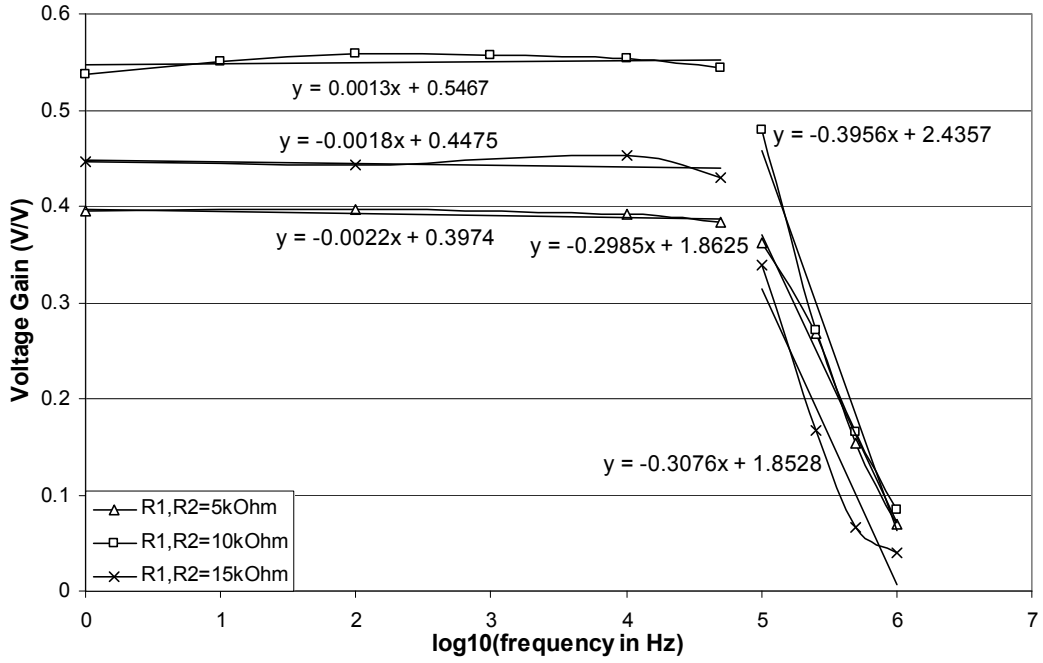

Figure 5.24 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three load resistors values with trend lines

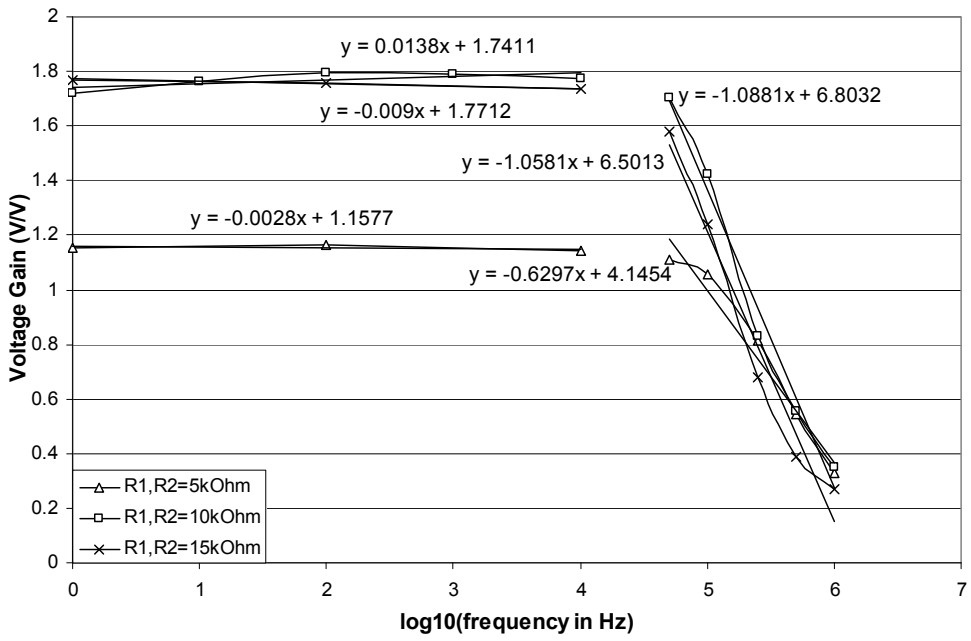

Figure 5.25 Plot of voltage gain of differential output vs. logarithm of frequency for three load resistors values with trend lines

The slopes of the trend lines at the lower frequencies are nearly zero, as was previously noted that the data lines are almost horizontal. Also, the slopes of the trend lines at higher frequencies are negative and similar in value.

Next, the source resistor, R_3, was varied. V_{DD} was kept at 6V and the gates of the FeFETs were positively polarized with $V_{p,pos}$ of 6V. The frequency ranged from 1Hz to 2.3MHz, and the values of R_3 examined were 2.5kΩ, 5kΩ, and 7.5kΩ. At R_3 of 2.5kΩ, v_{in1} was 1*sin(ωt)+1.5 and V_{IN2} was 2.5V. At R_3 of 5kΩ, vin1 was 1*sin(ωt)+2.8 and V_{IN2} was 2.4V. Lastly, at R_3 of 7.5kΩ, v_{in1} was 1*sin(ωt)+3.24 and V_{IN2} was set to 3.5V. Figures 5.26 through 5.28 are plots of the phase shift of the output signals vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output, respectively.

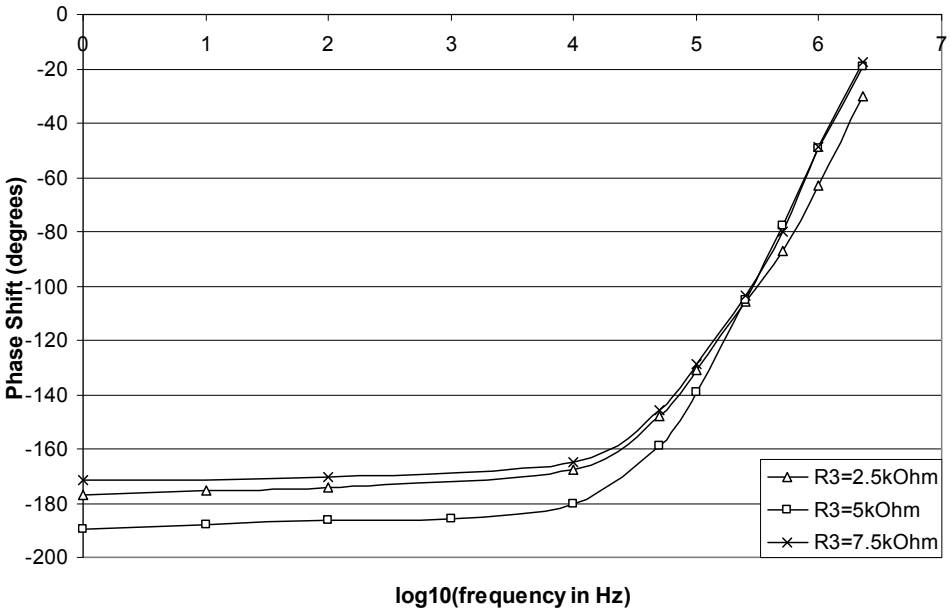

Figure 5.26 Plot of phase shift of v_{out1} vs. logarithm of frequency for three source resistor values

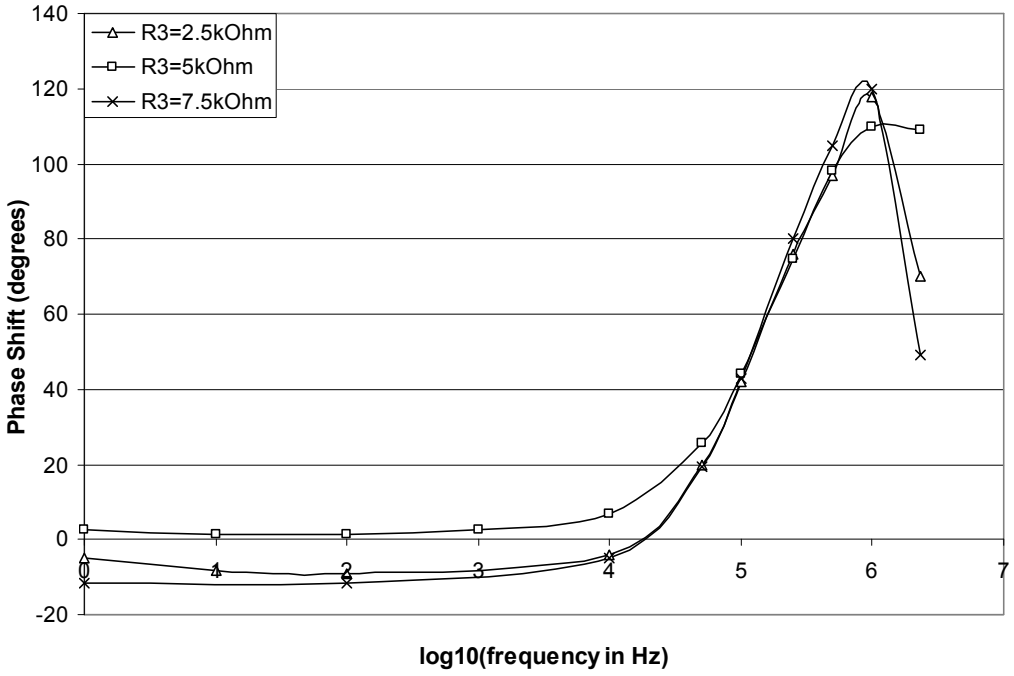

Figure 5.27 Plot of phase shift of v_{out2} vs. logarithm of frequency for three source resistor values

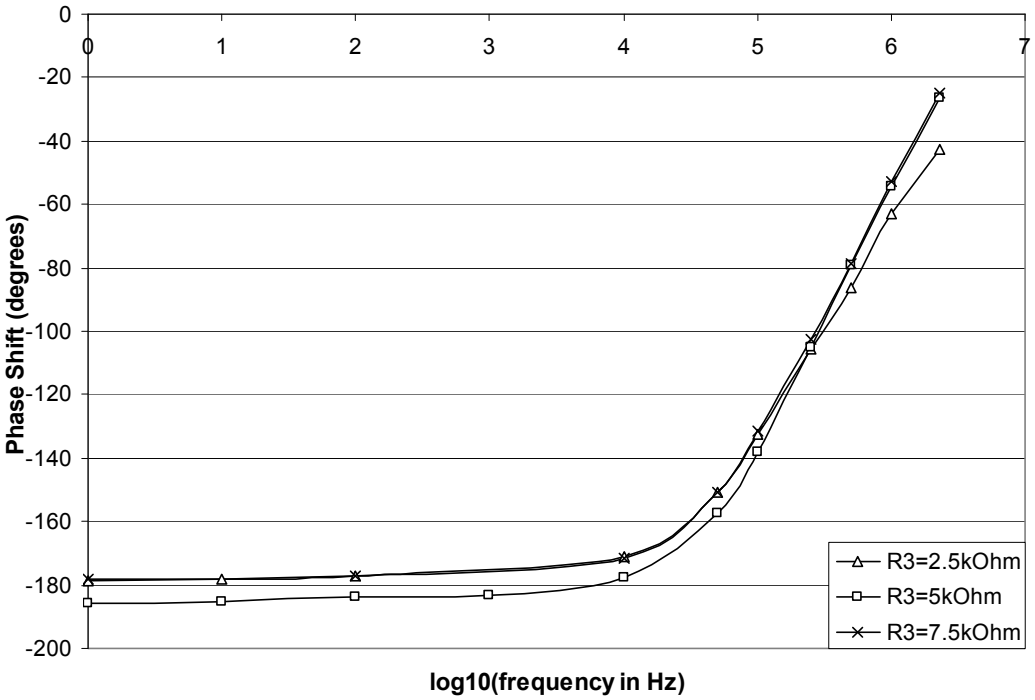

Figure 5.28 Plot of phase shift of differential output vs. logarithm of frequency for three source resistor values

The previous three plots show that the magnitude of the phase shift of the output signal has no direct correlation with the value of the source resistance. For example, the largest magnitude of phase shift of v_{out1} resulted from the 5kΩ source resistance, whereas the lowest phase shift magnitude occurred at R_3 of 7.5kΩ. However, all the plots show that up to an input frequency of 10kHz, the phase shift data lines are almost linear and horizontal. For the higher frequencies, the data lines are nearly linear with positive slopes if the last data point on the v_{out2} phase shift plot is ignored. Figures 5.29, 5.30, and 5.31 are the phase shift vs. logarithm of frequency plots with trend lines for v_{out1}, v_{out2}, and the differential output.

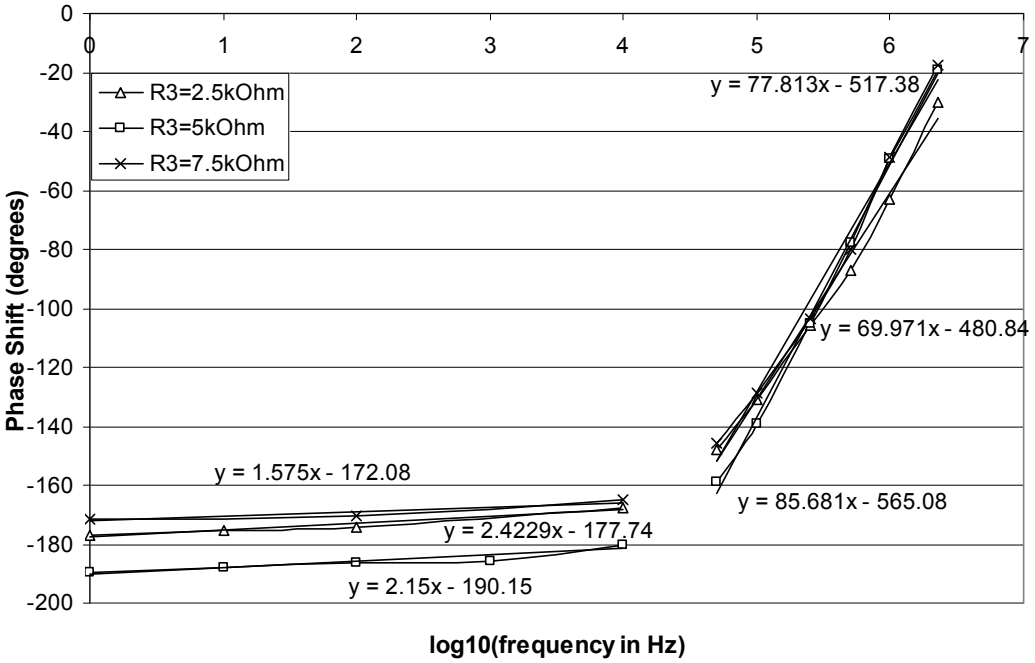

Figure 5.29 Plot of phase shift of v_{out1} vs. logarithm of frequency for three source resistor values with trend lines

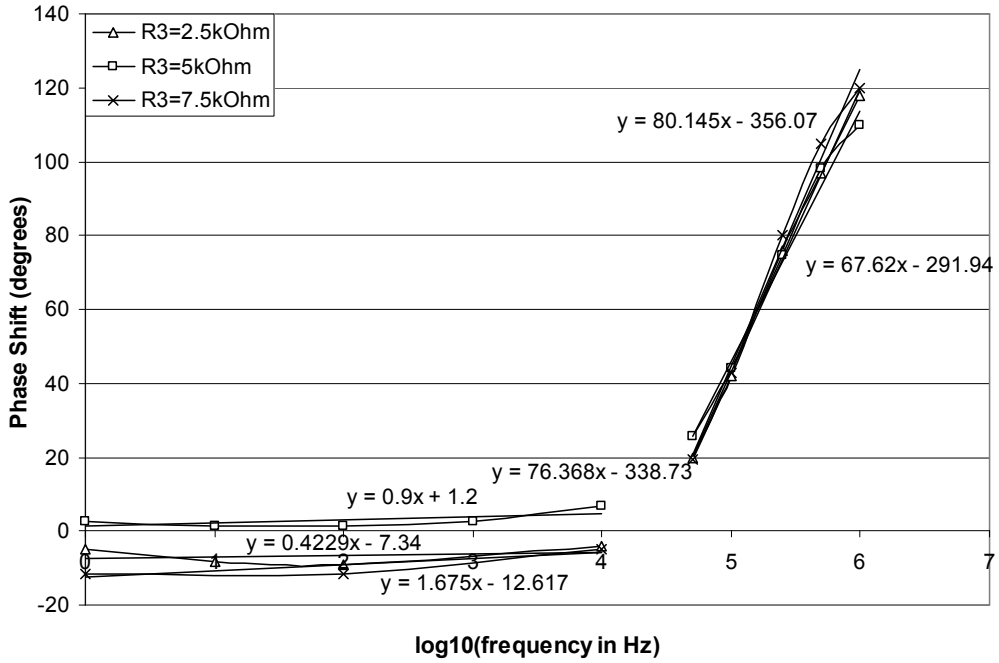

Figure 5.30 Plot of phase shift of v_{out2} vs. logarithm of frequency for three source resistor values with trend lines

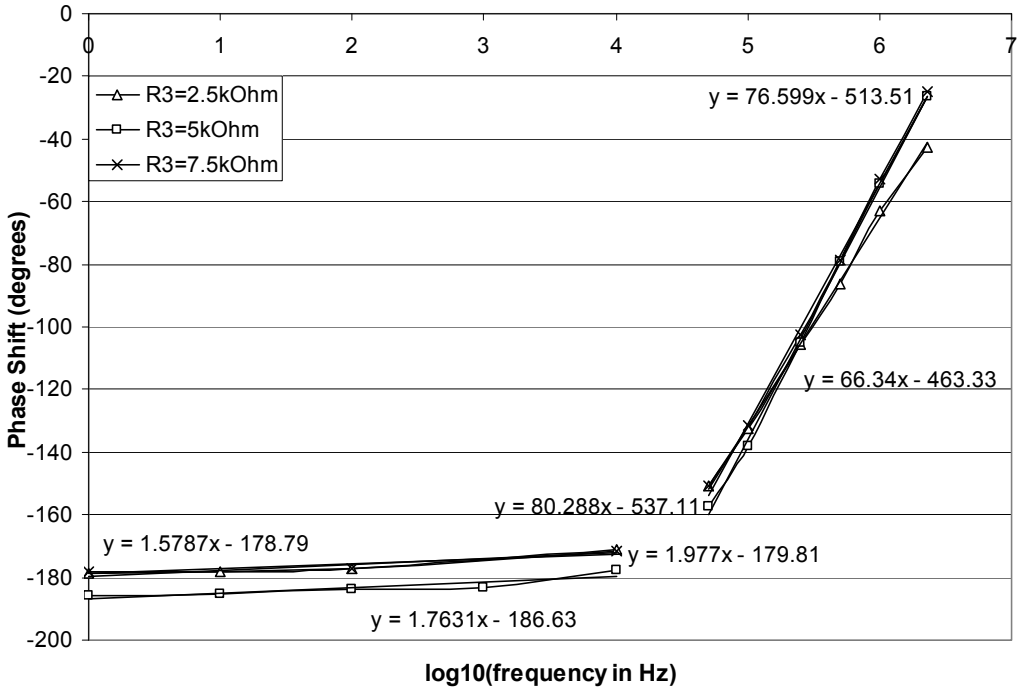

Figure 5.31 Plot of phase shift of differential output vs. logarithm of frequency for three source resistor values with trend lines

The trend lines of the previous plots show that the data lines for frequencies at or below 10kHz are close together and have very small positive slopes. The data lines at the higher frequencies are also very similar in shape and value if the last data point of the v_{out2} plot is ignored. Moreover, comparing the low-frequency data lines on all the plots shows that they all have similar slopes. This is also the case for the high-frequency data lines.

The effect of varying the source resistance on the voltage gain was next examined. All parameters remained unchanged. The plots of Figures 5.32, 5.33, and 5.34 show the voltage gain vs. the logarithm of the input frequency for v_{out1}, v_{out2}, and the differential output signal, respectively.

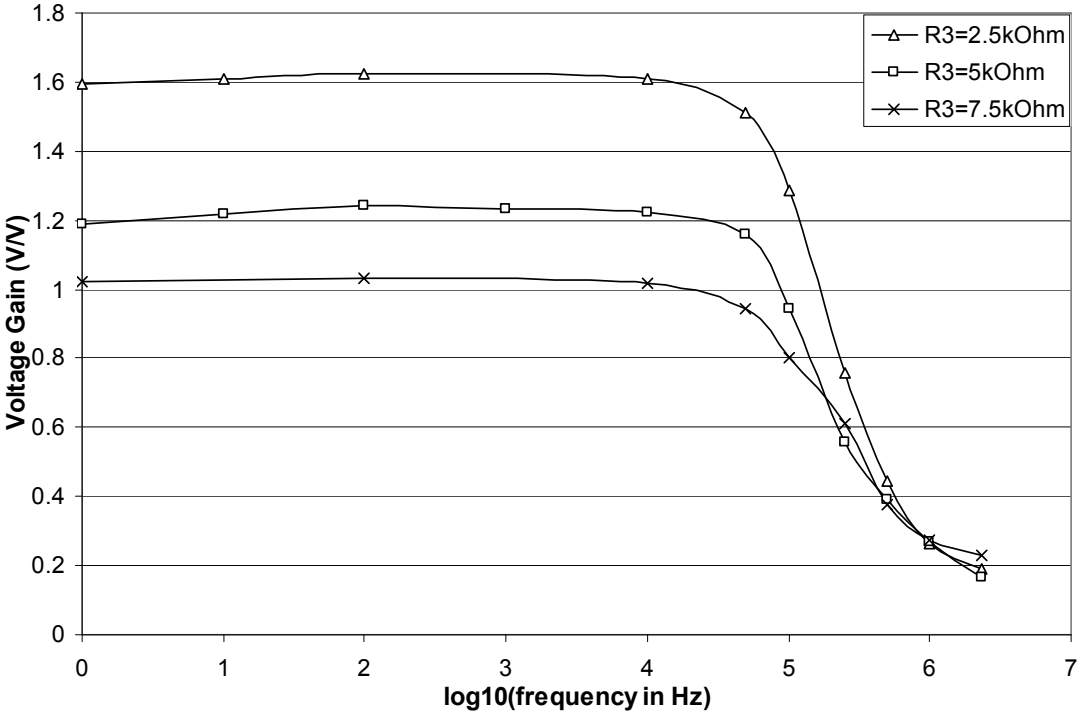

Figure 5.32 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three source resistor values

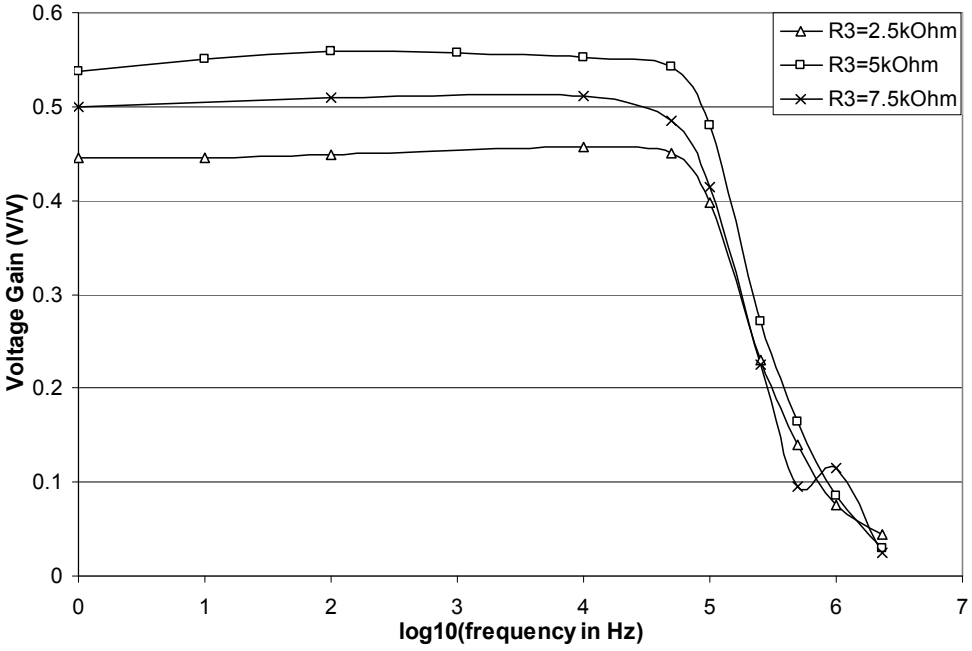

Figure 5.33 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three source resistor values

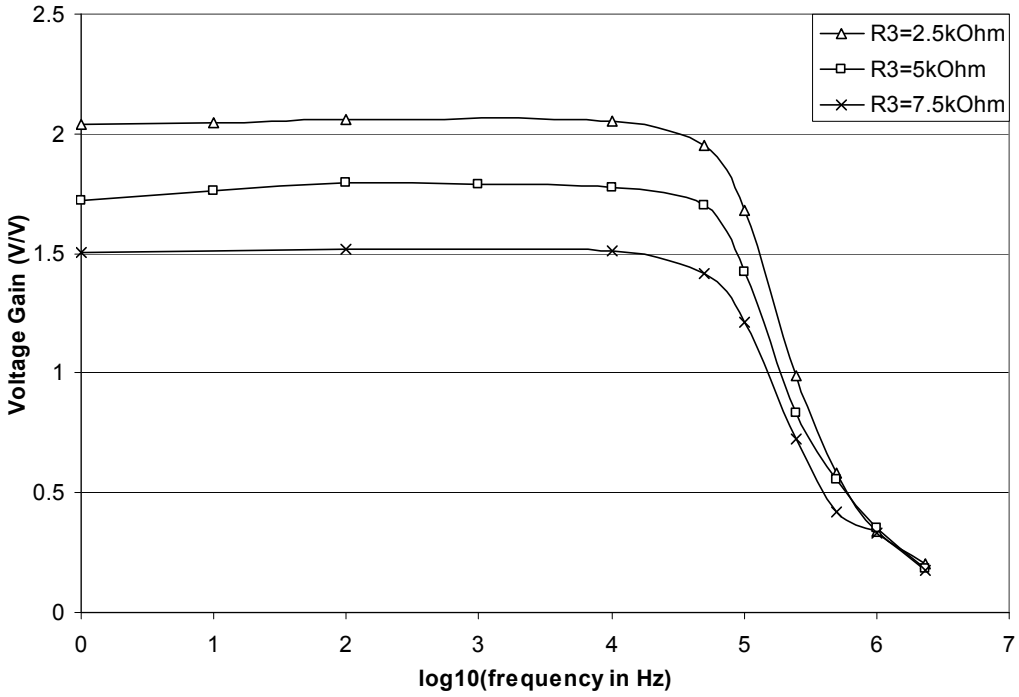

Figure 5.34 Plot of voltage gain of differential output vs. logarithm of frequency for three source resistor values

The v_{out1} and differential output plots show that the voltage gain increases with decreasing source resistance. In the v_{out2} plot, however, the lowest source resistance resulted in the lowest voltage gain, and the 5kΩ source resistance produced the highest voltage gain. All the plots are characterized by nearly horizontal data lines for frequencies up to 10kHz and almost linear lines with negative slopes for the higher frequencies. These observations are reinforced in the plots of Figures 5.35 through 5.37, which show the voltage gain vs. logarithm of frequency plots with trend lines for v_{out1}, v_{out2}, and the differential output, respectively.

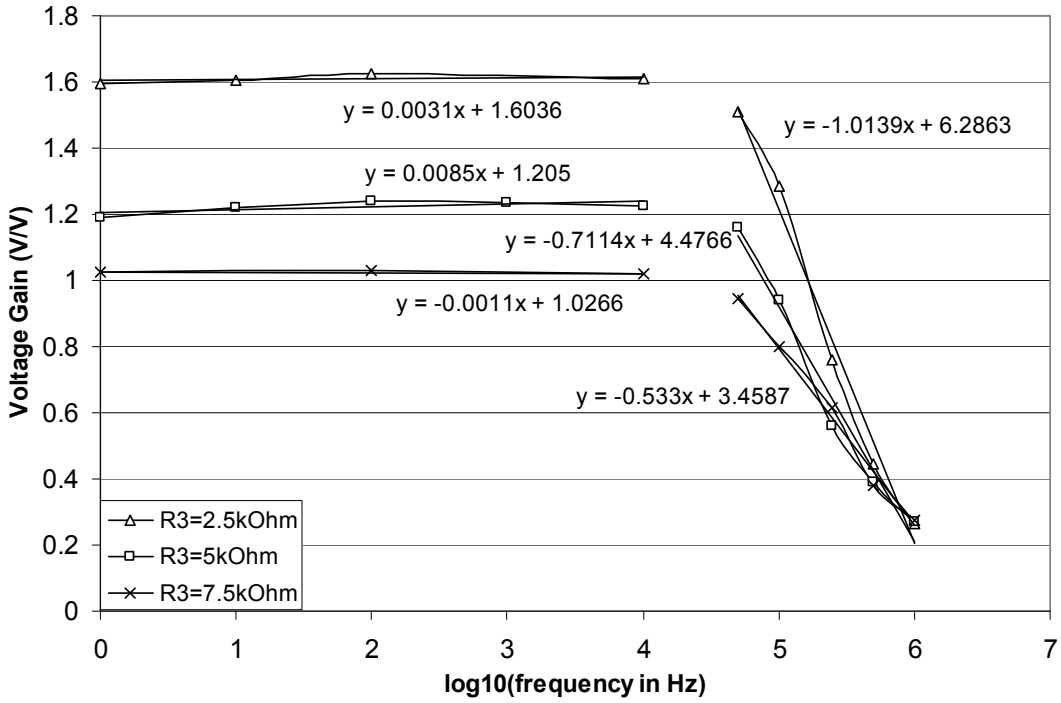

Figure 5.35 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three source resistor values with trend lines

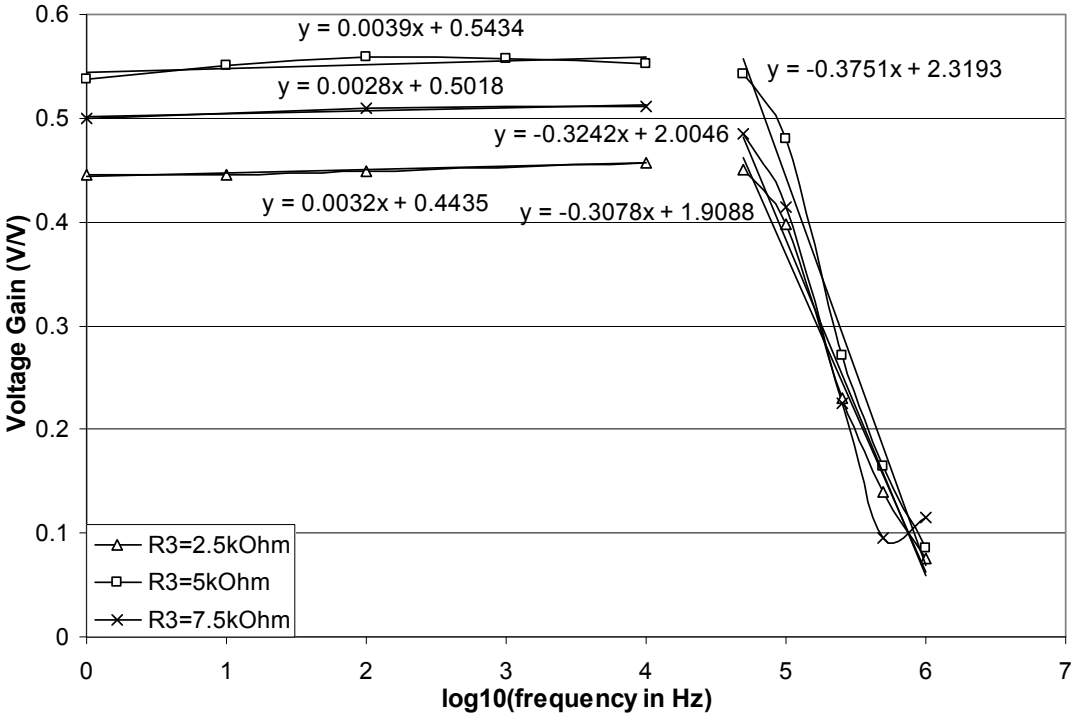

Figure 5.36 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three source resistor values with trend lines

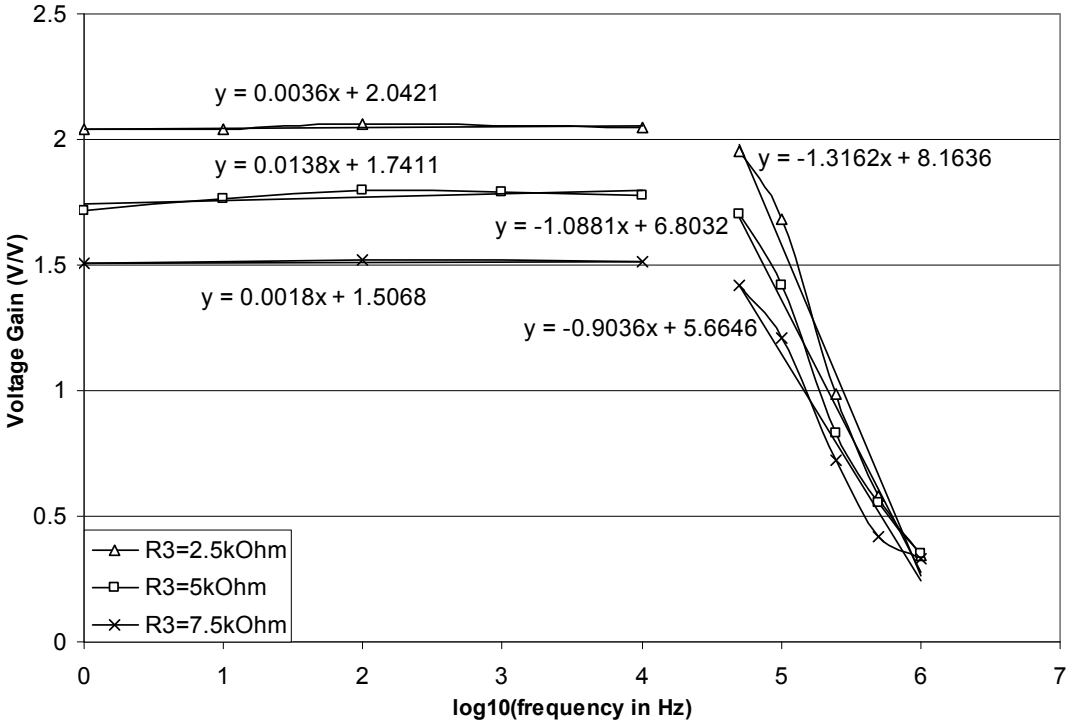

Figure 5.37 Plot of voltage gain of differential output vs. logarithm of frequency for three source resistor values with trend lines

Examining the voltage gain plots with their trend lines shows that all the low-frequency trend lines have nearly the same slopes in all the plots. The same is true for the high-frequency trend lines.

ii. Both Input Signals are Sinusoidal

Phase shift and voltage gain measurements were also carried out when both input signals were sinusoidal. First, the load resistors were varied, and the source resistance was set to 5kΩ. V_{DD} was 6V and $V_{p,pos}$ of 6V was applied to the gate of each FeFET. The input signals were chosen to be 180° out of phase. Thus, when R_1 and R_2 were set to 5kΩ, v_{in1} was 1*sin(ωt)+4.385 and v_{in2} was -1*sin(ωt)+4.385. At load resistors values of 10kΩ, v_{in1} was 1*sin(ωt)+2.819 and v_{in2} was -1*sin(ωt)+2.819. Finally, when R_1 and R_2 were 15kΩ, v_{in1} was set to 1*sin(ωt)+2.922 and v_{in2} was -1*sin(ωt)+2.922. Again, the

offset voltages included in v_{in1} and v_{in2} were selected so as to produce the highest voltage gain at the specified resistance. Figures 5.38, 5.39, and 5.40 are plots of the phase shift vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output, respectively.

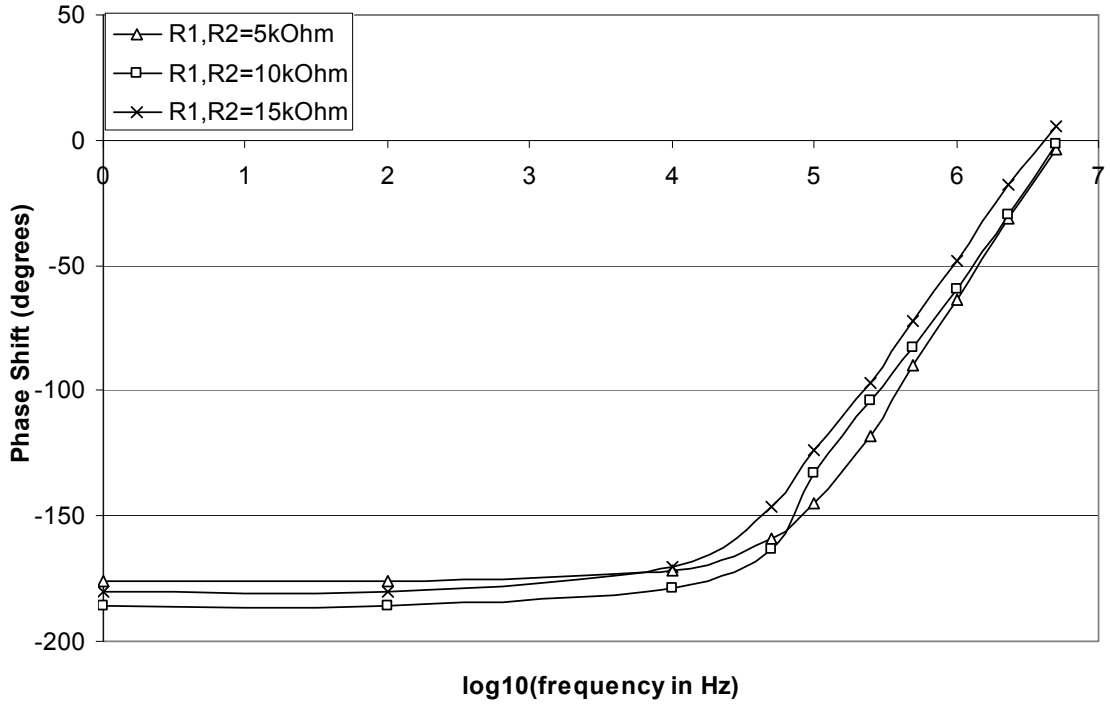

Figure 5.38 Plot of phase shift of v_{out1} vs. logarithm of frequency for three load resistors values

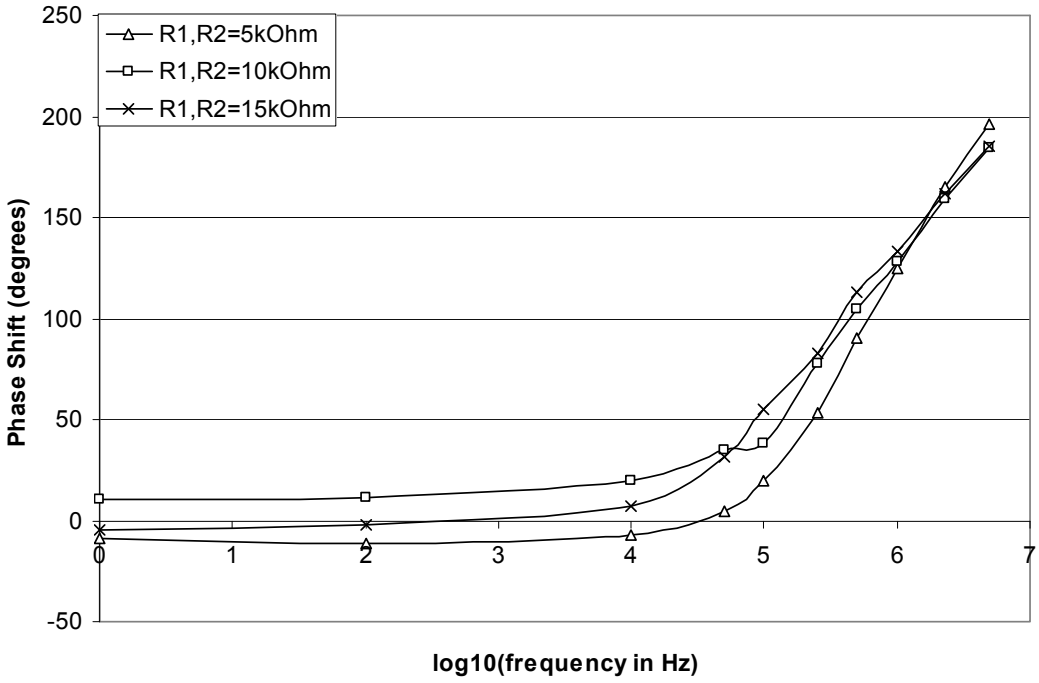

Figure 5.39 Plot of phase shift of v_{out2} vs. logarithm of frequency for three load resistors values

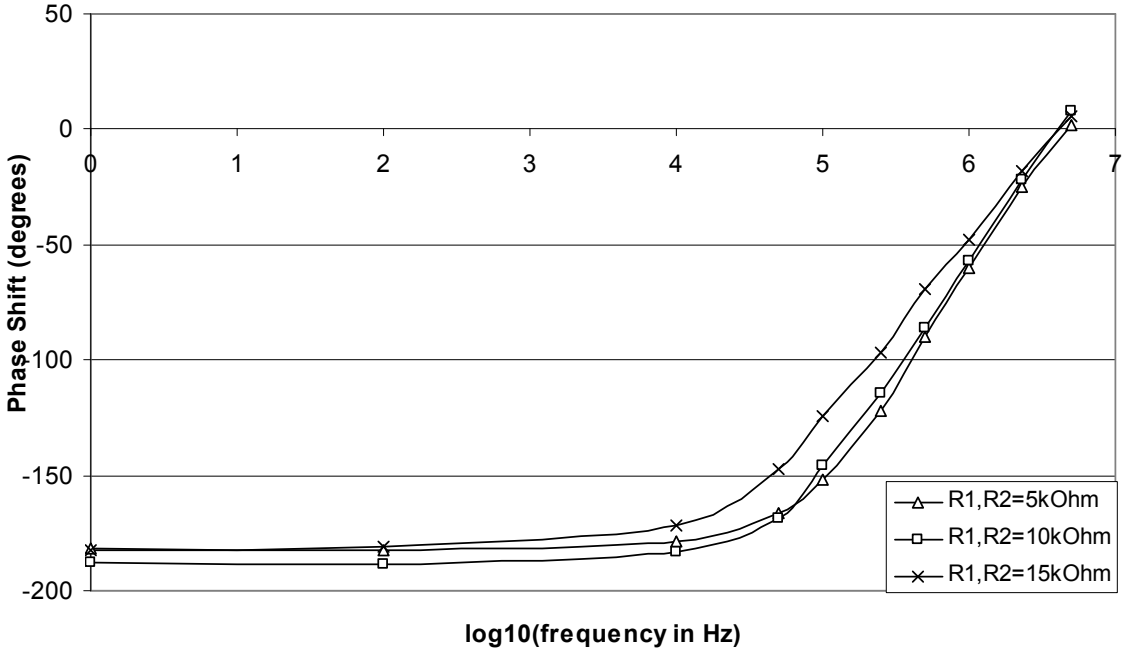

Figure 5.40 Plot of phase shift of differential output vs. logarithm of frequency for three load resistors values

As was noted with the sinusoidal v_{in1} and dc V_{IN2} plots, there is no direct correlation between the magnitude of the phase shift and the value of the load resistors. However, the three previous plots display a trend in the shape of the data lines. For input frequencies up to 10kHz, the data lines are nearly linear with a very small positive slope. For the higher frequencies, the data lines tend to be almost linear with a significant positive slope. The trend lines best describing the data lines and their slopes are shown in Figures 5.41, 5.42, and 5.43 for v_{out1}, v_{out2}, and the differential output, respectively.

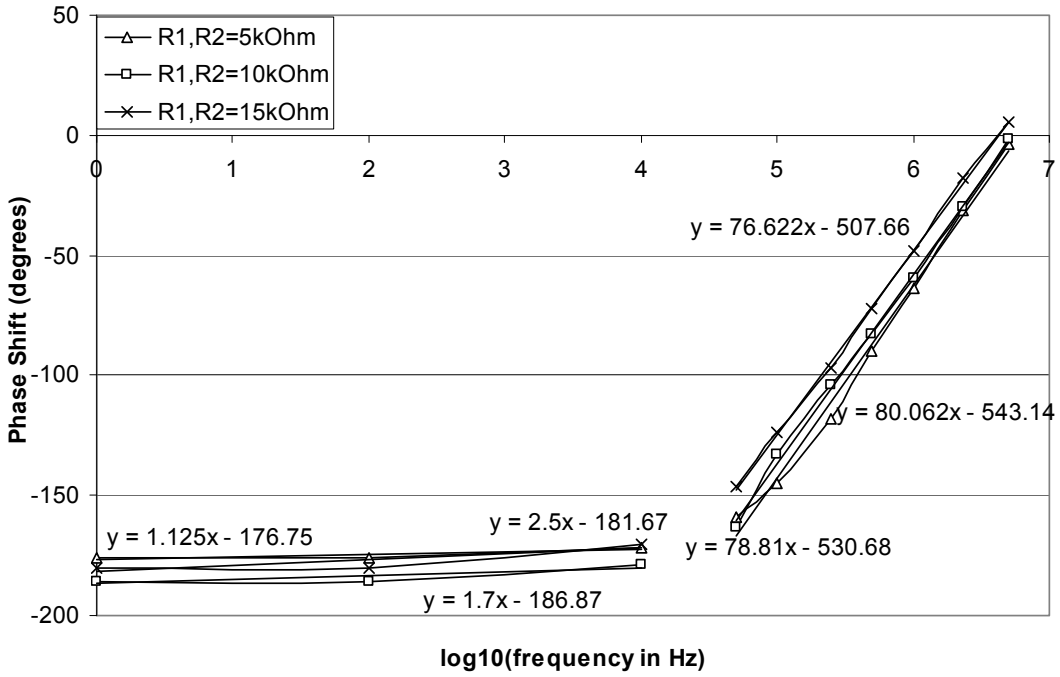

Figure 5.41 Plot of phase shift of v_{out1} vs. logarithm of frequency for three load resistors values with trend lines

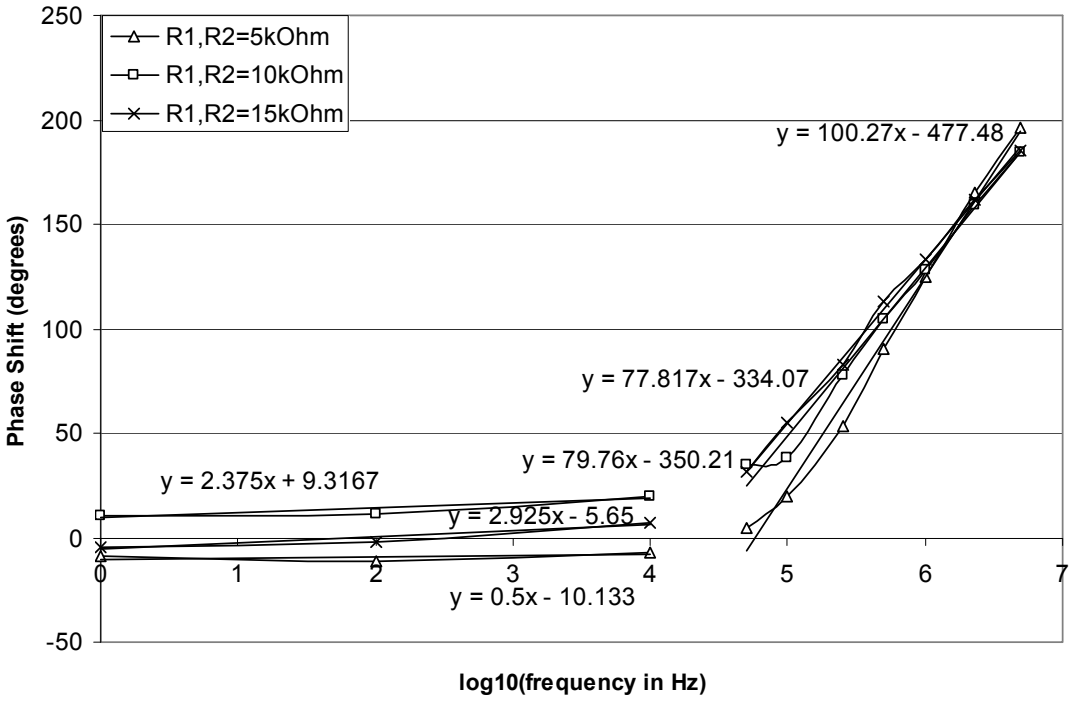

Figure 5.42 Plot of phase shift of v_{out2} vs. logarithm of frequency for three load resistors values with trend lines

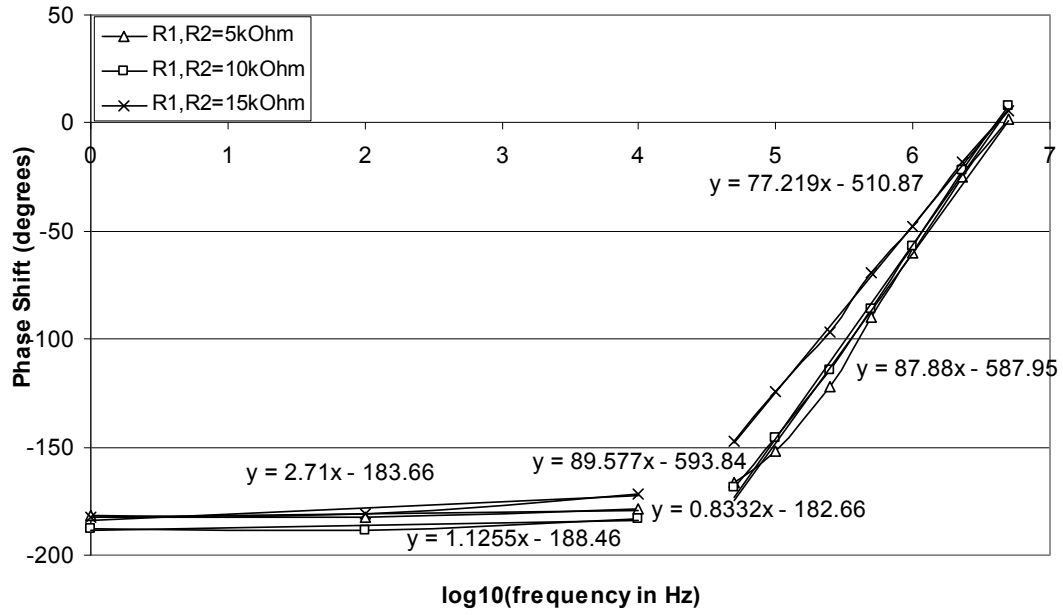

Figure 5.43 Plot of phase shift of differential output vs. logarithm of frequency for three load resistors values with trend lines

The trend lines of the previous figures show that the data lines at the low frequencies have very similar small slopes, while the high-frequency data lines have significantly larger slopes. Also, the slopes of the low-frequency data lines are similar for the v_{out1}, v_{out2}, and differential output plots. The same observation holds for the higher-frequency data lines.

The voltage gain was measured next. All parameter values remained unchanged. The voltage gain vs. the logarithm of frequency plots for v_{out1}, v_{out2}, and the differential output are shown in Figures 5.44, 5.45, and 5.46, respectively.

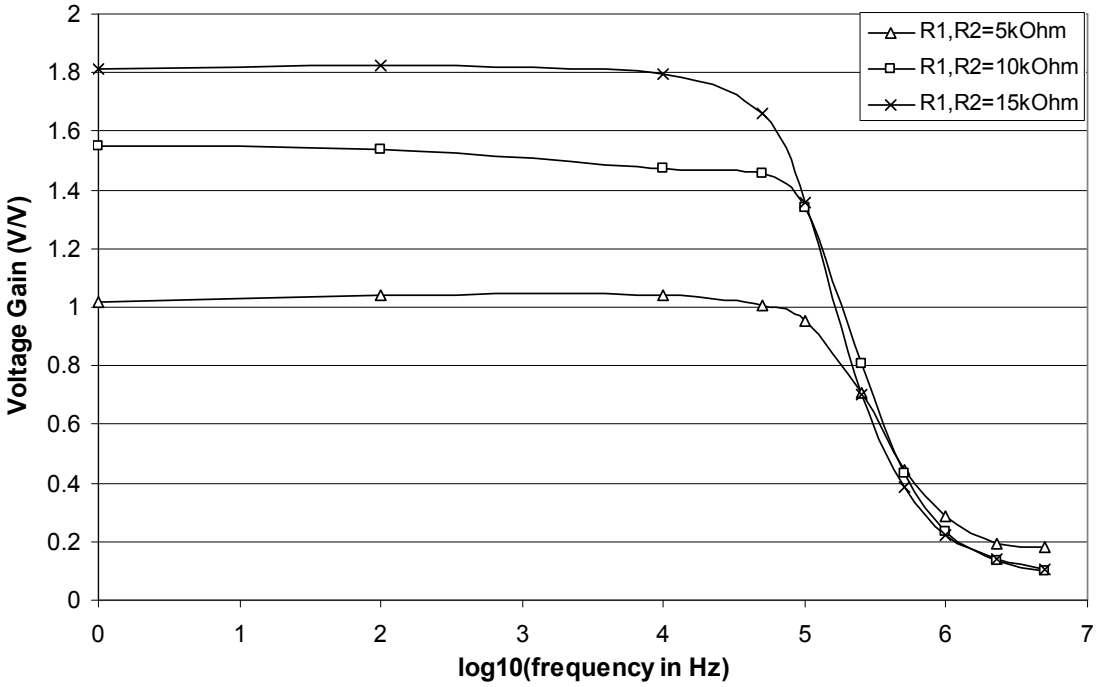

Figure 5.44 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three load resistors values

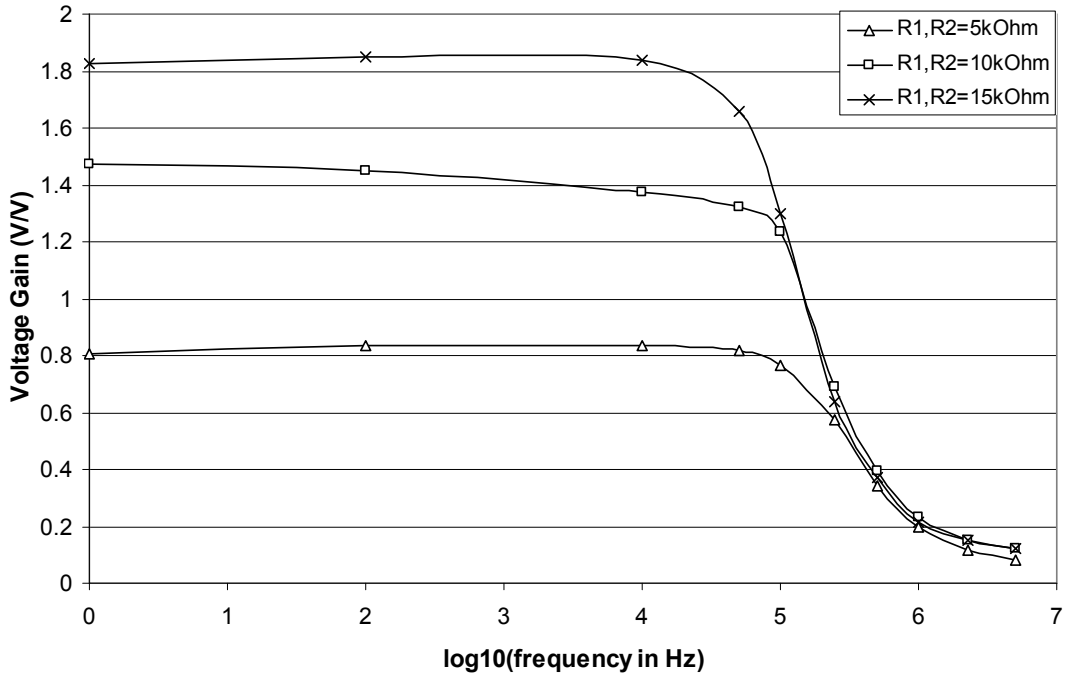

Figure 5.45 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three load resistors values

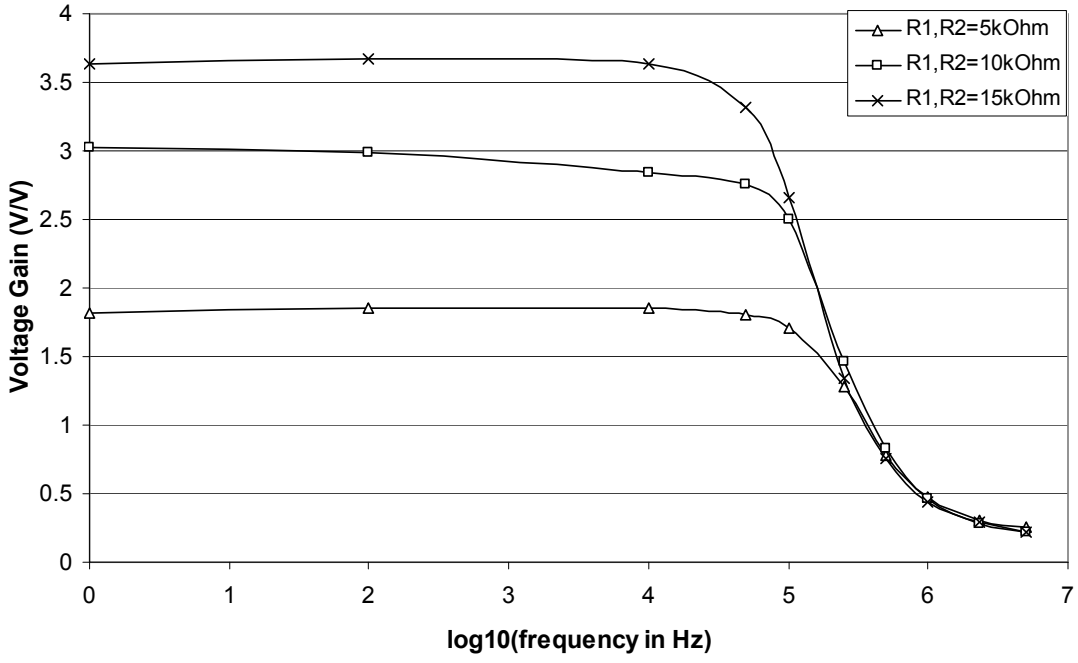

Figure 5.46 Plot of voltage gain of differential output vs. logarithm of frequency for three load resistors values

Unlike the voltage gain plots resulting from a constant V_{IN2}, these plots display a correlation between the value of the load resistors and the magnitude of the voltage gain. It can be seen that the voltage gain increases with increasing load resistance. Another difference between these voltage gain plots and those resulting from a dc V_{IN2} is the exponential shape of the high-frequency portion of the data lines. This observation is further illustrated in Figures 5.47, 5.48, and 5.49, which show the trend lines estimating the data lines of the voltage gain of v_{out1}, v_{out2}, and the differential output, respectively.

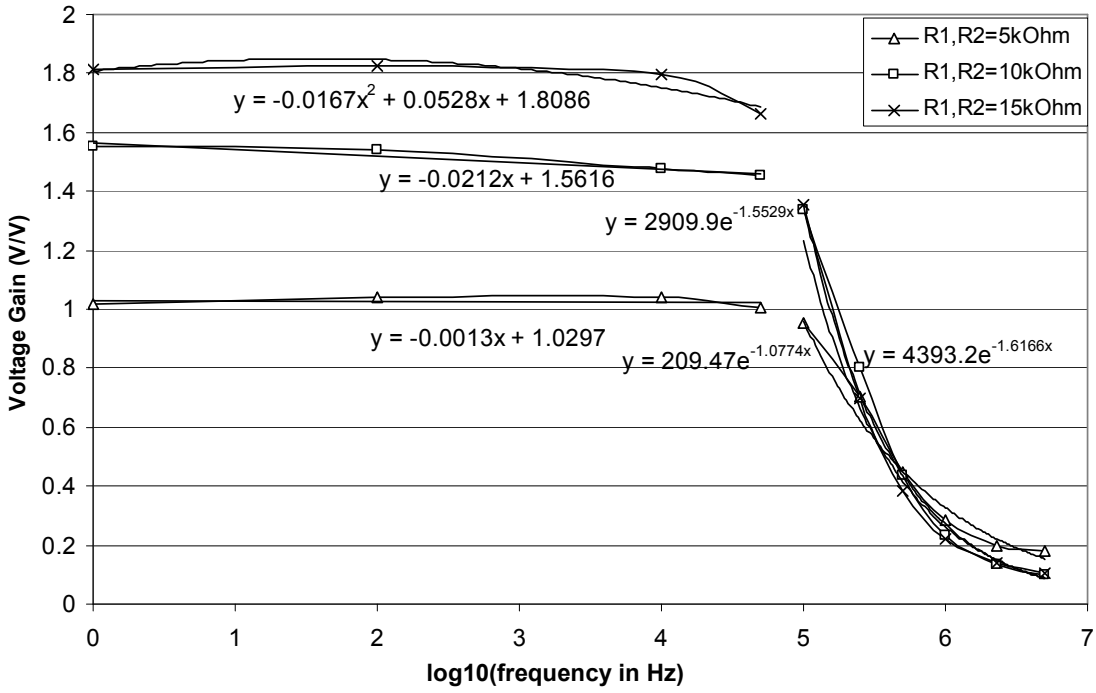

Figure 5.47 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three load resistors values with trend lines

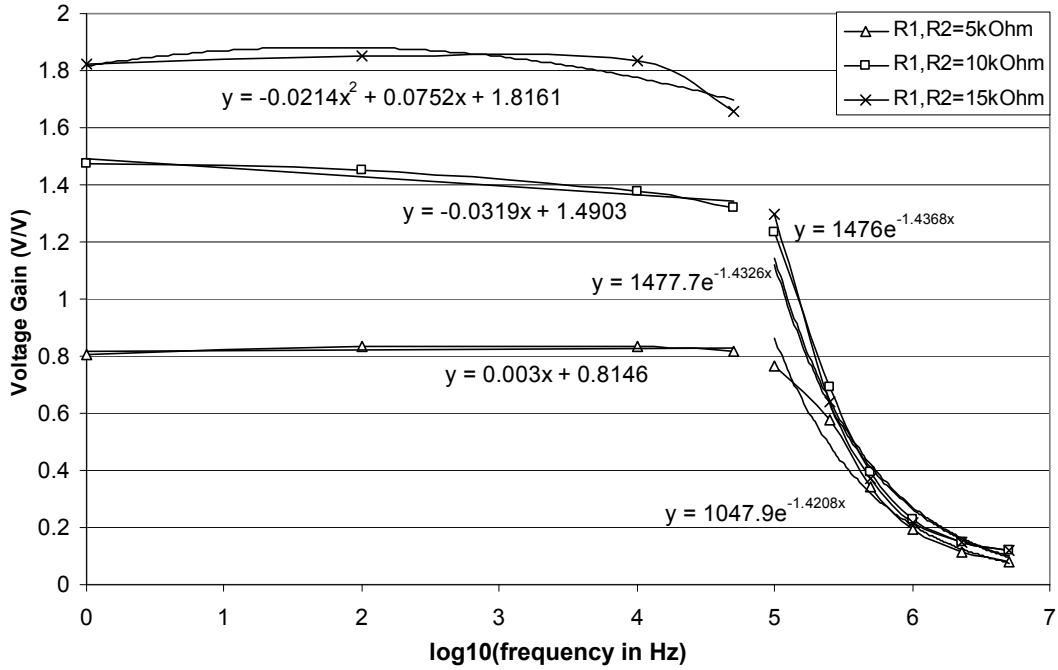

Figure 5.48 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three load resistors values with trend lines

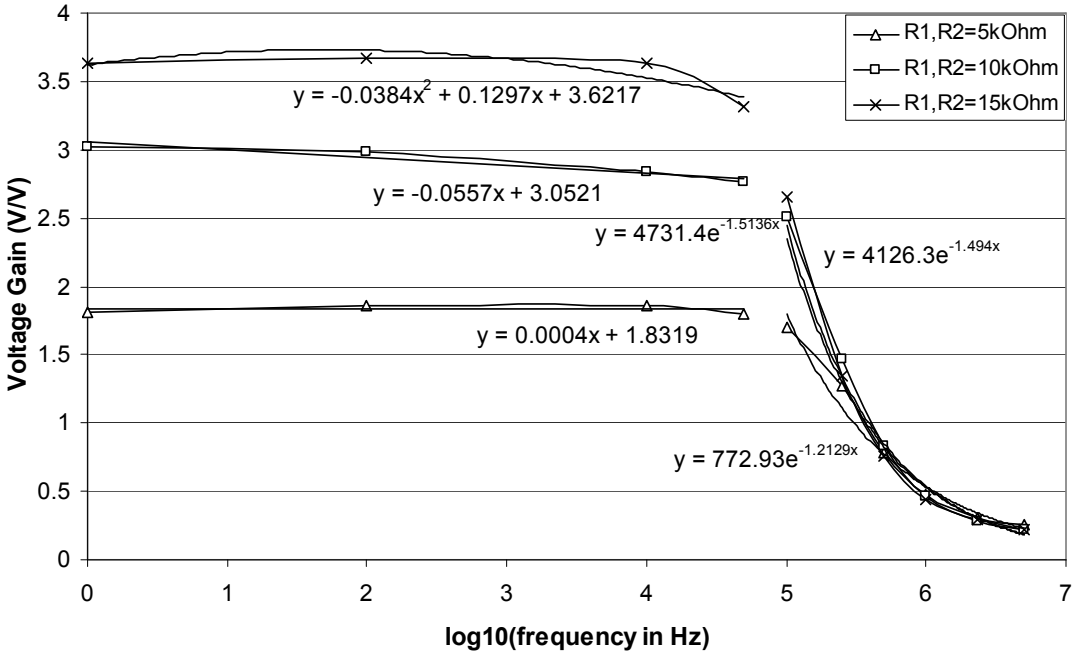

Figure 5.49 Plot of voltage gain of differential output vs. logarithm of frequency for three load resistors values with trend lines

As was previously noted, the trend lines describing the data lines starting from 100kHz are exponential. The lower-frequency portions of the 5kΩ and 10kΩ data lines are nearly linear and horizontal. However, the 15kΩ data line up to 50kHz is best described by a parabolic trend line. The equation of the lower-frequency 15kΩ trend line is similar on all the plots.

The effect of changing the source resistance on the phase shift and voltage gain of the output signals was also studied. Measurements were taken at R_3 of 2.5kΩ, 5kΩ, and 7.5kΩ. V_{DD} remained at 6V, R_1 and R_2 were 10kΩ, and $V_{p,pos}$ of 6V was applied at each FeFET's gate. As was the case when the load resistors were varied, the input signals were about 180° out of phase. When R_3 was 2.5kΩ, v_{in1} was 1*sin(ωt)+3 and v_{in2} was -1*sin(ωt)+3. When the source resistor was 5kΩ, v_{in1} was set to 1*sin(ωt)+2.819 and v_{in2} was -1*sin(ωt)+2.819. Finally, at R_3 of 7.5kΩ, v_{in1} was 1*sin(ωt)+4.078 and v_{in2} was -1*sin(ωt)+3.593. The plots of phase shift vs. logarithm of frequency for v_{out1}, v_{out2}, and the differential output are shown in Figures 5.50, 5.51, and 5.52, respectively.

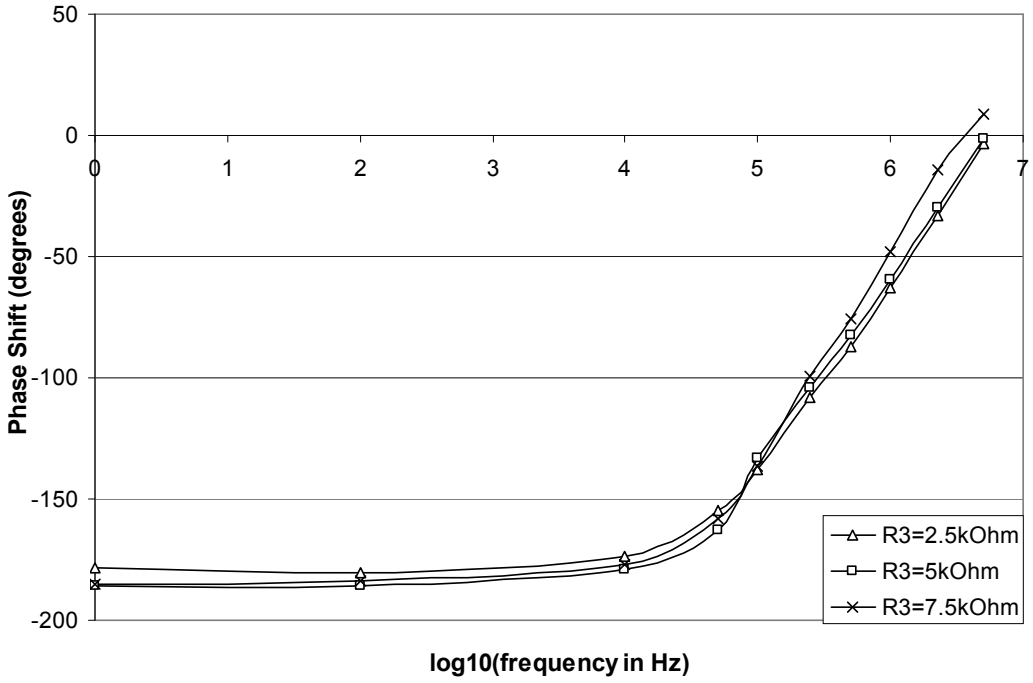

Figure 5.50 Plot of phase shift of v_{out1} vs. logarithm of frequency for three source resistor values

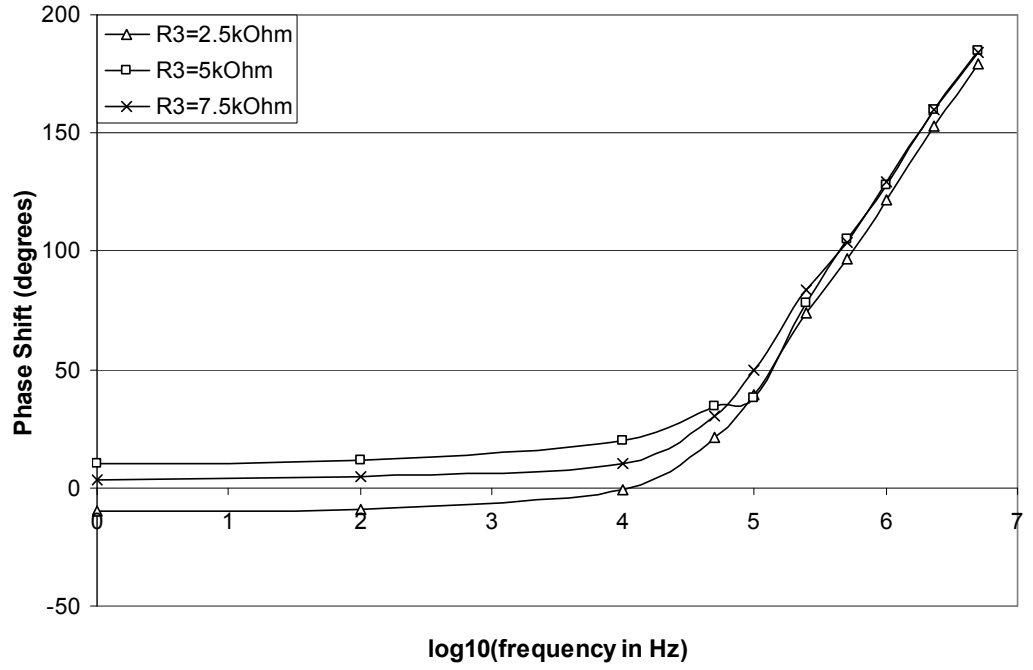

Figure 5.51 Plot of phase shift of v_{out2} vs. logarithm of frequency for three source resistor values

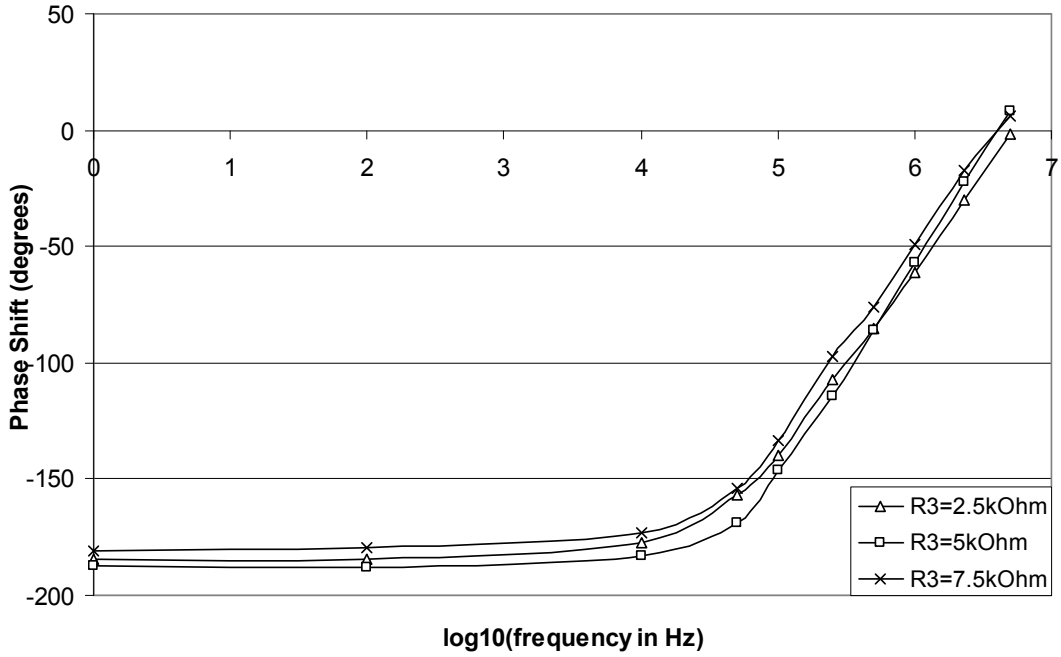

Figure 5.52 Plot of phase shift of differential output vs. logarithm of frequency for three source resistor values

The previous phase shift plots do not display a relationship between the magnitude of the phase shift and the value of the source resistor. However, all the plots are characterized by almost linear data lines with small positive slopes for frequencies up to 10kHz. At the higher frequencies, the data lines are also almost linear but with higher positive slopes. Figures 5.53 through 5.55 show the trend lines that best fit the data lines for the phase shift of v_{out1}, v_{out2}, and the differential output, respectively.

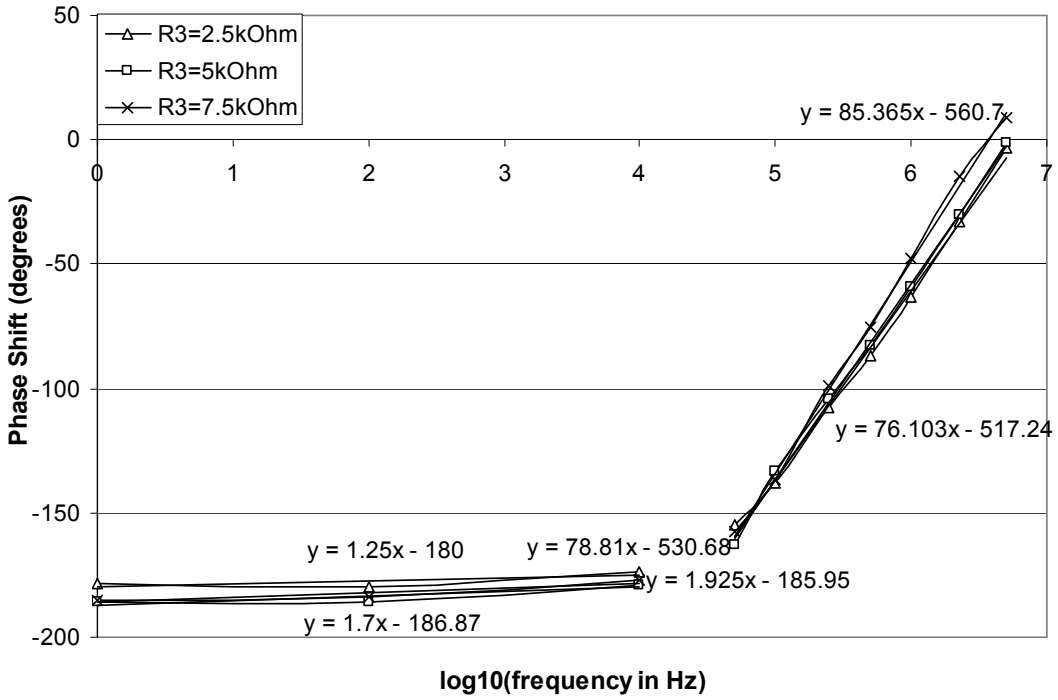

Figure 5.53 Plot of phase shift of v_{out1} vs. logarithm of frequency for three source resistor values with trend lines

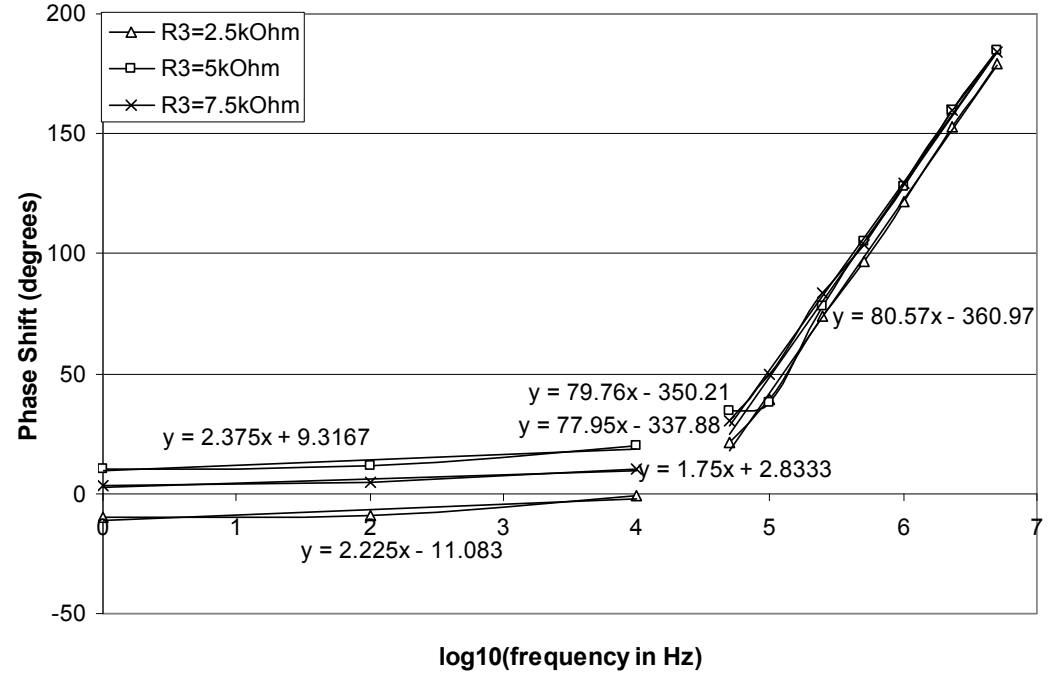

Figure 5.54 Plot of phase shift of v_{out2} vs. logarithm of frequency for three source resistor values with trend lines

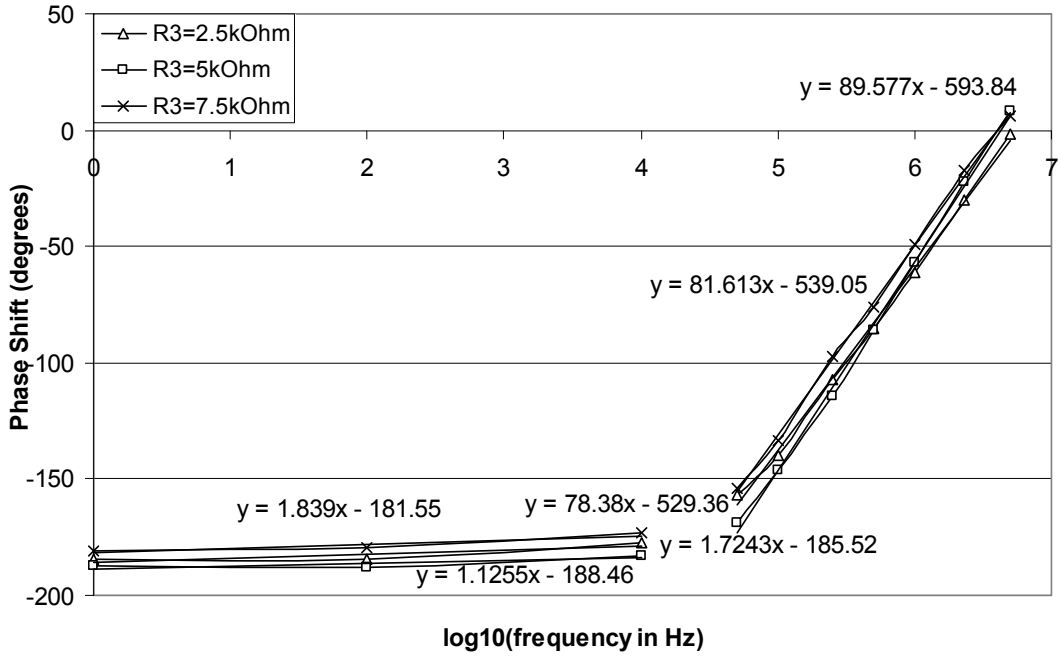

Figure 5.55 Plot of phase shift of differential output vs. logarithm of frequency for three source resistor values with trend lines

The trend lines of the previous plots show that the low-frequency portions of the data lines are nearly linear and their trend lines have small positive slopes. For the trend lines of the high-frequency portions of the data lines, the slopes are significantly larger. Moreover, the slopes of the low-frequency trend lines are similar in all the graphs. The same is true for the high-frequency trend lines.

Lastly, the effect of the source resistance on the voltage gain of the differential amplifier with sinusoidal v_{in1} and v_{in2} was analyzed. The parameters remained unchanged. The plots of voltage gain vs. the logarithm of frequency for v_{out1}, v_{out2}, and the differential output are shown in Figures 5.56, 5.57, and 5.58, respectively.

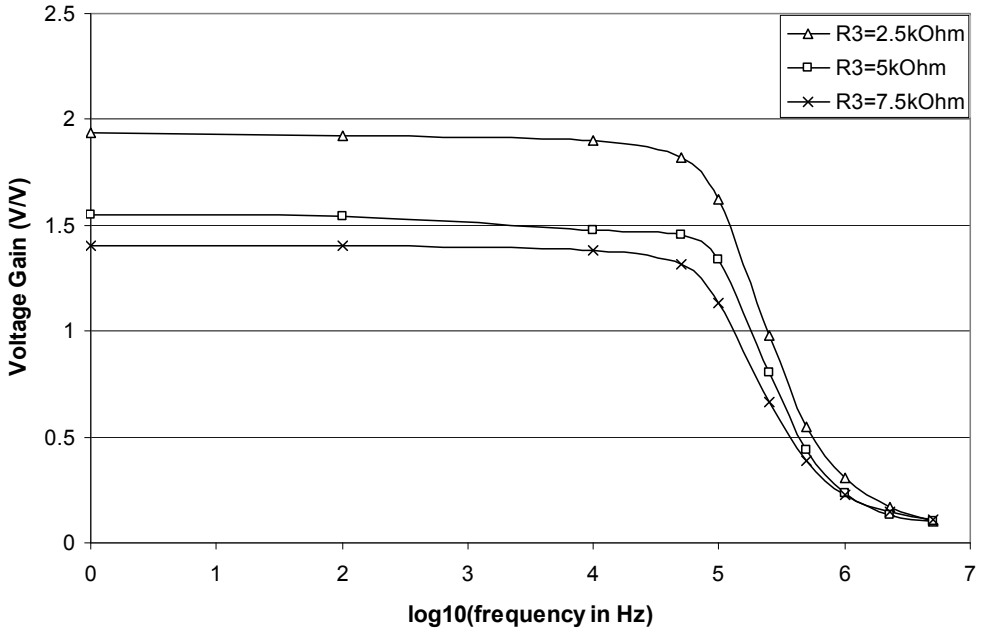

Figure 5.56 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three source resistor values

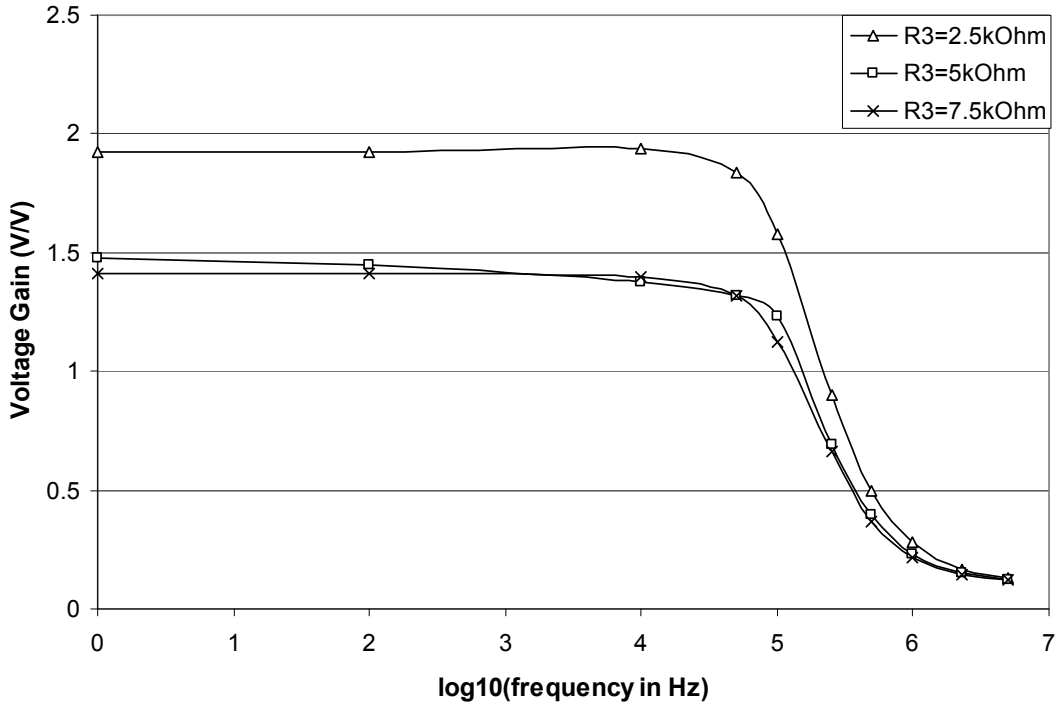

Figure 5.57 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three source resistor values

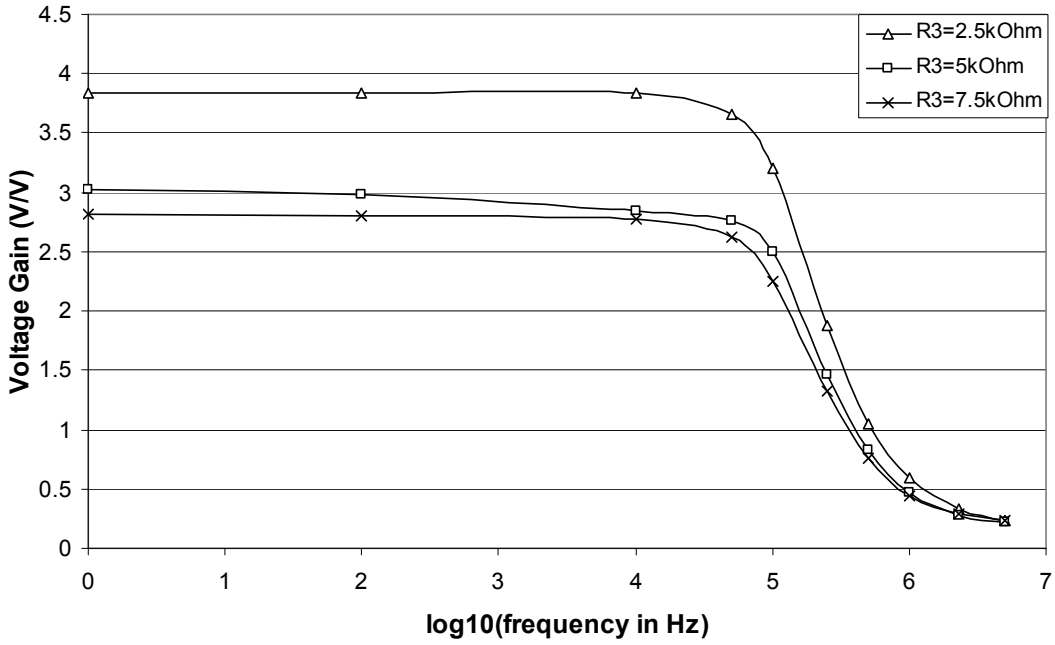

Figure 5.58 Plot of voltage gain of differential output vs. logarithm of frequency for three source resistor values

All the plots of the voltage gain vs. the logarithm of frequency show a relationship between the value of the resistance and the magnitude of the voltage gain that was not consistently present in all the voltage gain plots resulting from a dc V_{IN2}. The above plots show that the voltage gain increases with increasing source resistance. Moreover, the data lines up to 50kHz are nearly linear, and the higher-frequency data lines are exponential. This observation is further illustrated in the plots of Figures 5.59 through 5.61, which show the trend lines describing the data lines of the voltage gain plots of v_{out1}, v_{out2}, and the differential output, respectively.

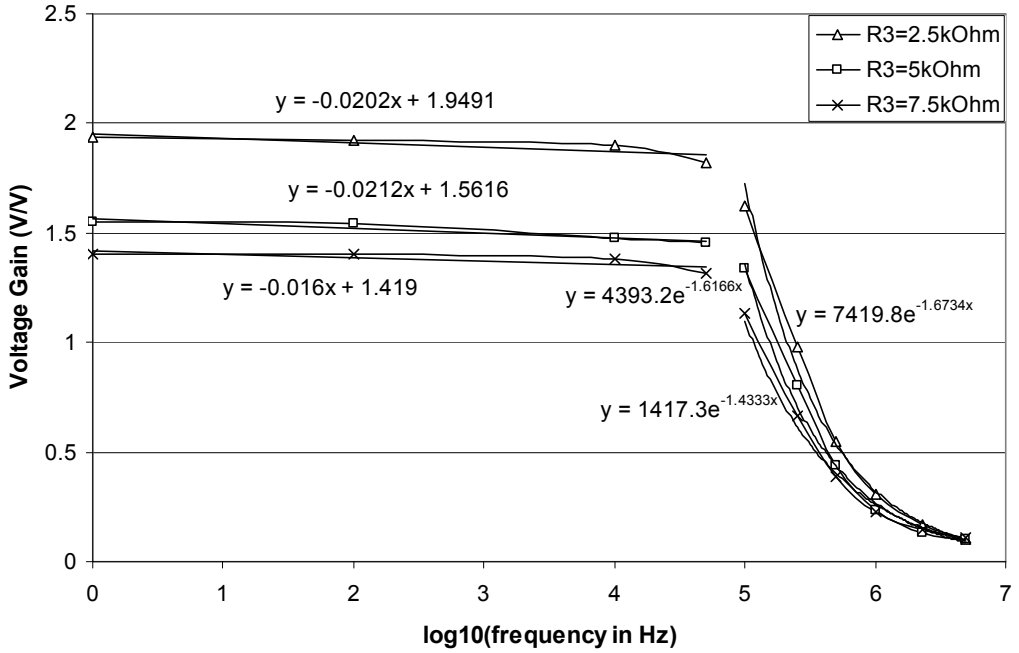

Figure 5.59 Plot of voltage gain of v_{out1} vs. logarithm of frequency for three source resistor values with trend lines

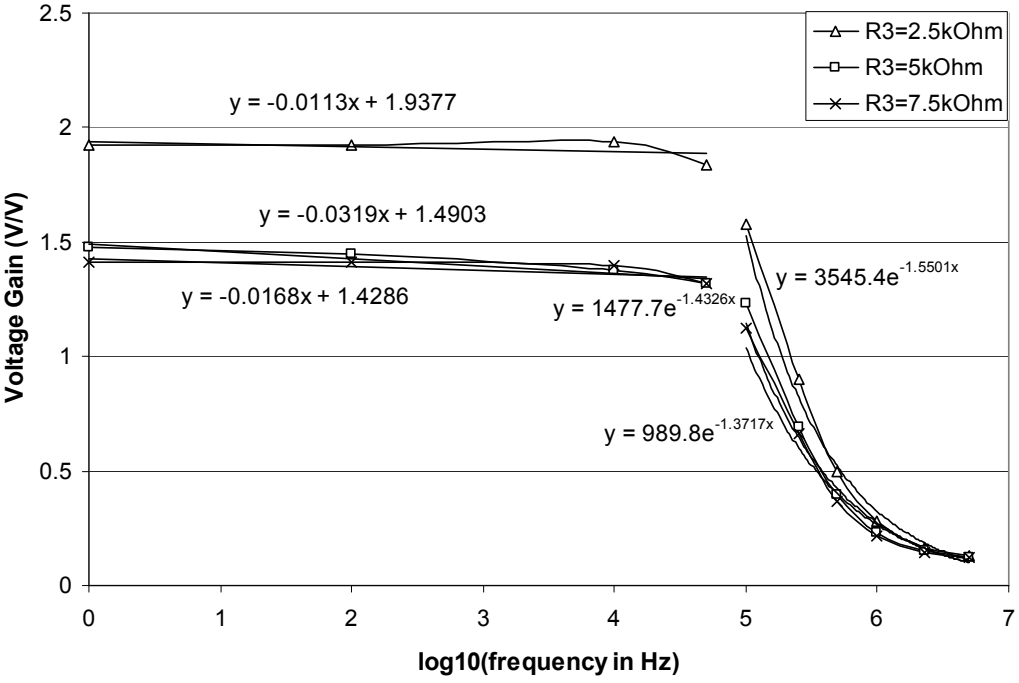

Figure 5.60 Plot of voltage gain of v_{out2} vs. logarithm of frequency for three source resistor values with trend lines

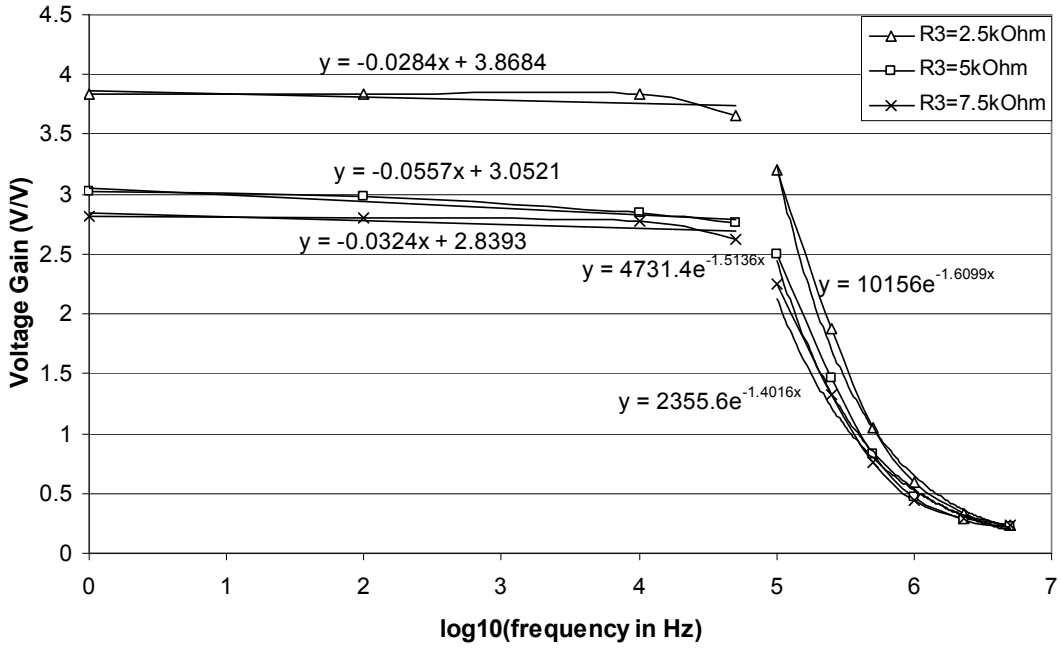

Figure 5.61 Plot of voltage gain of differential output vs. logarithm of frequency for three source resistor values with trend lines

The trend lines show that the low-frequency trend lines are linear with small negative slopes. The high-frequency trend lines are exponential and close together.

C. Comparison of the Voltage Gain and Phase Shift of the FeFET and MOSFET Differential Amplifiers

The voltage gain and phase shift of the FeFET differential amplifier were compared to the MOSFET differential amplifier built according to the configuration of Figure 5.1. It was observed that the shapes of the voltage gain vs. logarithm of frequency and the phase shift vs. logarithm of frequency plots of the FeFET differential amplifier were similar in shape to those of its MOSFET counterpart. When both input signals were sinusoidal, the voltage gain values achieved using the FeFETs were slightly lower than the values produced by the MOSFET amplifier. However, when the first input signal was sinusoidal while the other input signal was dc, the voltage gain values of the FeFET

differential amplifier were significantly lower than those of the MOSFET amplifier. Comparing the phase shift values of the two amplifiers, it was noted that for both input cases, both amplifier types displayed initial phase shift values of -180° for v_{out1} and the differential output and 0° for v_{out2}. At higher frequencies, the FeFET phase shift plots were always more consistent and stable than the MOSFET plots, but the values of the phase difference were higher in the FeFET differential amplifier. When both input signals were sinusoidal, the FeFET amplifier provided much smoother and more consistent plots than the MOSFET amplifier. In fact, there were no dips in the FeFET plots at higher frequencies as was seen in the MOSFET plots. When one input signal was sinusoidal and the other was dc, both the FeFET and MOSFET v_{out1} and differential output plots increased at higher frequencies, but the FeFET plots were more linear and consistent. For the v_{out2} phase shift plot, both the MOSFET and FeFET phase values increased and then decreased at the high frequencies, but the FeFET plots decreased at the highest frequency, while the MOSFET plots decreased at the second or third highest frequencies. Future work on the FeFET differential amplifier can compare the phase shift and voltage gain plots of more complex configurations of the FeFET and MOSFET differential amplifiers.

D. The Frequency Response

The frequency response of each of v_{out1}, v_{out2}, and the differential output of the FeFET differential amplifier were examined. Figures 5.62, 5.63, and 5.64 are plots of the voltage gain in decibels vs. the input frequency for each of v_{out1}, v_{out2}, and the differential output, respectively. All three plots have almost the same shape and follow nearly the same trends. Like the FeFET CS and CG amplifiers, the FeFET differential amplifier

displays decreasing low- through high-frequency responses. Again, the voltage gain begins to level off at the higher frequencies, but future examination of the very-high frequency response may show the frequency at which the voltage gain stops decreasing.

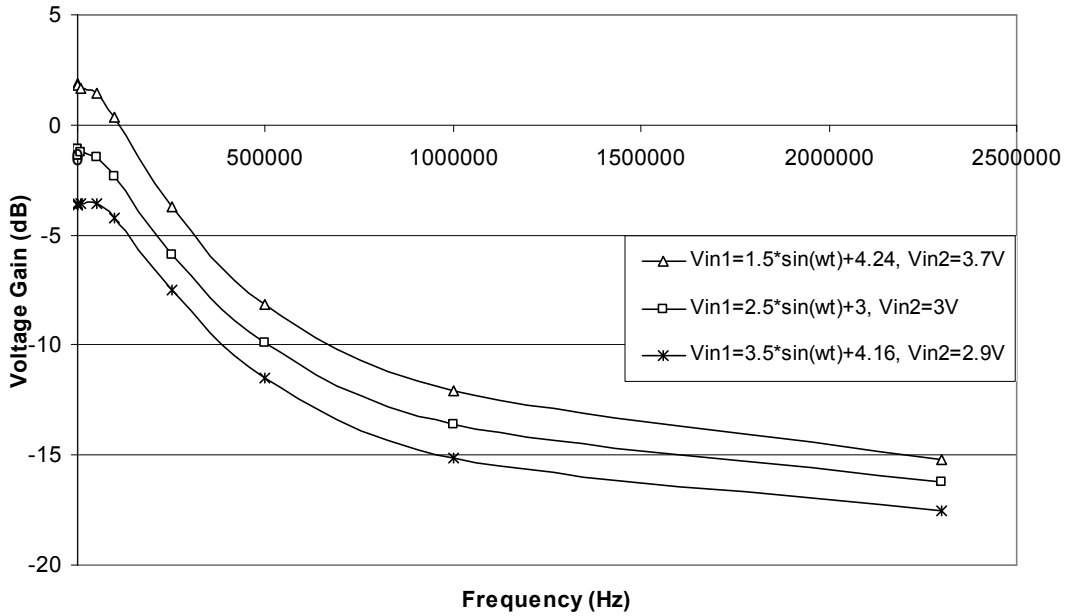

Figure 5.62 FeFET differential amplifier v_{out1} frequency response

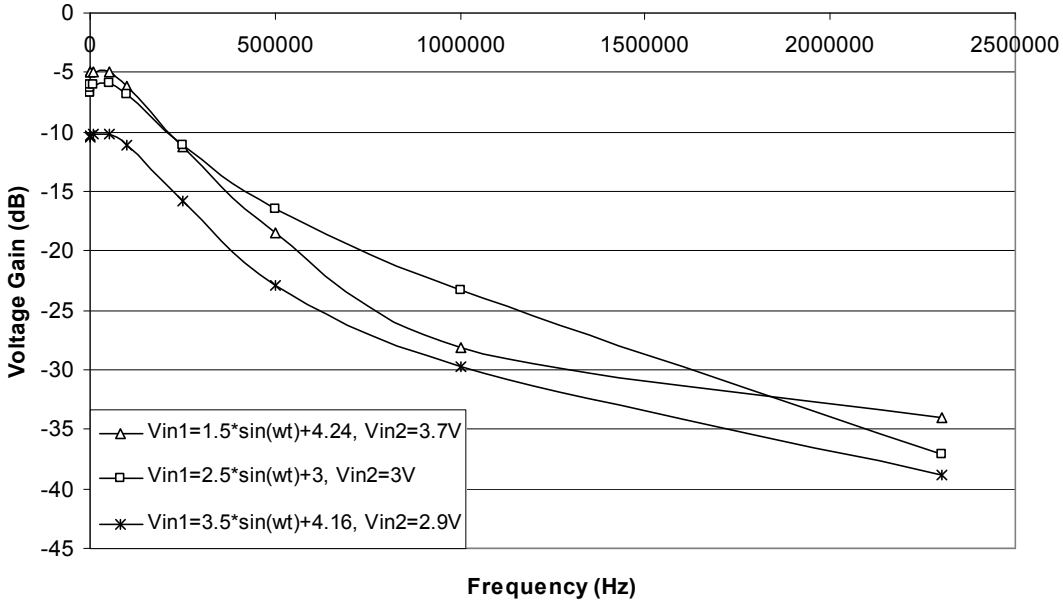

Figure 5.63 FeFET differential amplifier v_{out2} frequency response

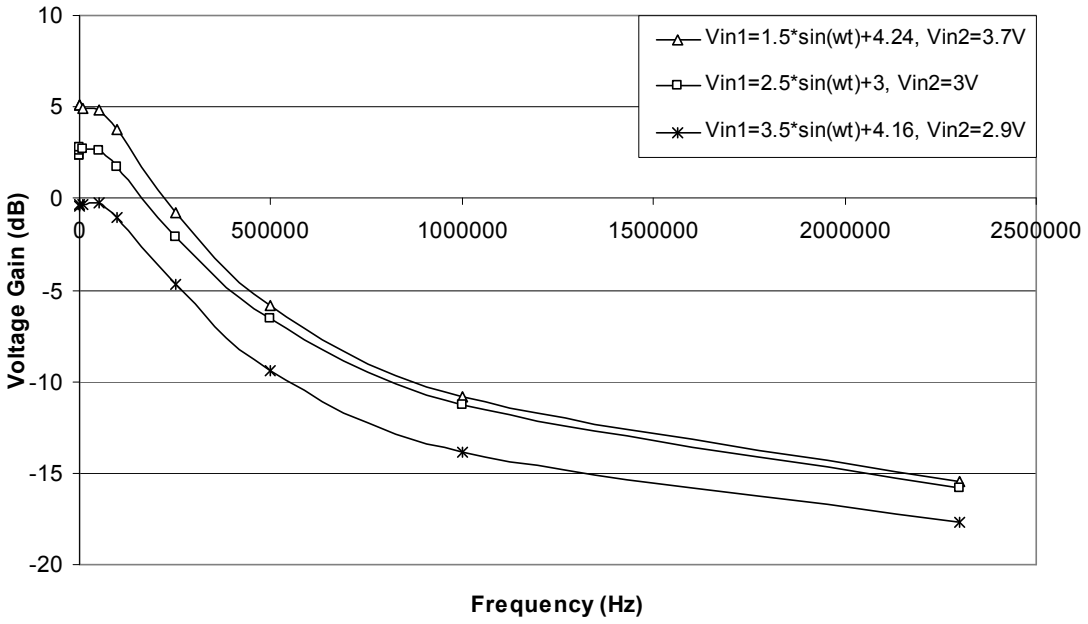

Figure 5.64 FeFET differential amplifier differential output frequency response

E. Conclusion of Experimental Results

The FeFET differential amplifier of the configuration shown in Figure 5.1 has been extensively studied. The logarithmic relationship that exists between the values of the output phase difference and each of the lower and higher frequency ranges for the three different outputs was observed. Also noted was the logarithmic relationship between the voltage gain and each of the lower and higher frequency ranges for the three output signals. Moreover, the effect of varying the load resistors and the source resistor were examined in two cases: when the first input signal was sinusoidal and the other was dc and when both input signals were sinusoidal. These basic relationships lay the groundwork for future study on the FeFET differential amplifier in this and many other configurations.

F. Nonquasi-Static FeFET Differential Amplifier Model

The behavior of the FeFET differential amplifier was modeled by the same NQS MATLAB® model that was used to describe the three previous amplifier types. Again, Equations (2.1) through (2.29) apply; however, two drain current and two output voltage equations were used for this amplifier. Specifically, I_{d1} is the drain current flowing through load resistor R_1 of the differential amplifier circuit shown in Figure 5.1, and I_{d2} is the current through R_2. Both current equations were derived in a similar manner as was done with the other amplifiers, and two scaling factors were used to provide more accurate results for the drain currents I_{d1} and I_{d2}. The equations for the two output voltages v_{out1} and v_{out2} are similar to the output voltage equation of the CG amplifier. Thus, the equations for V_{out1} and V_{out2} are as follows:

$$V_{out1} = V_{DD} - I_{d1} * R_1, \tag{5.1}$$

and

$$V_{out2} = V_{DD} - I_{d2} * R_2. \tag{5.2}$$

V_{out1} and V_{out2} were also multiplied by scaling factors to obtain more precise results.

a. Simulation Steps

The FeFET differential amplifier was simulated in MATLAB®, and the simulation steps are listed below. Figure 5.65 shows a flowchart of the detailed simulation steps.

1. Enter fabrication parameters (L, W, N_A, t_f, μ, etc.), simulation time interval, amplifier parameters (V_{DD}, input frequency, amplitude of input signal, load resistance, etc.), dc terminal voltages (V_D, V_G, V_S, and V_B), and number of channel partitions (N) for each FeFET.

2. Define the sinusoidal input signals v_{gs} and v_{gb} for each FeFET using the amplifier parameters entered and the current time step.
3. Rewrite the input signals using their phasor representations.
4. For each FeFET, calculate the surface potential at the source ($\psi_{s0}(t)$) and the surface potential at the drain ($\psi_{sL}(t)$) using Newton's method.
5. For each channel partition, calculate the surface potential at both edges of the partition using Newton's method for both FeFETs. Then, determine the surface potential across the partition by averaging the potentials at the edges and plugging this value into Equation (2.13) to obtain the most accurate surface potential value.
6. For each FeFET, propagate through a function for polarization and electric field calculations for each partition based on Equations (2.14)-(2.21).
7. Calculate the total ferroelectric charge per unit area, q'_F, for each FeFET by summing each partition's polarization and dividing by the number of partitions.
8. Determine each FeFET's threshold voltage using Equation (2.22).
9. For each FeFET, use the y-parameter model to calculate the drain currents, I_{d1} and I_{d2}, as described in Equations (2.23)-(2.29).
10. Multiply the drain currents by scaling factors.
11. Determine initial values for V_{out1} and V_{out2} using Equations (5.1) and (5.2).
12. Multiply V_{out1} and V_{out2} by scaling factors.
13. Update the values of I_{d1} and I_{d2} using Equation (2.23) with V_{ds} being replaced with the value for V_{out1} and V_{out2} for I_{d1} and I_{d2}, respectively.
14. Calculate an initial value for the source current, I_s, by summing I_{d1} and I_{d2}.

15. Determine an initial value for the source voltage, V_s, by multiplying I_s by the source resistance.
16. Update the values of I_{d1} and I_{d2} using Equation (2.23) with V_{ds} being replaced with the difference of V_{out1} and V_s for I_{d1} and the difference of V_{out2} and V_s for I_{d2}, V_{gs} replaced with the difference of the previous value of V_{gs} and V_s for both currents, and V_{bs} replaced with negative V_s for both currents.
17. Multiply each drain current by another scaling factor.
18. Recalculate V_{out1} and V_{out2} using the last values obtained for the drain currents.
19. Multiply each output voltage by another scaling factor.
20. Increment the simulation time by one time step.
21. If the incremented time is less than or equal to the final time step, go to Step 4. Otherwise, plot the output voltages with respect to ωt.

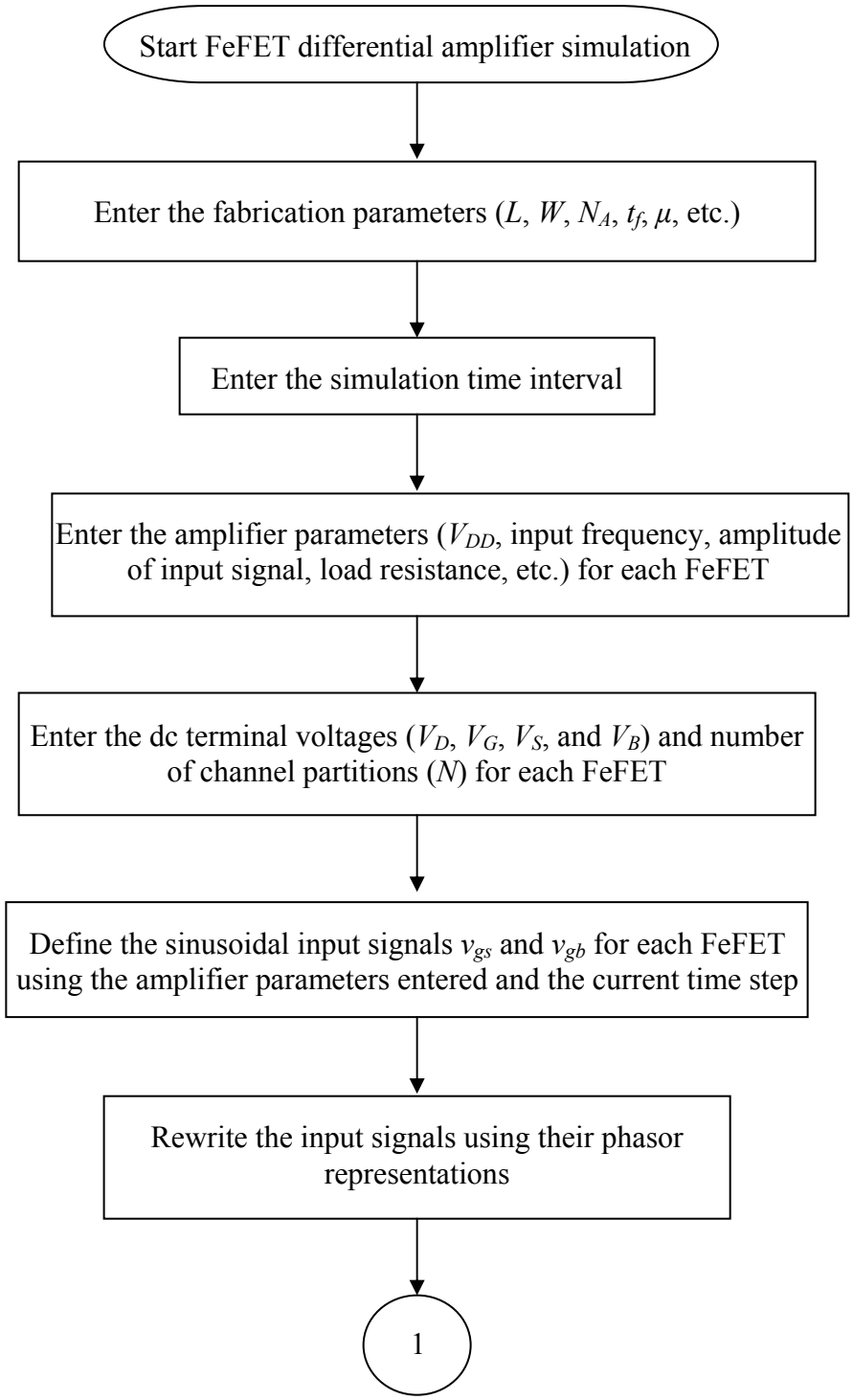

Figure 5.65 FeFET differential amplifier simulation steps

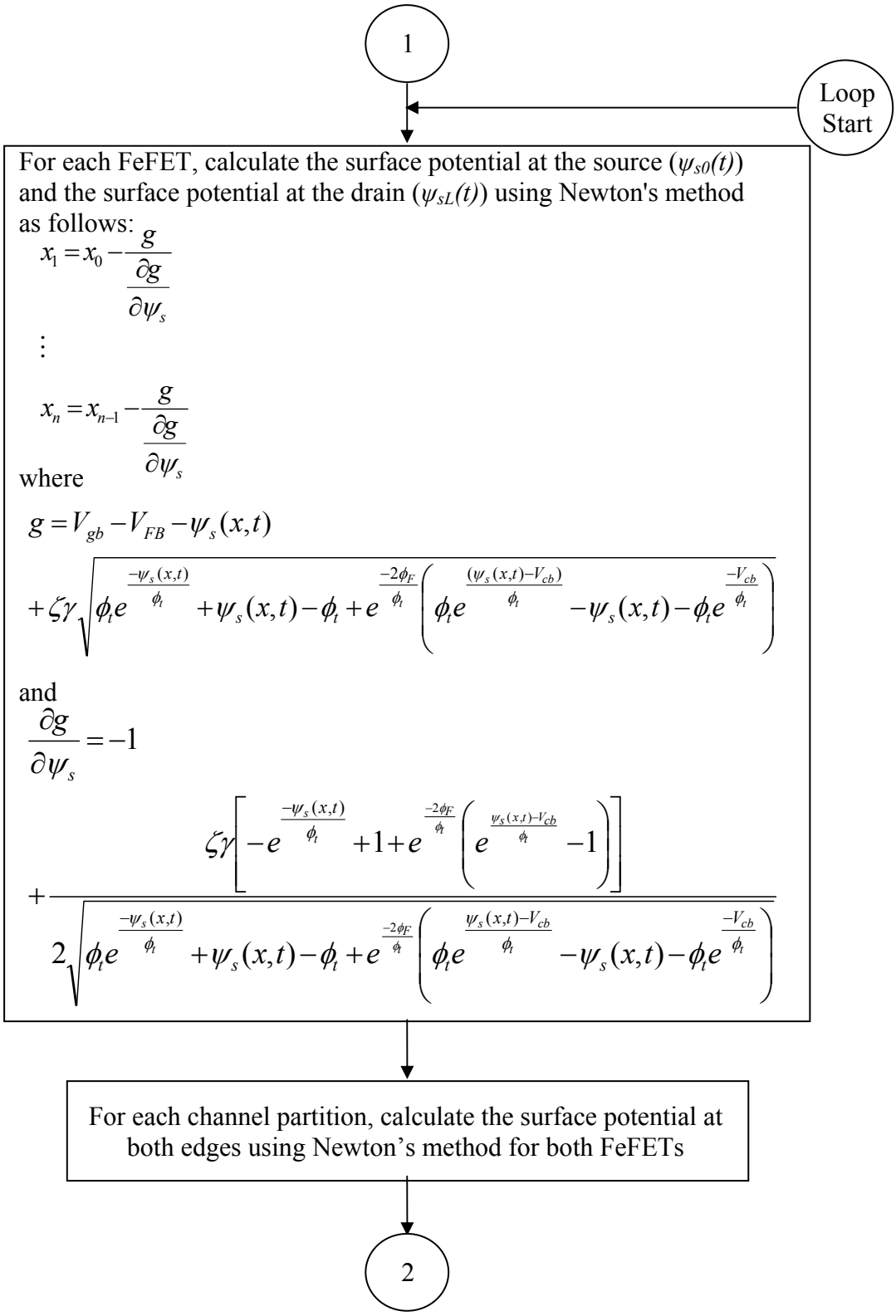

Figure 5.65 FeFET differential amplifier simulation steps (continued)

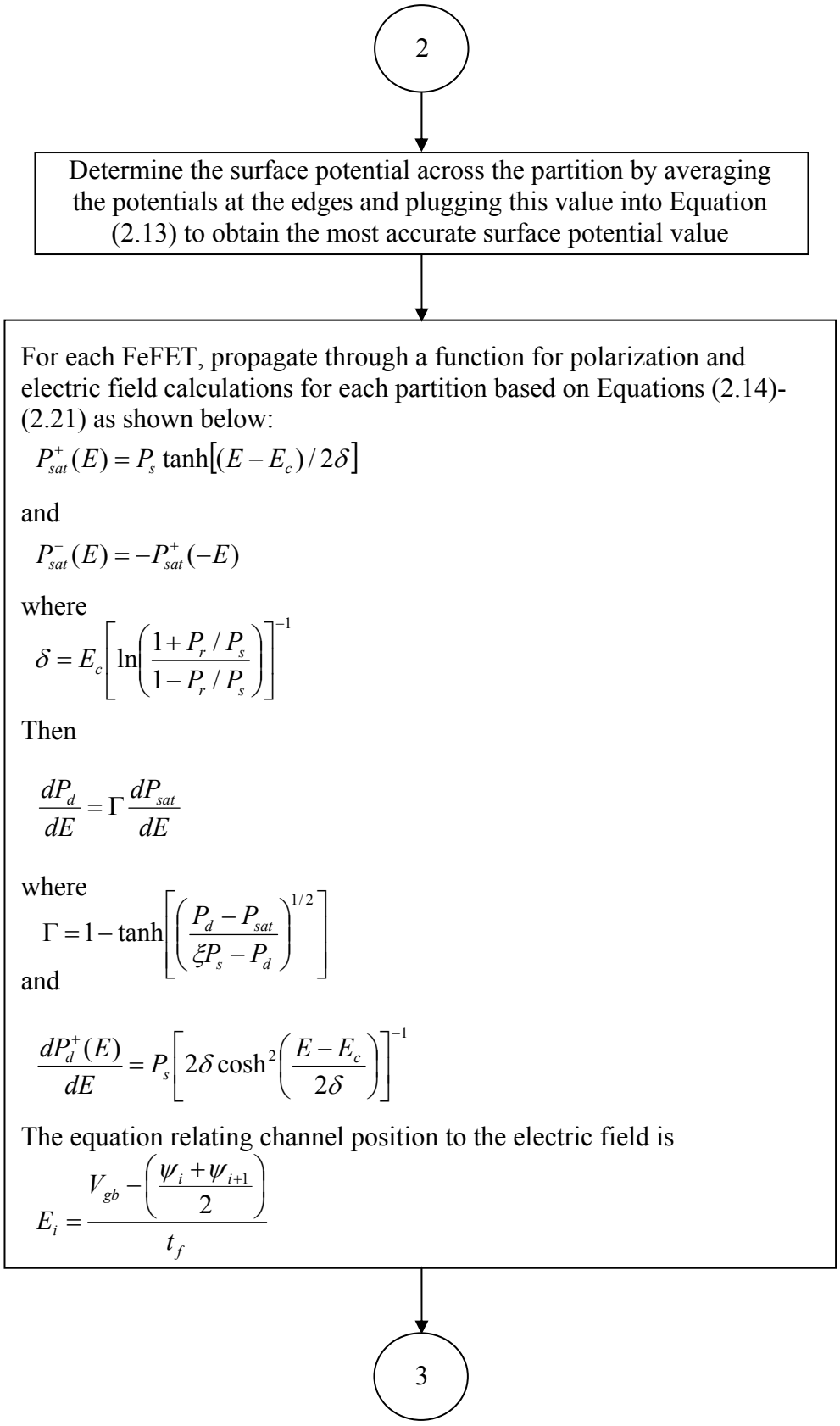

Figure 5.65 FeFET differential amplifier simulation steps (continued)

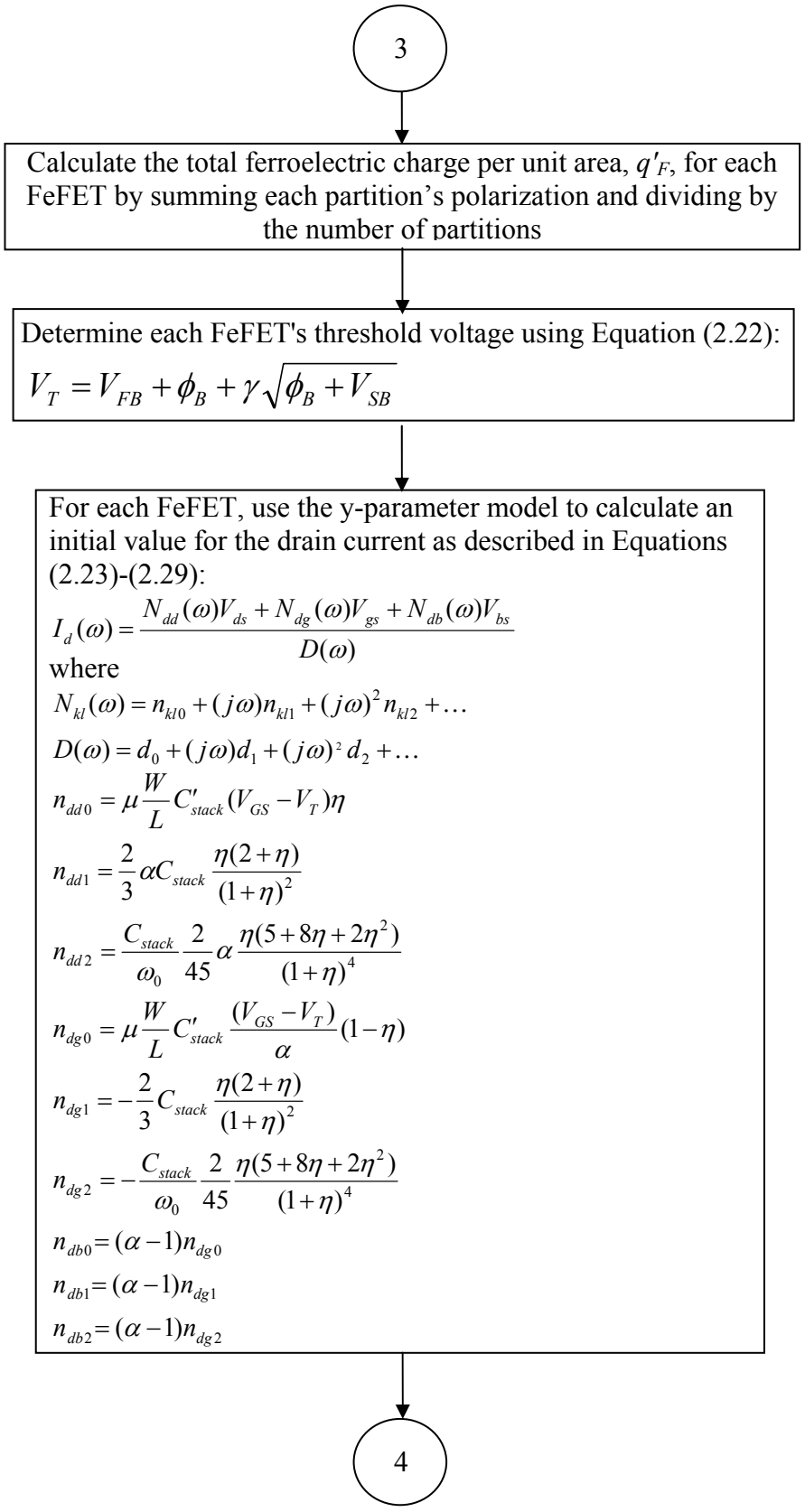

Figure 5.65 FeFET differential amplifier simulation steps (continued)

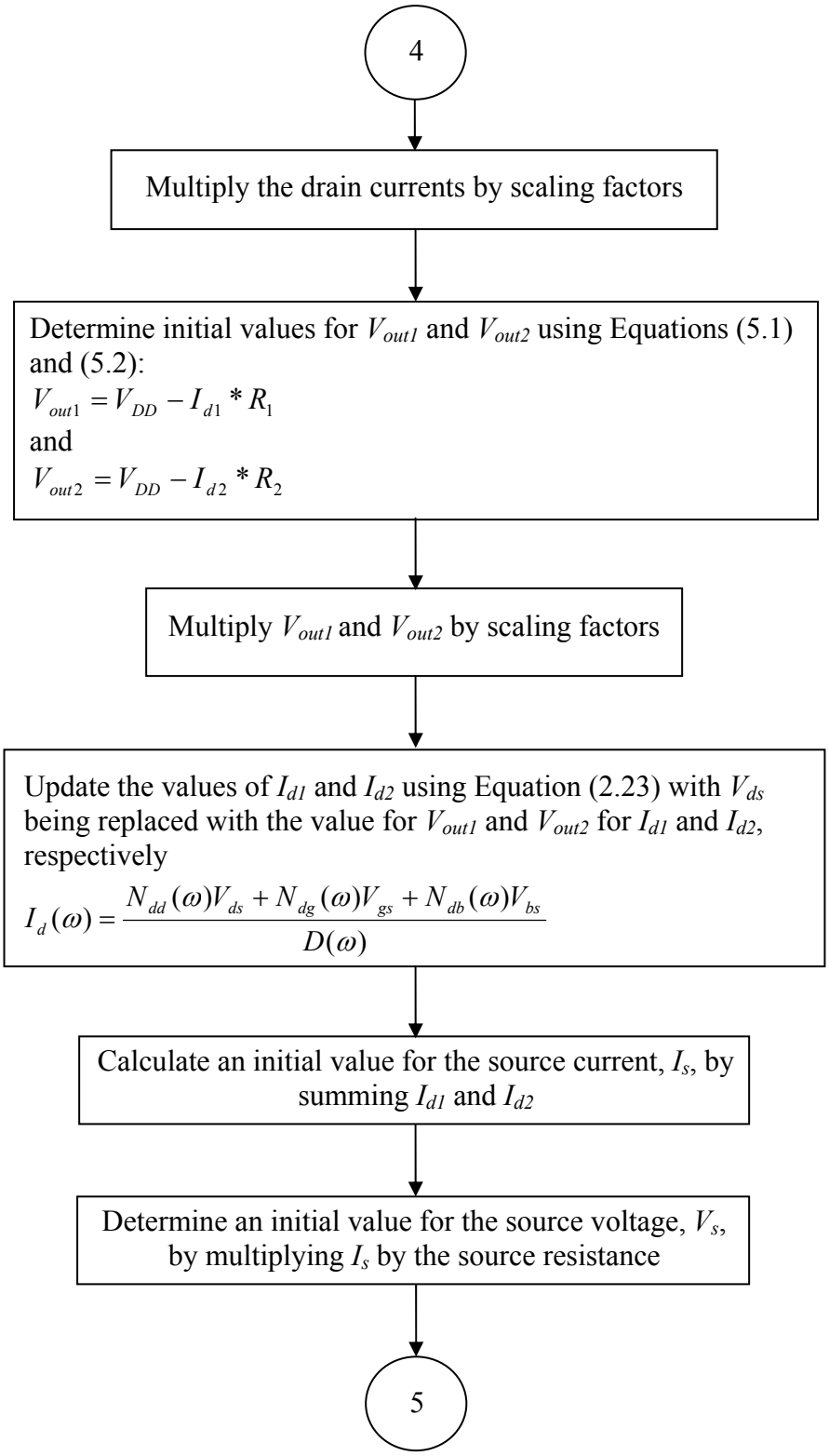

Figure 5.65 FeFET differential amplifier simulation steps (continued)

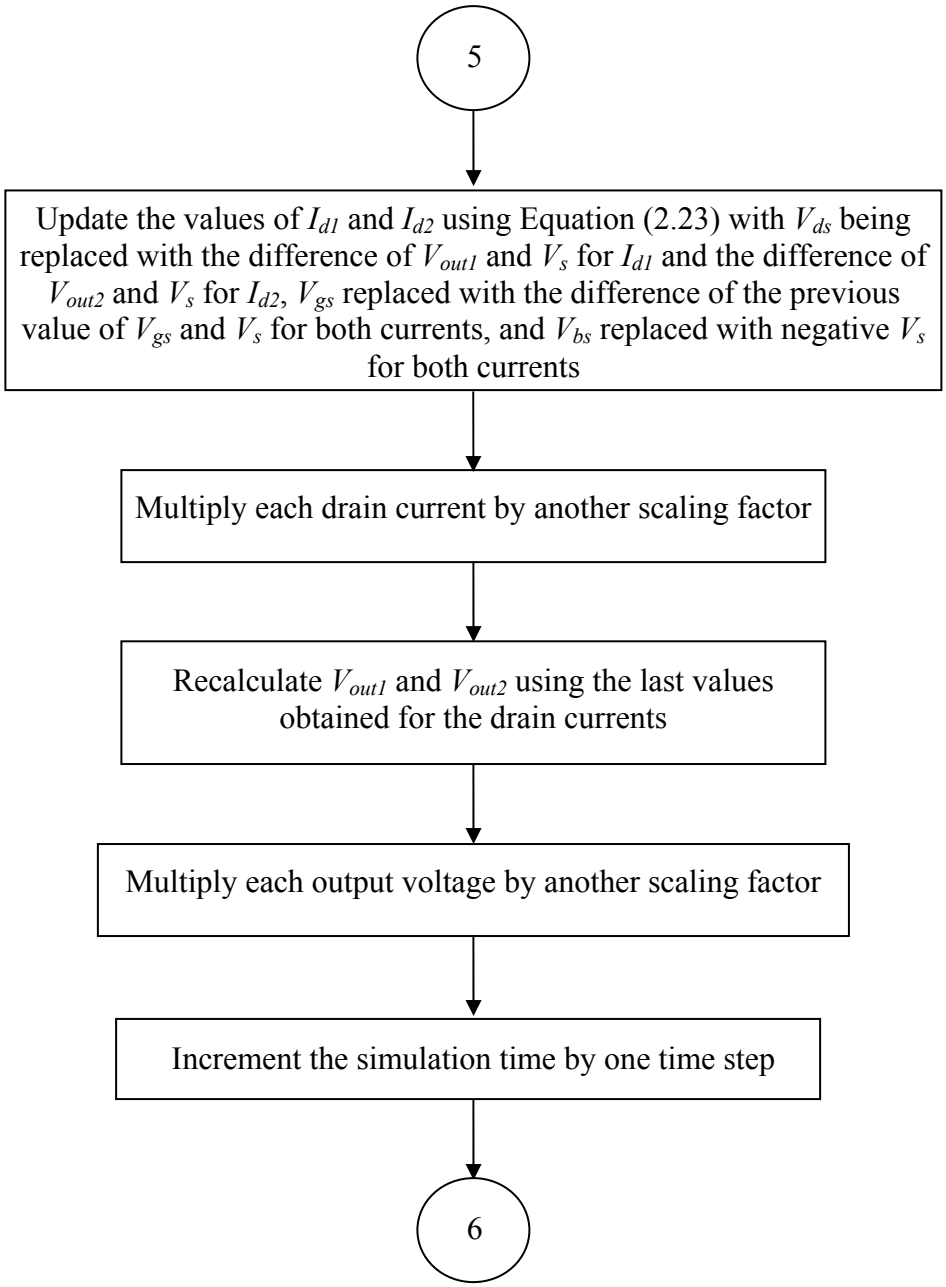

Figure 5.65 FeFET differential amplifier simulation steps (continued)

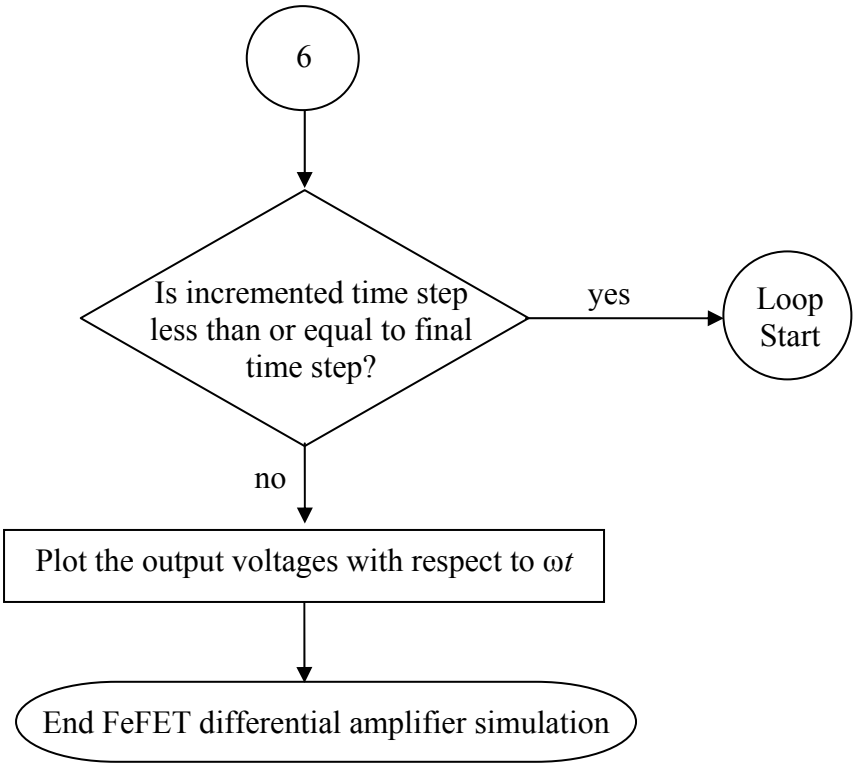

Figure 5.65 FeFET differential amplifier simulation steps (continued)

b. Model Results

Two test cases based on the circuit configuration of Figure 5.1 were carried out to confirm the model's accuracy and efficiency. For the first test case, V_{DD} was 8V, the amplitude of the sinusoidal input signal was 2.5V, the dc input signal was 3V, the offset voltage was 3V, the input frequency was set to 1MHz, the load resistors R_1 and R_2 were each 10kΩ, and the source resistor R_3 was 5kΩ. The currents' scaling factors were $1.38\text{x}10^{-8}$ for I_{d1} and $3.65\text{x}10^{-9}$ for I_{d2}. V_{out1} was multiplied by 0.4706 and V_{out2} was multiplied by 0.6151. Moreover, a positive polarization voltage $V_{p,pos}$ of 6V was added to the gate of each FeFET. Figures 5.66 and 5.67 show the oscilloscope and modeled output

plots, respectively. In both plots, the only input signal shown is the sinusoidal input signal (given by V_{in}).

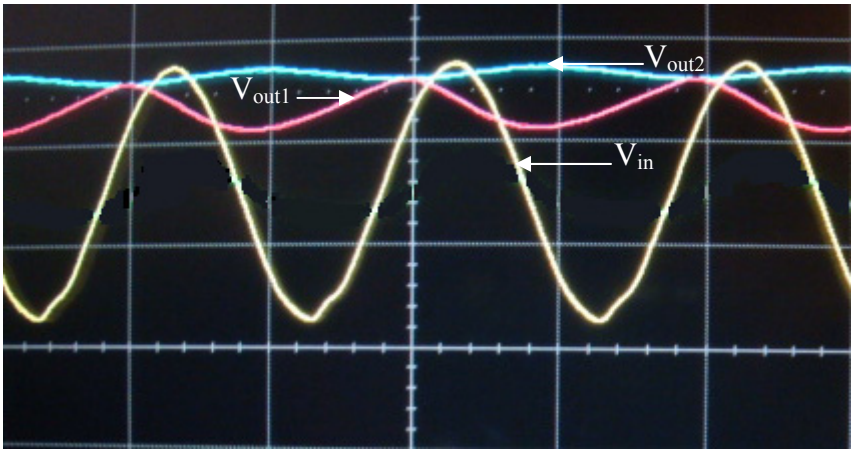

Figure 5.66 Oscilloscope output for the first test case with a scale of 2V per division for V_{in}, V_{out1}, and V_{out2}

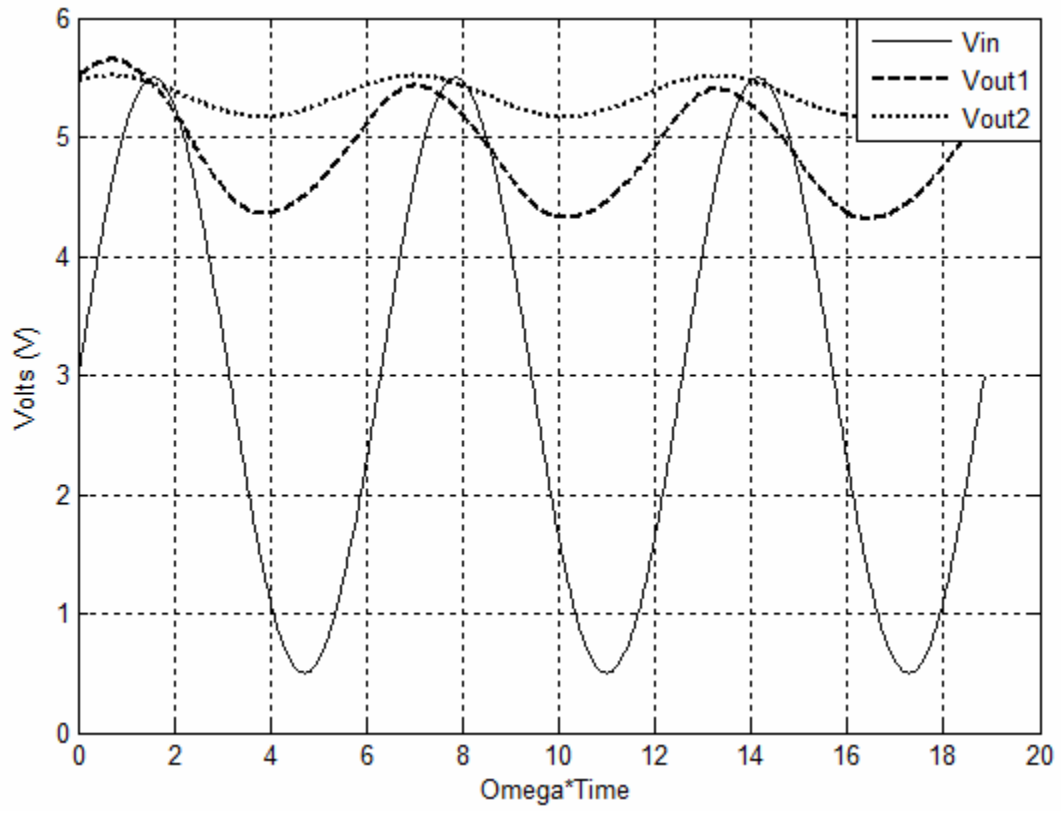

Figure 5.67 Modeled output for the first test case

Comparing the oscilloscope and modeled output plots shows that the model produces output voltage signals that are very similar in shape and values to those produced by the oscilloscope. However, one difference between the modeled and oscilloscope plots is that the phase shifts of V_{out1} and V_{out2} were the same in the plot produced by the model. This was the case since V_{in1} is a sinusoidal signal whereas V_{in2} is dc, so only V_{in1} has a phase shift parameter. In both of the test cases examined for the differential amplifier, V_{out1} and V_{out2} displayed an inherent phase shift of 85°. V_{out1}'s phase shift was easily adjusted by changing the value of V_{in1}'s phase shift parameter. However, V_{out2}'s phase shift could not be properly adjusted since that signal had no phase shift parameter. Tables 5.1 and 5.2 compare the maximum and minimum values of the oscilloscope and simulated signals for V_{out1} and V_{out2}.

For the second test case, V_{DD} was set to 4V, the sinusoidal input signal's amplitude was 0.5V, the dc input signal was 1.4V, a positive offset voltage of 2.75V was included, the frequency was 1MHz, and the load and source resistances remained unchanged from the previous test case. The drain currents' scaling factors were 3.162×10^{-8} and 1.350×10^{-8} for I_{d1} and I_{d2}, respectively. The output voltages' scaling factors were 0.4713 for V_{out1} and 0.6144 for V_{out2}. A positive polarization voltage $V_{p,pos}$ of 6V was also added to the gates of the FeFETs of this differential amplifier. Figure 5.68 is the oscilloscope plot and Figure 5.69 is the modeled plot.

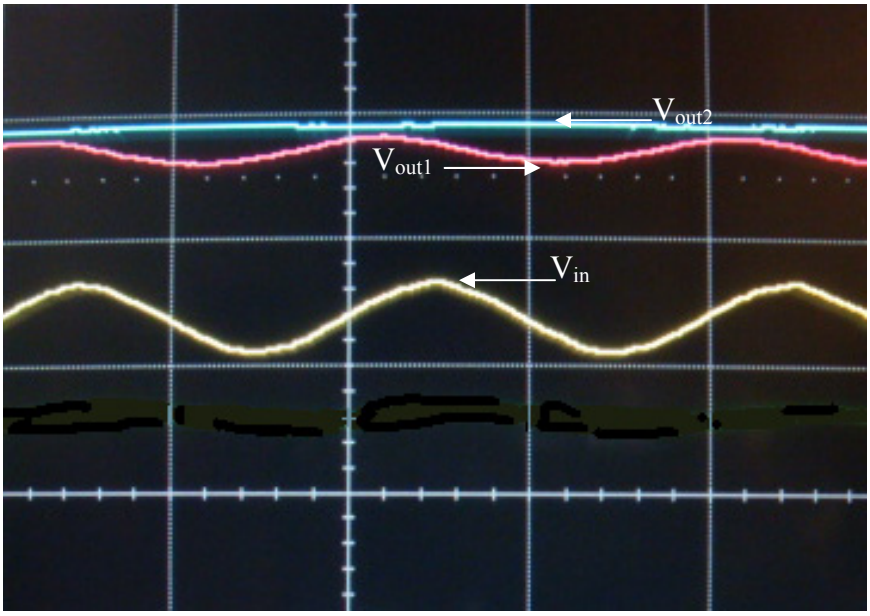

Figure 5.68 Oscilloscope output for the second test case with a scale of 2V per division for V_{in} and 1V per division for V_{out1} and V_{out2}

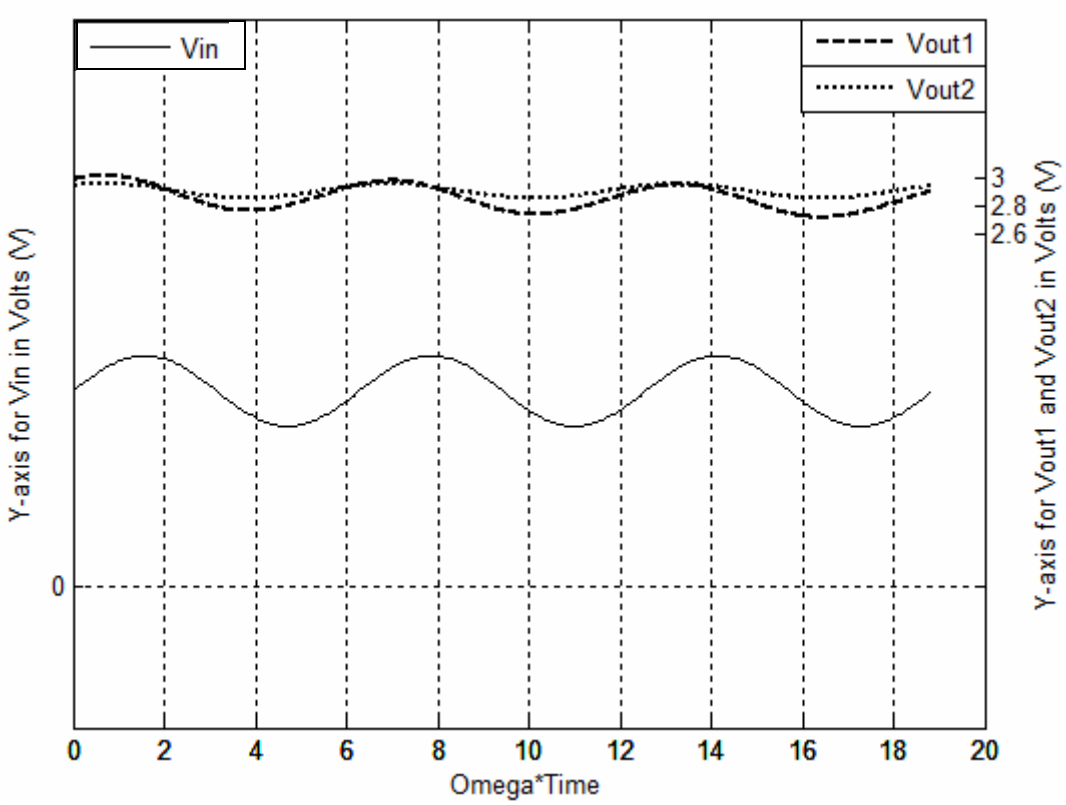

Figure 5.69 Modeled output for the second test case

As with the previous test case, the modeled plot is very similar in shape and values to the oscilloscope plot. The model clearly produces accurate results. As with the previous test case, V_{out2}'s phase shift could not be properly adjusted since that signal had no phase shift parameter.

Table 5.1 Oscilloscope and simulation results for V_{out1} of FeFET differential amplifier

	Test Case I—V_{out1}		Test Case I—V_{out2}	
	Max. value	Min. value	Max. value	Min. value
Oscilloscope Results	5.35	4.31	5.51	5.17
Simulation Results	5.402	4.315	5.513	5.165

Table 5.2 Oscilloscope and simulation results for V_{out2} of FeFET differential amplifier

	Test Case II—V_{out1}		Test Case II—V_{out2}	
	Max. value	Min. value	Max. value	Min. value
Oscilloscope Results	2.814	2.605	2.923	2.85
Simulation Results	2.839	2.609	2.957	2.851

G. Conclusion of Modeled Data Analysis

The model's ability to accurately describe the FeFET differential amplifier of the configuration shown in Figure 5.1 proves its versatility and adaptability in more complex analog circuits. The model has been shown to accurately describe the behavior of multiple output signals based on multiple input signals. It can be clearly seen that this model can be easily altered to describe the behavior of other differential amplifier configurations and countless other FeFET-based circuits.

CHAPTER VI

CONCLUSION

This dissertation introduced, characterized, and modeled several FeFET analog circuit configurations. The dissertation began with a brief introduction of the properties, theory of operation, and characterization of the FeFET based on the work done by the author in [18]. The FeFET's I-V characteristics were accurately modeled and the hysteresis effect was reproduced.

Then, the FeFET-based CD, CS, CG, and differential amplifiers were studied. The characteristics of the FeFET CD amplifier were adapted from the author's thesis [18]. Specifically, empirical measurements were carried out to determine the effect of input frequency and load resistance on each of the phase shift of the output signal, the output voltage, and the voltage gain. It was found that a logarithmic relationship existed between the input frequency and each of these three output parameters. The same holds true for the load resistance and the output parameters examined. Next, a physically-derived NQS model was created in MATLAB® to simulate the behavior of this amplifier. The model was based on the method of partitioned ferroelectric layer [2] and incorporated the differential equations describing the ferroelectric polarization as a function of an applied electric field [37, 38]. The model's accuracy in reproducing the

shape and magnitude of the oscilloscope signals was verified by comparing the modeled output signals with empirical results. The model was found to be accurate, efficient, and easy to use since it incorporates the standard MOSFET equations and the NQS y-parameter representation of drain current [3] that have been modified to include the effect of the ferroelectric layer.

The FeFET CS amplifier was next examined. As with the FeFET CD amplifier, the effect of frequency and load resistance on the phase shift of the output signal, the output voltage, and the voltage gain were studied. Examined independently at the low and high frequencies, there was a logarithmic relationship between frequency and each of the three output parameters. The phase shift of the output signal was logarithmically related to the load resistance, and the shape of the output voltage and voltage gain plots vs. load resistance were unique. Next, the relationships between the dc input voltage, output voltage, drain current, and load resistance were observed. It was noted that the plot of the output voltage vs. the dc input voltage had a similar hysteretic shape as that of the FeFET remnant polarization plot, whereas the hysteretic shape of the plot of the drain current vs. dc input voltage was similar to that of the active polarization plot. The drain current and the output voltage were linearly related. Moreover, the power dissipated by the FeFET in the CS amplifier configuration was noted. Then, the NQS model that was used to describe the behavior of the FeFET CD amplifier was altered to reflect the behavior of the CS amplifier circuit. Again, the model was found to be both accurate and efficient in simulating this FeFET circuit.

The next circuit configuration studied was the FeFET CG amplifier. The effect of varying the input frequency on the phase shift of the output signal, the output voltage,

and the voltage gain was first examined. There was a logarithmic relationship between the frequency and each of these output parameters at each of the lower and higher frequency ranges. The effect of the load resistance on the aforementioned output parameters was also noted. Furthermore, the effect of applying positive and negative polarization voltages at the gate of the FeFET CG amplifier was examined. It was observed that applying a negative polarization voltage greatly enhances the voltage gain of the amplifier. Lastly, the physically-derived NQS model was altered to apply to the FeFET CG amplifier configuration. As was the case with the previous circuits, the output plots of the model were very similar to those of the oscilloscope.

The last circuit configuration presented was the FeFET differential amplifier. Several relationships were empirically measured. First, the effect of frequency on the individual and differential phase shifts and voltage gains was studied. It was found that v_{out1} and the differential output signals were logarithmically related to frequency when the low and high frequency ranges were examined independently. The same holds true for v_{out2} when the last data point was ignored. The voltage gain of each of the three output signals was also logarithmically related to each of the low and high frequency ranges. The effect of varying the load resistors and the source resistor on the phase shift and voltage gain of the output signals was next observed for two cases: when the first input signal was sinusoidal and the second was dc and when both input signals were sinusoidal. For the first input case, no specific trend between the magnitude of the phase shift of the three output signals and the value of the load resistors was noted. For v_{out1}, the voltage gain increased with increasing load resistances. No direct correlation was noted between the magnitude of the phase shift of the output signals and the value of the

source resistance for the first input case. The voltage gain of v_{out1} and differential output signal increased with decreasing source resistance. For the second input case, no direct relationship was observed between the magnitude of the phase shift and the value of the load resistors. However, the voltage gain increased with increasing load resistance. As with varying the load resistances, no correlation was seen between the phase shift and the value of the source resistor. The voltage gain increased with increasing source resistance. Finally, the model presented in this dissertation was adapted to simulate the behavior of the FeFET differential amplifier. As with all the previous amplifiers studied, the model was able to effectively and accurately reproduce the empirically-derived output signals.

This dissertation presented several new and previously unexplored concepts in the field of ferroelectric circuit design. It investigated the basic characteristics of the FeFET CD, CS, CG, and differential amplifier configurations. Moreover, a physically-derived NQS model that is valid in accumulation, depletion, and the three inversion regions was created to simulate the behavior of these FeFET amplifiers. While researching all these circuits, many points of further study were noted. For example, the frequency response of all these FeFET amplifiers can be more closely examined, especially at higher frequencies. Also, the impact of the linearity describing many of the relationships between the logarithm of frequency and the output parameters of phase shift, output voltage, and voltage gain can be further explored. Another interesting point for further study is the effect of polarization on the amplifiers' behavior. This work examined the basic configurations of the aforementioned four FeFET amplifier types, so with a good understanding of their behavior, more complex versions of these amplifiers can now be effectively studied. Furthermore, with a user-friendly and effective computer model that

accurately describes the behavior of these FeFET amplifiers, the possibility of modeling and creating innumerable FeFET circuits is now much more feasible.

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