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High quality factor microwave resonators using embedded structures in PCB

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HIGH QUALITY FACTOR MICROWAVE RESONATORS USING EMBEDDED STRUCTURES IN PCB

by

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A DISSERTATION

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for the degree of Doctor of Philosophy
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Submitted by Reza Kamali Sarvestani in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering and accepted on behalf of the Faculty of the School of Graduate Studies by the dissertation committee.

We, the undersigned members of the Graduate Faculty of The University of Alabama in Huntsville, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering.

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ABSTRACT

The School of Graduate Studies
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Name of Candidate Reza Kamali Sarvestani
Title High Quality Factor Microwave Resonators Using Embedded Structures in PCB

The market is always expecting miniaturization and cost reduction to provide continuous improvement for customer satisfaction. In the field of wireless communications, the digital components have been improved continually, but it is suffering from the low quality factor passive devices. Passive components such as inductors, capacitors, and resistors are constantly being redesigned to enable higher performance and smaller size. Inductors and resonators are among the chief components currently being studied to achieve higher quality factors and size improvements. It is essential to make high quality inductors and resonators with accurate values and cost effective methods for modern microwave applications.

Methods utilizing printed circuit boards (PCB) provide an effective solution for the fabrication of passive radio frequency components. A key technology in the PCB fabrication is the embedding of Thru-hole via. The new approach in this study is to use minimum feature size of standard PCB production to make embedded solenoids in a Duroid substrate with 2.2 relative permittivity. Each solenoid turn included two embedded copper vias of 125 μm radius and two surface conductors of 250 μm wide. Different pitch sizes, conductor lengths, solenoid heights, and number of turns were

simulated and produced. The highest quality factor of 160.3 was received for a 500 μm pitch size and 1 mm conductor length in a substrate of 380 μm thicknesses.

This work shows the optimization of high Q resonators using the new solenoid inductor required a one turn solenoid. Furthermore, it introduces a series capacitance within the via to move the poles of characteristic function of the equivalent circuit toward higher frequencies. This provides significant enhancement in the quality factor which is realized using pole transfer. The result increased the resonance frequency to 12.25 GHz with a Q-factor of 306. Both the inductor and capacitive coupled resonator can be batch fabricated using conventional circuit board techniques. Analytical designs for the inductor and resonator were investigated using both a lumped circuit model and electromagnetic (EM) simulation. S-parameter measurements were in close agreement with simulations. The micro-solenoids and tuned resonator had a higher quality factor compared to the other counterparts.

Abstract Approval:

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CHAPTER 1

INTRODUCTION

The rapid growth of wireless communications and frequency applications necessitates efficient usage of frequency spectrum as a limited source of energy [1]. Also, the increasing number of frequency users results in higher network interference and requires new filtering techniques for bandwidth employment [2]. For example, the Mobile-Fi, Zig-bee, and UWB systems will occupy a large frequency bandwidth and need high quality filters to avoid any inter-modulation and interference in their front end radios. Other examples are the devices that in higher frequency ranges such as the application of 5.8 GHz for Bluetooth, WLAN, and Cordless Phones. These communication systems provide many adjacent channels and require interference protection circuits. At the same time, there is a high demand for miniaturization and light weight components [3]. It is to meet the market expectation for providing a continuous improvement and customer satisfaction. To fulfill this requirement, the communication industry needs new passive devices such as inductors with smaller size and lower weight.

Passive components are mainly used in the front ends of the radios and include inductors and capacitors. In fact, good passive components result in better wireless

devices such as resonators, filters, baluns, oscillators, and matching network circuits [4], [3]. It is essential to apply inductors and resonators for making any of the previously mentioned circuits. Due to such a large application for the inductors and resonators, some research has been done to improve the performance of the inductors and resonators.

One of the main parameters to evaluate the performance of an inductor is the quality factor [5], [6]. The quality factor of a resonator can be defined using the ratio of the resonance frequency to half power bandwidth, as given in equation (1.1) [6]. However, inductors operate near but not at the resonant frequency. Therefore, the Q-factor of the inductors is frequently referred to in the literature as the ratio of the energy stored in the inductor to the energy dissipated in the device for the same cycle as given in equation (1.2) [7]-[11].

$$Q_{resonator} = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{1.1}$$

$$Q_{Inductor} \equiv \frac{Energy\_stored\_in\_the\_inductor\_in\_one\_cycle}{Energy\_loss\_in\_the\_inductor\_in\_one\_cycle} \tag{1.2}$$

The higher the quality factor, the better the selectivity of the frequency channel. As a result of better selectivity, lower power signals can be received without any interference damage. Also, a higher quality factor would result in lower insertion loss in the filters. Lower insertion loss improves the transmission features of the filter and accommodates the weaker signals. An example for the application of these filters is

given in the Figure 1.1; this figure illustrates the block diagram for the front end of a high frequency radio.

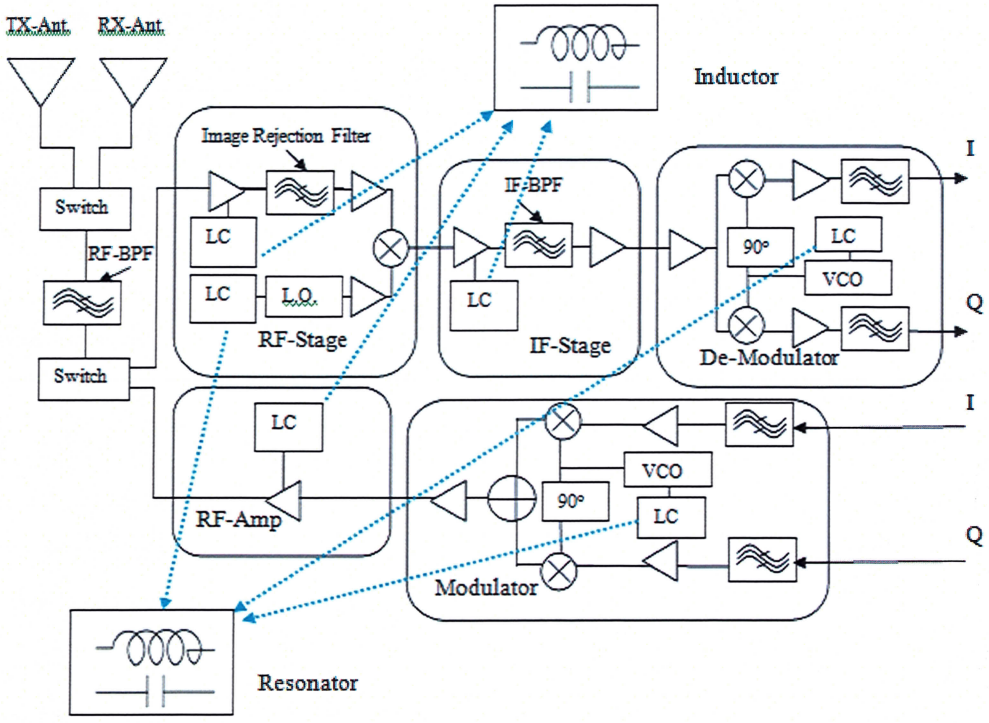

Figure 1.1 Block diagram of the front end for a wireless communication radio showing the application of resonators and inductors [12].

Two different filters are used in this diagram. A band pass filter is used as RF-filter and it includes inductors for tuning and filtering features. Also an image filter is used, and it is a stop band filter consisting of inductors or resonators for blocking the image frequencies. RF resonators and inductors are fundamental parts of the filters and oscillators [3]. A Higher quality factor in the oscillator will result in better phase noise

and improves the performance. Two different methodologies are reported to make high quality factor RF-inductors and resonators [13]. The first approach is the On-chip fabrication of the components. The other method is using a supporting substrate to make the high quality factor passive for silicon chip technology.

Silicon was traditionally used for the fabrication of the inductors to make the On-chip inductors integrate to the other components and to take the benefit of silicon wafer fabrication techniques [14], [15]. However silicon has higher conductivity compared to common microwave substrates such as Alumina, RT/Duroid, and Low Temperature Co-fired Ceramics (LTCC) [13]. Having this conductivity, the silicon wafer is not a good candidate for microwave substrate. The main reasons for low resolution for RF-inductors fabricated on silicon wafer are the eddy current loss and parasitic capacitance [16], [17]. The magnetic field induced in the silicon substrate would result in eddy current, and this current loss degrades the quality factor of the silicon. On the other hand, the silicon layer will work like a poor ground for the Micro-inductor. Such a ground layer close to the coil will cause parasitic capacitances. Although these capacitances were extensively studied and different methods were developed to overcome their effect, they are still a major source for lowering the Q-factor of the Micro-inductors [15]. The quality factor of the passive components can be limited to the low resolution of the On-chip passives. Table 1.1 shows the road map that needs Q improvement for wireless communication in the next 5 years [18]. One should immediately recognize that the inductor based Q values have to improve within this period.

The insulator substrates can overcome the silicon conductivity effects. Substrates such as glass, low temperature co-fired ceramic (LTCC), benzocyclobutene (BCB), and

organic materials have been used for the fabrication of Micro-inductors. Improvement in the quality factor was reported due to the decrease the parasitic capacitances. But most of these materials are not commercially used as the microwave substrate and the processing method defined for the fabrication of the inductor on them is complicated and costly.

Table 1.1 Wireless communication requirements for inductors in the next 5 years [18].

	Year of Production	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**
Inductor on Organic Substrate	**Max Q**	>40	>40	>40	>40	>40	>45
	Self Resonance	>10	>10	>10	>10	>10	>10
Inductor on Inorganic Substrate	**Q (5 GHz, 1 nH)**	40	50	50	50	50	60
On-Chip Inductor	**Q (5 GHz, 1 nH)**	30	35	40	42	44	46

To become familiar with the previous work related to the micro-inductors, and also demonstrate their advantages and disadvantages, a review of the major previous methods is given in the next session. After that the organization of this dissertation is explained. In this dissertation a novel method based on the second approach is defined for the design and fabrication of high Q inductors and resonators. The new method not only resulted in a higher quality factor comparing to the other counterparts but also benefits from facility design and ease of fabrication.

1.1 Review of previous works

The traditional inductors were commonly used in the megahertz frequency range but due to their high inductance and high parasitic capacitance, they cannot maintain their performance characteristics above a few gigahertzes (GHz). To increase the working frequency of the inductors in the past 15 years, Micro-inductors were developed. The first approach is to make the inductors on chip.

On-chip inductors such as micro-spirals [9], [19], [20], [21], micro-solenoids [22]-[26], and micro-toroidals [27], [28] have been extensively studied in the literature. Among the circuit parameters related to micro-inductors is the parasitic capacitance between the coil and the ground, which has a significant effect on the resonance frequency and the quality factor of the actual inductor. For example, On-chip micro-spirals have large parasitic capacitance between the coil and the substrate. However several design techniques including ground shielding, suspended micro-coils, and isolation layers have been developed to decrease this capacitance. Nevertheless, the On-chip micro-spirals are not able to provide Q-factors over 100 [29], [30]. Alternatively, to overcome the parasitic capacitance different On-chip micro-solenoid structure schemes have been made, but they require complex fabrication. For example to make a suspended micro-solenoid with a low parasitic capacitance, one needs five layers of photolithographic patterning. Regardless of the improvements in their Q, these coils are currently unreliable as commercial devices in the market [31].

A few approaches have been proposed to enhance the quality factor by making Off-chip micro-inductors. New substrates were used for the sake of lower parasitic capacitance. Soh et al. used a high resistivity silicon wafer to build the micro-solenoid using vias through the wafer [32]. Nevertheless this method had an uncommon fabrication process and it did not receive a Q-factor higher than 18.5. Yoon et al. and Lu et al. have used Pyrex glass as the substrate which decreased the capacitive coupling and substrate loss in the fabrication of micro-solenoids [33], [34]. However the resulting quality factor was still less than 100. Other approaches were the application of alumina as a microwave substrate, system on package (SOP) using LTCC, and organic packaging substrates for making spiral and helical RF-inductors. These techniques can provide Q-factors higher than 100, but they all suffer from multi layer and costly fabrication process [35]-[37].

1.2 Application of printed circuit board vias for the fabrication of inductors

Functional components such as resonators, matching circuits, and filters are commonly made by PCBs. In a recent study, a microwave substrate material with a low relative dielectric of 2.2 was used for making micro-toroidals using a microstrip or stripline [38]. The Micro-toroidals were fabricated using vias fabricated through a microstrip. This research showed an improvement of 1.5 times when compared to the conventional micro-spiral inductors. Due to the microstrip grounding layer in the middle of the toroidal, the maximum Q was received in the frequency less than 1.25 GHz and the thickness of actual multilayer dielectric board became more than 3 mm. Although they have received quality factors higher than On-chip inductors, the application of monolithic

commercial microwave printed circuit board (PCB) production with common thicknesses for the micro-electronic structures has not been investigated in the literature. Due to available printed circuit board techniques, the application of Standard PCB method for Micro-inductor fabrication will decrease the cost, and complexity of the device when compared to the other counterparts.

Application of microwave PCBs as a dielectric substrate for micro-inductors is not only important for the commercialization and ease of fabrication but also becasue it benefits from variety of different relative dielectric permittivity, and substrate thicknesses available in PCB materials. The permittivity is a major parameter to decrease the loss in the substrate and optimize the quality factor. The current study was done to find a commercial monolithic design and creation method for micro-solenoids with low parasitic capacitance using common microwave PCBs.

This work describes the design, fabrication, and test of novel Off-chip solenoid inductors for RF frequency applications. The Inductor consisted of a monolithic micro-solenoid embedded inside a RT/Duroid 5880 circuit board.

The low relative permittivity of 2.2 in this substrate helped to maintain low stray capacitance as well as low loss for the fields inside it to yield a high Q [39], [40]. Each turn of the solenoid inductor included one top conductor patterned through the copper cladding layer over the board and a couple of copper vias attached to the top layer to connect two sides of the board, and then a bottom conductor layer under the PCB to make a loop. A schematic diagram of a three turn Micro-solenoid is in Figure 1.2. Due to the

difficulty of drilling high aspect ratio vias close to each other, this effort used a drilling diameter of 0.250 mm in order to achieve the maximum possible resonance frequency. Laser drilling at 0.150 mm diameter is also commercially available at higher costs. The authors had difficulty making laser drilling vias in a tight proximity filled with metal. In fact, several attempts were required by the vendor to achieve the vias required for this project. Various lengths, heights, and pitch sizes were modeled to find the best response. A set of the resulting devices with different size parameters based on our modeling was used to optimize experimental resonant frequency and quality factor.

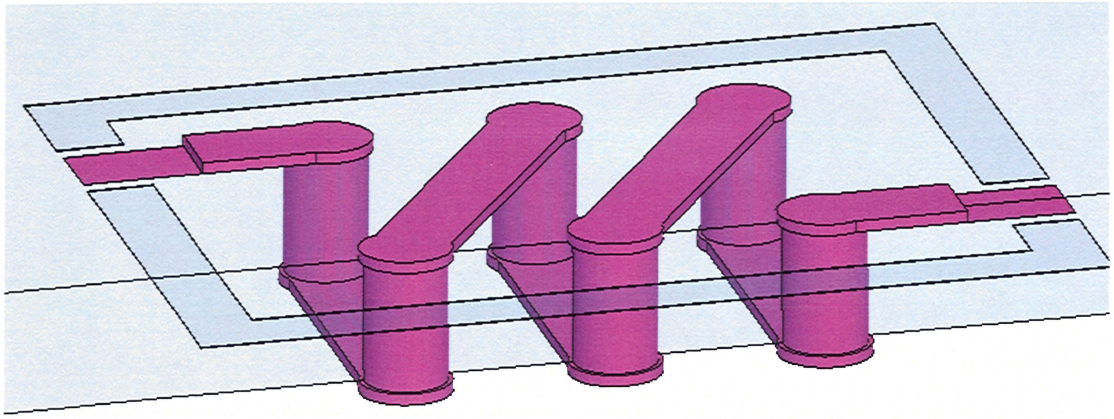

Figure 1.2 Schematic diagram of two turn solenoid in Duroid substrate.

Two modeling techniques were used for investigation of the circuit. Analytic modeling of the circuit was done using a single π-circuit model. Also an electromagnetic simulation of device was done with Ansoft-HFSS software. Simulated results were

compared to the S-parameters of the fabricated devices measured experimentally using a microwave probe station. Both the Inductance and quality factor were evaluated. Experimental data shows close agreement with modeling and simulation. Again, the low cost standard PCB production techniques decreased the cost, and complexity of device commercialization when compared to micro-inductors counterparts.

1.3 Dissertation organization

The objective of this dissertation is the design, simulation, and fabrication of novel off-chip solenoid inductors and resonators with high quality factors and using commercial dielectric substrates such as RT/Duroid. In the next chapter the analytical modeling of the 3D structures using Thru-hole vias is covered. In Chapter 3, the high frequency simulation using the electromagnetic software is explained. This work is followed by the microwave measurement methods and the calibration process for the micro-inductors in Chapter 4. Then in Chapter 6, the fabrication of an OFF-chip Micro-solenoid inductor using the Thru-hole vias is demonstrated. Chapter 6 examines the Micro-solenoid structured for the fabrication of the microwave resonator using the Thru-hole vias and an embedded capacitor in series with the circuit. The future works and the conclusion of this study are in Chapter 7.

CHAPTER 2

ANALYTICAL MODELING OF 3D STRUCTURES USING THRU-HOLE VIAS

2.1 Introduction

Analytical modeling is an important technique for the design and improvement of passive devices. It provides a convenient method for the realization of component features using the device parameters and dimensions before going through a costly fabrication process. As such, extensive studies have been done in the literature to improve models for On-chip and Off-chip Micro-inductors and resonators. There are two primary techniques utilized for such system, the lumped and the distributed circuit models [11], [41]. If the related device dimensions on all sides of the component are less than $\lambda/10$, then a lumped circuit model can be used for the component. As a result, closed form equations are applicable. Also software solutions provide numerical methods to study the Micro-inductor using an analytical model. The validation of the lumped circuit model in this approach allows for various different electromagnetic modeling software package tools to be used for this project. Such software provides a numerical method to study the passive devices.

Application of the analytical model allows the determination of device dimensions. For various quality factors and resonant frequencies, the resulting circuit model using this method is acceptable for the estimation of frequency response up to the resonant frequency, but it is not well enough to predict the higher frequency characterization accurately [13], [42]. To overcome these requirements, numerical methods were used by the application of electromagnetic simulators. In general the numerical analysis software was used to solve Maxwell's equations in the related boundary conditions using one of the numerical methods. The two commonly reported techniques are the finite element method (FEM) and the method of moments (MoM). The finite element method is a fully 3D solution and has been used in software packages such as Ansoft HFSS, and CTS Microwave Studio. It benefits from higher flexibility for the complex 3D structures. Also it will take skin effect, proximity effect, and discontinuities in various different metallic and dielectric geometries. The method of moment is a quasi-3D technique that has commonly been used for planar devices. It is not accurate enough for evaluation of Q in high frequencies for this study. Software packages such as Agilent ADS, Ansoft Designer use this method.

Boundary conditions and port excitations should be accurately designed to provide a good result from the EM-simulation. Simulations are performed in a box with boundary conditions defining radiation modes. The walls are at least one wavelength far away from the device [43]. Terminals of the device are also being exited using terminal exited lumped ports. Due to the large number of meshed elements required for a complex

structure like a Micro-solenoid in this study, the simulation requires a fair amount of computational power depending on the size and number of turns.

One needs to have a good model for the inductor to make a well designed coil. This also helps the designer extract the circuit parameters from the measurements and simulations. Optimization of the device is possible with a control over the circuit parameters of the related model. Inductors are evaluated by several different factors such as quality factor, inductance, etc., but some of the factors are not extractable from the S-parameters directly. Evaluation of these factors can be realized using the analytical modeling and the circuit parameters [44]. Several different equivalent circuits have been reported for the On-chip and Off-chip inductors [17], [45]. Single-π and double-π circuit models are more preferred than the others. In this study single-π was considered as an equivalent circuit model for a high frequency inductor. This work will focus on a π-model and electromagnetic simulation to evaluate every individual component. Then the model will be used for characterization of the Micro-solenoid and Micro-resonator in the other chapters.

2.2 Single-π model

The most used modeling technique for high frequency inductor application is a single π-circuit. Figure 2.1-a illustrates this model applicable for inductors separated by an insulator from the ground [46].

The equivalent circuit has five major components for evaluation. The inductive feature of the component is named Ls and includes the total self and mutual inductance related to this coil. The turn by turn capacitance, which is familiar as stray capacitance, is named C_s in this circuit model. The R_s represents ohmic resistance of the conductor. Also the capacitance between the inductor and the ground shielding is named C_p. Q-factor is considered as a measure of the resolution for this solenoid. The quality factor can be calculated after finding all circuit parameters.

At low frequencies, the turn by turn capacitance will become negligible and the inductance model can be considered like Figure 2.1-a. In the high frequency applications, the capacitance between turns will become significant [17], and therefore considered as C_s in Figure 2.1-b. Evaluation of the parameter is studied in the next sections.

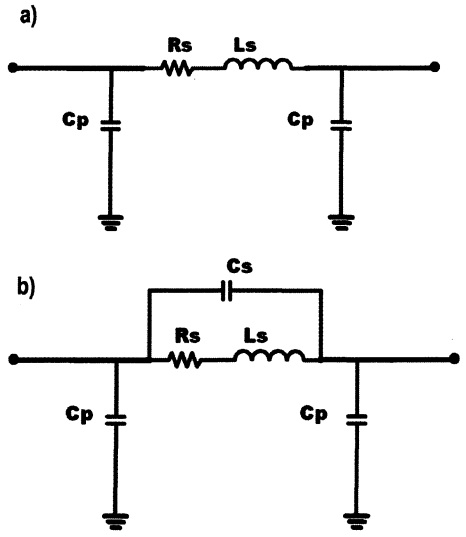

Figure 2.1 Equivalent circuit model of Micro-inductor using a) microstrip model, and b) lumped model with interturn capacitance [12].

2.2.1 Series inductance

The total inductance is a major parameter in the circuit. It consists of the self and mutual inductance of the coil turns. Different methods were reported for the analysis of inductance such as the Microstrip model [17], the Greenhouse model [47], [48], and the Wheeler model [49]. The Microstrip model is restricted for planar inductors and was not a preferred method for solenoids. Both the Greenhouse-Grover and Wheeler models were investigated for the current research. The Greenhouse method was chosen for evaluation of inductors throughout this study because the Wheeler method is limited to the square shaped cross-sections and is not applicable to rectangular cross sections.

A. Greenhouse model

A coupling mode evaluation of the total inductance was reported by Greenhouse and Grover [48]. This method provides the inductive feature of the coil from DC to the frequency ranges below the resonant frequency of the circuit model. Basically, this calculation is related to the frequency by considering the skin effect. Total inductance was obtained by adding self inductances of each individual segment to the algebraic sum of the values for the mutual inductances.

In this chapter, both cylindrical and rectangular segments were considered. Also an evaluation of the mutual inductance between all segments was required. The self inductance of a circular via such as Figure 2.2-a is located inside the substrate. Thus the term via is named L_{cs} with the approximate value in nH equal to [47].

$$L_{cs} = 0.2h\left[\ln\left(\frac{2h}{0.5w}\right) - 1 + \frac{0.5w}{h} + \frac{\mu T}{4}\right] \quad , \qquad (2.1)$$

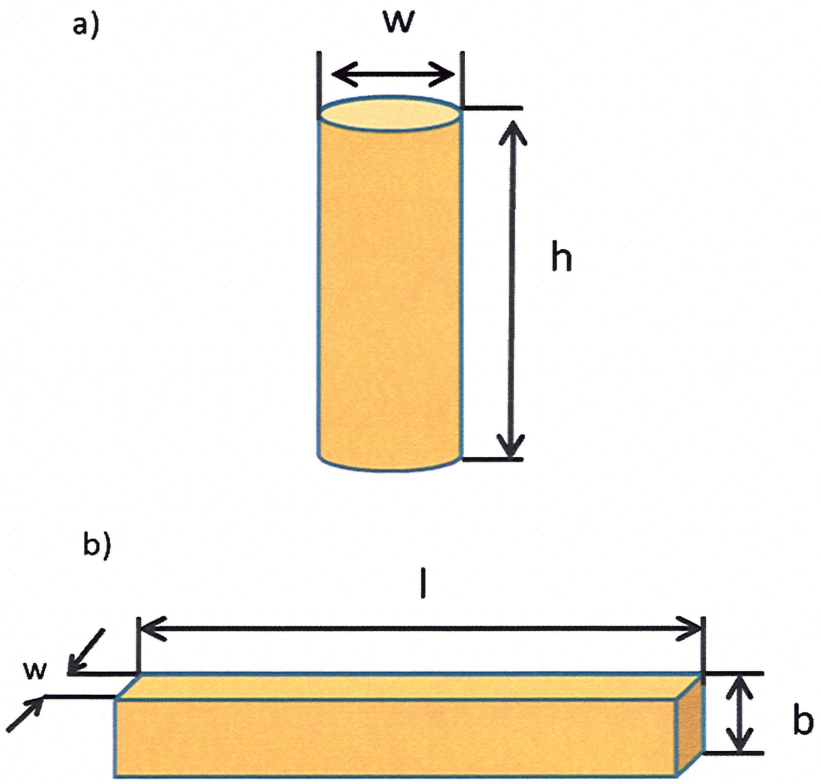

Figure 2.2 Dimensions of the segments a) cylindrical (via) segments, and b) rectangular (surface conductor) segments.

where **h** is the height and **w** is the diameter of the segment. The relative permeability μ of the metal conductor was considered one for materials such as copper due to the very high frequency of the current application. The skin effect contribution of T was considered

approximately one by Greenhouse for frequencies higher than 1 GHz. T is related to frequency and will be less than one for frequencies lower than 1 GHz [47]. Then, the simplified formula is

$$L_{cs} = 0.2h\left[\ln\left(\frac{2h}{0.5w}\right) - 0.75 + \frac{0.5w}{h}\right] \quad . \tag{2.2}$$

A rectangular wire is depicted in Figure 2.2-b. If b would be the thickness of the copper, w the width of the segment, and 1 the length, then the self inductance of a rectangular wire, L_{rs}, in nH can be approximately evaluated by [47].

$$L_{rs} = 0.2l\left[\ln\left(\frac{2l}{b+w}\right) + 0.25049 + \left(\frac{b+w}{3l}\right) + \frac{\mu T}{4}\right] \quad . \tag{2.3}$$

For T=1, and μ=1, the simplified equation is going to be

$$L_{rs} = 0.2l\left[\ln\left(\frac{2l}{b+w}\right) + 0.50049 + \left(\frac{b+w}{3l}\right)\right] \quad . \tag{2.4}$$

The mutual inductance of M between each couple of segments like two elements in Figure 2.3, can be evaluated by [47].

$$M = 2lG \tag{2.5}$$

The resulting mutual inductance is positive if the current in both segments is in the same direction and negative if it is in the opposite direction. The value of l is the length of the segment. To find the geometric mean distance, G, the following relations can be used:

$$G = \ln\left[\left(\frac{l}{D}\right)+\left(1+\frac{l^2}{D^2}\right)^{1/2}\right]-\left[1+\left(\frac{D^2}{l^2}\right)\right]^{1/2}+\left(\frac{D}{l}\right) \tag{2.6}$$

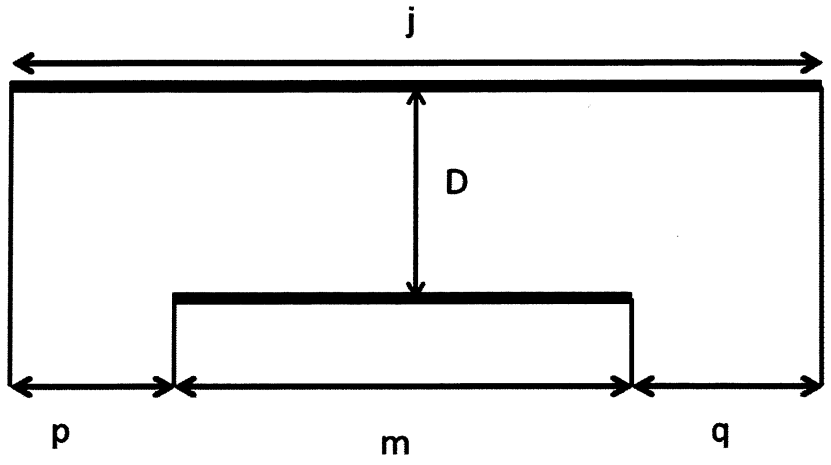

Figure 2.3 Geometry of two parallel segments of different lengths.

where D is the parameter that relates the dimensions of the inductor to the geometric mean distance. To find D the following equation is used:

$$\ln(D) \cong \ln(d) - \left[\frac{1}{12}\left(\frac{d}{w}\right)^2\right] + \left[\frac{1}{60}\left(\frac{d}{w}\right)^4\right] + \left[\frac{1}{60}\left(\frac{d}{w}\right)^6\right] + \left[\frac{1}{60}\left(\frac{d}{w}\right)^8\right] + \left[\frac{1}{60}\left(\frac{d}{w}\right)^{10}\right], \quad (2.7)$$

where the value of d is the distance between the centers of two tracks and w the width of the track. The total inductance of L_T is the sum of all self inductances of and mutual inductances of M for m segments of the coil:

$$L_T = \Sigma_{s=1}^{m} L_{0-s} + \Sigma_{s=1}^{m} \Sigma_{i=1, i \neq s}^{m} M_{si} \quad . \quad (2.8)$$

The values of mutual inductances are reduced by the distance between segments, so the major mutual inductances happen between adjacent conductors. It helps us to evaluate the mutual and self inductance of one turn solenoid and simplify the formula due to the reoccurrence of the turns. The next formula gives a close approximation for the total inductance of a solenoid of n turns:

$$L_T \cong (n+1)L_{one_{turn}} - nM_{one_{turn}} \quad . \quad (2.9)$$

B. Wheeler method

Unrestricted formulas for evaluation of circular and square solenoids was reported by H. A. Wheeler in 1982 [49]. The dimensions are $2a$ for the length of the square and b for the axial length. Other symbols are the number of turns n, the relative permeability μ, and inductance reduction factor K. The inductance value was evaluated using the K parameters as

$$L = \left(\frac{\mu_0 n^2 4a^2}{b} \right) K \quad . \quad (2.10)$$

For a square loop of length $2a$, the radius is considered:

$$r = \frac{2a}{b} \quad . \quad (2.11)$$

And K is evaluated using

$$\frac{\pi}{2}K = a\tan\frac{\sqrt{1+2r^2}}{r^2} + \frac{1}{r}\left(\operatorname{asinh} r - \operatorname{asinh}\frac{r}{\sqrt{1+r^2}}\right) - r\left(\operatorname{asinh} 1 - \operatorname{asinh}\frac{r}{\sqrt{1+r^2}}\right)$$
$$+ \frac{1-\sqrt{r^2}}{3\left(1+\sqrt{1+r^2}\right)\left(\sqrt{r^2}+\sqrt{1+r^2}\right)}$$
$$- \frac{\sqrt{1+r^2}-\sqrt{2r^2}}{3\left(\sqrt{1+r^2}+\sqrt{1+2\sqrt{r^2}}\right)\left(\sqrt{2r^2}+\sqrt{1+2r^2}\right)} \quad . \tag{2.12}$$

For a short solenoid, the inductance was be simplified to

$$L = \frac{4\mu_0 n^2 a}{\pi}\left(\ln\left(1+\frac{\pi a}{b}\right) + \frac{1}{3.64+\frac{2a}{b}+0.51(b/a)^2}\right) \quad . \tag{2.13}$$

Also for a long coil, the inductance was approximated to

$$L = \frac{4\mu_0 n^2 a}{\pi}\left(\ln(1+0.5a) + \frac{2.67}{1.26+\frac{b}{a}}\right) \quad . \tag{2.14}$$

2.2.2 Series capacitance

The series capacitances for a single independent circuit are located between the segments from the first terminal to the second. The so called stray capacitance depends on the cross section, distance, and the dielectric constant between segments. Frequently

reported methods for evaluation of stray capacitance include the segment method and the feed forward closed form method [46], [15]. Both were defined and commonly investigated in the literature for solenoid inductances. The feed forward closed form method is applied for air core solenoids and is often developed for circular coils. It is possible to find an average value for the radios of the rectangle and use the closed form [26]. But in this study, it is not considered the best candidate for the estimation of stray capacitance in a rectangular solenoid due to lower accuracy. However the segment model is a good method for the calculation of capacitance in all segments and was used in this research.

A. Closed form model feed forward capacitance

The feed forward capacitance was used for finding the capacitance between two adjacent turns in a solenoid structure as depicted in Figure 2.4. This fringing capacitance was expressed as

$$C_{one-t} = \frac{\pi^2 D \varepsilon_0 \varepsilon_r}{\ln\left[\frac{p}{2r} + \sqrt{\left(\left(\frac{p}{2r}\right)^2 - 1\right)}\right]} \quad , \tag{2.15}$$

where D is turn diameter, p is the pitch size, and r the conductor radius. For n turns solenoid, it can be evaluated as

$$C_n = \frac{C_{one}}{n-1} \tag{2.16}$$

For a single turn to shield capacitance, the estimated value is

$$C_{one-s} = \frac{2\pi^2 D\varepsilon_0\varepsilon_r}{\ln\left[\frac{h}{r}+\sqrt{\left(\frac{h}{r}\right)^2-1}\right]} \tag{2.17}$$

Here h is the distance between the central axis of the coil and the shield.

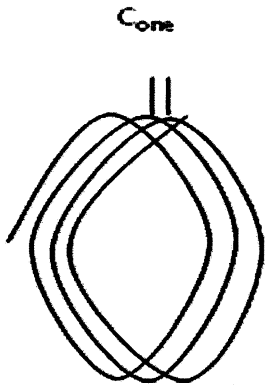

Figure 2.4 Turn to turn capacitance in a circular solenoid.

B. Segment model stray capacitance

Despite the fact that the capacitances between vias are much higher than the other segments, in the calculation of C_s for the n turn solenoids, the capacitance between all adjacent segments was considered and it made a close estimation. Figure 2.5 depicts different capacitive features in a segment modeling of solenoid; the capacitance C_d will be added for the fabrication of a resonator. The stray capacitance is formulated as follows:

$$C_S \cong \varepsilon_0 \frac{\left[(2n-1)l_t + 2nl_b\right]b}{(d-w)} + \varepsilon_r\varepsilon_0 \frac{nl_t w}{\left[h^2 + (0.5d)^2\right]^{\frac{1}{2}}} + \varepsilon_r\varepsilon_0 \frac{(2n+1)hw}{l_b} + \varepsilon_r\varepsilon_0 \frac{2n(2b+h)}{d} \quad (2.18)$$

Each segment makes a capacitance to the ground. They made parallel capacitive features of the two port network. It was called C_p and consisted of the lower segment capacitances of C_L and upper segment capacitances of C_U.

$$C_p = \frac{1}{2}\left(C_L + C_U\right) \quad , \quad (2.19)$$

where C_L and C_U are

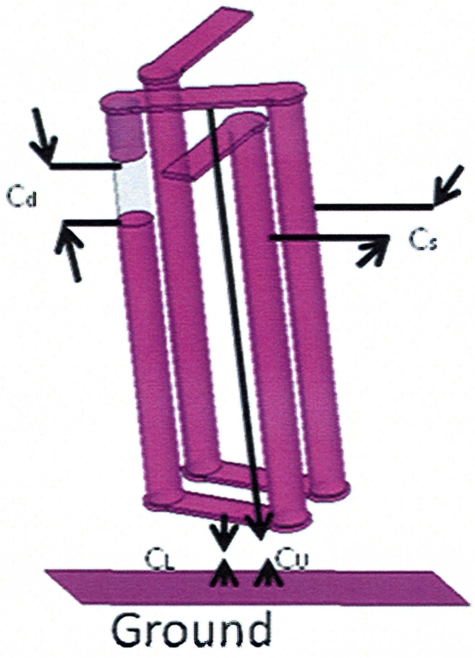

Figure 2.5 Different capacitive features in a segment modeling of solenoid capacitances.

$$C_L = \frac{\varepsilon_r \varepsilon_0}{2} \frac{(n+1) w l_b + (2n+2)\left(\frac{w}{2}\right)^2 \pi}{l_{sub}} \tag{2.20}$$

$$C_U = \frac{\varepsilon_0}{2} \frac{nwa}{n+b+l_{sub}} \tag{2.21}$$

2.2.3 Resistance

The series resistance of the coil is contributed by the ohmic features of the conductor. It is very dependent on both skin effect and proximity effect defined by the distance between the conductors. The eddy current loss also increases the resistivity of

solenoid. Two major methods for evaluation of the solenoid resistance are the segment model and closed form formula. Both models were considered for study and provided very close values.

A. The closed form resistance value

This model takes the benefit of considering both the skin effect and proximity effect. Of course the proximity effect was only considered between the adjacent turns. If the series resistance of a wire with rectangular cross section would be considered as R_S then this resistance is given by

$$R_S = R_{dc} \frac{t}{\delta\left(1 - s^{-\frac{t}{\delta}}\right)} \quad , \tag{2.22}$$

where R_{dc} is the dc resistance of the coil with thickness of t and width of w. R_{dc} is equal to

$$R_{dc} = \frac{\rho l}{A} \quad . \tag{2.23}$$

The value of A is the cross section of the conductor. The length is l and the resistivity is ρ. Also the δ is the skin depth and t is the thickness of the conductor. The skin depth δ as illustrated in Figure 2.6, for the permeability of μ and frequency of f, is given by [50]

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad , \tag{2.24}$$

Where μ and f are permeability of copper and frequency, respectively.

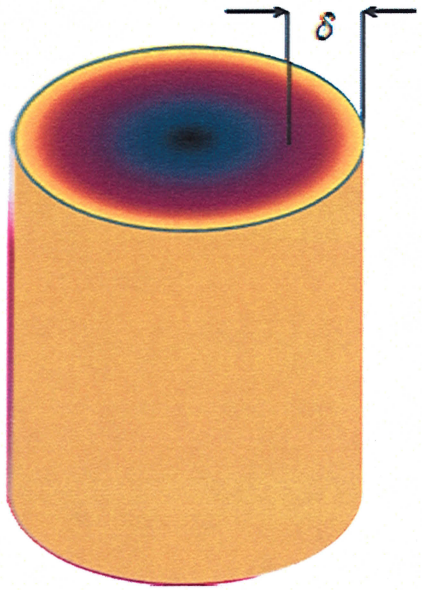

Figure 2.6 Skin depths, for a high frequency signal passing through a cylindrical conductor.

B. Segment model resistance

The series resistance includes the resistances of surface conductors in series with the resistances of the columns. As in equation (2.25) the skin effect also should be considered for this calculation.

$$R_S = \frac{c\rho[(2n+2)h]}{\delta(\pi w)} + \frac{c\rho\left[(n+1)a + n\left[a^2 + (0.5d)^2\right]^{\frac{1}{2}}\right]}{\delta(2w+2b)} \quad , \tag{2.25}$$

where c is a constant which can be considered one in this experiment [15]. Also ρ is the resistivity of copper.

2.2.4 Quality Factor

The major parameter to show the resolution of the inductor coil is the quality factor or Q. It is the given as

$$Q_{Inductor} \equiv \frac{Energy\_stored\_in\_the\_inductor\_in\_one\_cycle}{Energy\_loss\_in\_the\_inductor\_in\_one\_cycle} \quad . \tag{2.26}$$

This can be estimated as

$$Q_{Inductor} \approx \frac{\omega L}{R_s(\omega)} \text{(Self Resonance Factor)(Eddy Current Loss Factor for Substrates)} \quad . \tag{2.27}$$

For the equivalent π-model of the circuit, the quality factor was evaluated by [17]

$$Q_{Inductor} = \frac{\omega L_S}{R_S}\left[1 - \frac{R_s^2\left(C_s + C_p\right)}{L_s} - \omega^2 L_s\left(C_s + C_p\right) - \omega R_s\left(C_s + C_p\right)\right] \quad . \tag{2.28}$$

CHAPTER 3

HIGH FREQUENCY SIMULATION

The lumped circuits provided by analytical modeling for inductors are the quick approach for designing of the device in the target frequency. It also provides the dimensions and the final structure for the coil. However, analytical modeling is not adequate to cover all the high frequency features of an inductor [13]. Electromagnetic simulation using the finite element analysis (FEA), finite difference time domain (FDTD), or method of moment (MOM) software is another method for evaluation of a high frequency device [51]. Accurate EM-simulation often results in close matches to measured device performance and provides more flexibility for the structural design. The simulation results are often provided in terms of measurement parameters such as the scattering matrix, impedance matrix, and admittance matrix [7]. To extract the final value for each of the components in the circuit, one need to use the high frequency relations applicable for calculation of the inductive, capacitive, and resistive values of a passive model. The same method can be used for the evaluation of the fabricated device and extraction of the circuit elements. To provide an accurate measurement, the microwave station set up and the related calibration need to be applied.

The current chapter will cover an overview of the HFSS, an EM-simulation software package and discuss the benefits of its use with regards to the inductor design application. Then the 3D design for micro-solenoid through the PCB is described. The next section is the analysis of the component in the frequency range.

3.1 Electromagnetic simulation using Ansoft HFSS

The flexibility of modern electromagnetic simulation packages has made them a favorite method for the study of high frequency devices in recent years. These applications often require powerful computers with large amounts of RAM and multi-core processors. For example, Ansoft HFSS needs 8 Giga-bits RAM and a 4 core processor for its most recent version [42]. However EM-simulations benefit from high accuracy, making them worthwhile evaluate complex designs prior to fabrication. Simulations incorporate 3D computer aided design (CAD) modeling and use Maxwell's equations over the electric and magnetic terms. After applying the boundary conditions, the lay out will be exited through ports using terminal currents or modal fields as a known source. Then the differential equation will be solved and the field current components will be found. As a result of that, high frequency aspects like skin effect, proximity effect, eddy loss, and discontinuities will be taken into effect.

There are different solving methods available in the EM-simulation software based on time domain or frequency domain. The most frequently used methods are the finite elements (FEM) method and method of moments (MoM) [13]. Ansoft HFSS uses the FEM and Sonnet Software uses the MoM. They both apply the analysis in the

frequency domain and use a mesh division to find the unknown values in small subsets and apply the boundary and field to the next subsets.

The resulting values in the EM-simulation software are very close to each other and accurate. In this study Ansoft HFSS was used for the simulations and will be covered in the current chapter. First the creating of 3D structures will be described, then the analysis will be covered.

3.2 Three-dimensional (3D) design

To create a 3D structure for simulation in Ansoft HFSS, one need to perform the following settings in the HFSS OPTIONS of the software:

- Create new boundaries.
- Duplicate boundaries with geometry.
- Automatically cover closed polylines.
- Edit property of new primitives.

A project should be opened, and due to the current excitation in the solenoid device, the solution type is going to be the driven terminal. For this application, due to having different size dimensions from tens of millimeters to microns, the model unit will be set into millimeters. To make the structure after choosing the material for each element of the device, a 3D-CAD toolbar can be used. Every single part should be made and then they will be united as in Figure 3.1.

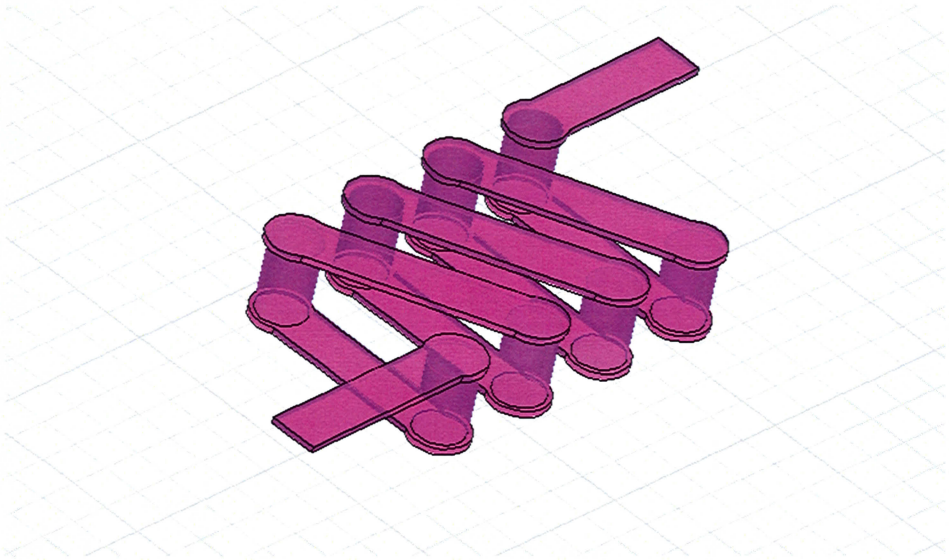

Figure 3.1 Three turn solenoid structures created using Ansoft HFSS Cad tools.

After making the conductor, then the substrate Duroid body should be added. This can be done by choosing the material and making a box using that. For solenoid application, two thicknesses of 0.380 mm and 3.010 mm were considered. The surface dimension of the boxes can be made using squares of 3 mm to 10 mm side dimensions. The box needs to be extruded by the via holes. The via can be made by subtracting a copy of the conductor from the substrate. Duroid was considered as the substrate material for the solenoid inductor. The Box and the vias are given in Figure 3.2.

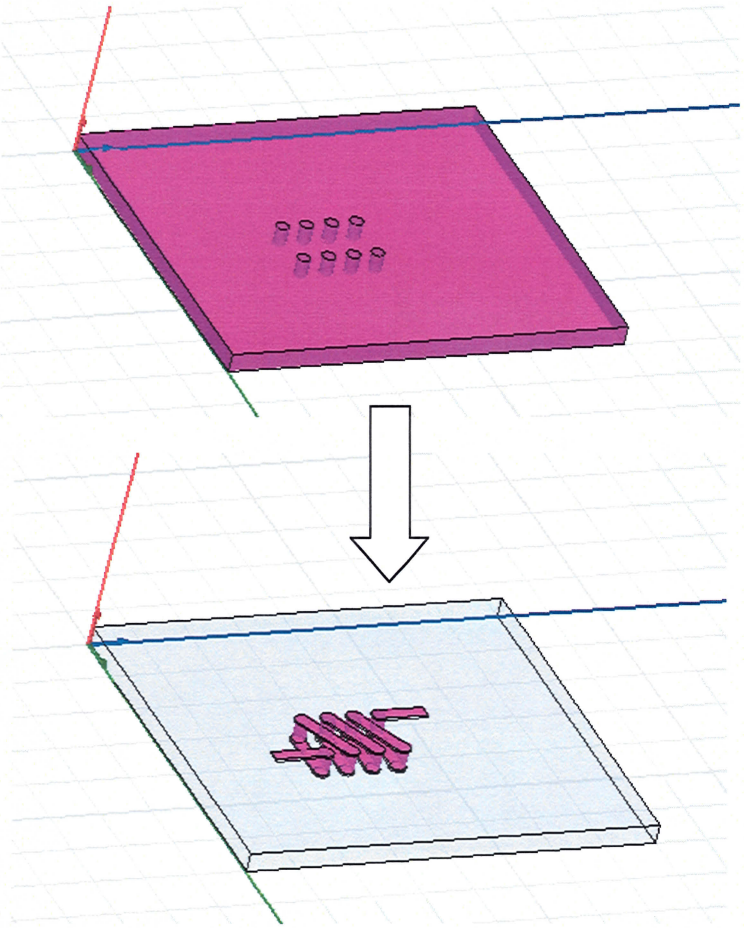

Figure 3.2 The substrate and vias for the three turns solenoid.

The solenoid conductor needs a return path to make a closed circuit. In the microwave circuits, it is considered as a ground for a two port network. In most EM-Simulation software packages, this will be made by a perfect conductor (PEC). Here to make things more close to the actual fabricated samples, this pad was made using the same copper material as the solenoid conductor. The excitation ports will be added between this conductor pad and the coli terminals. A model of this ground pad is depicted in Figure 3.3.

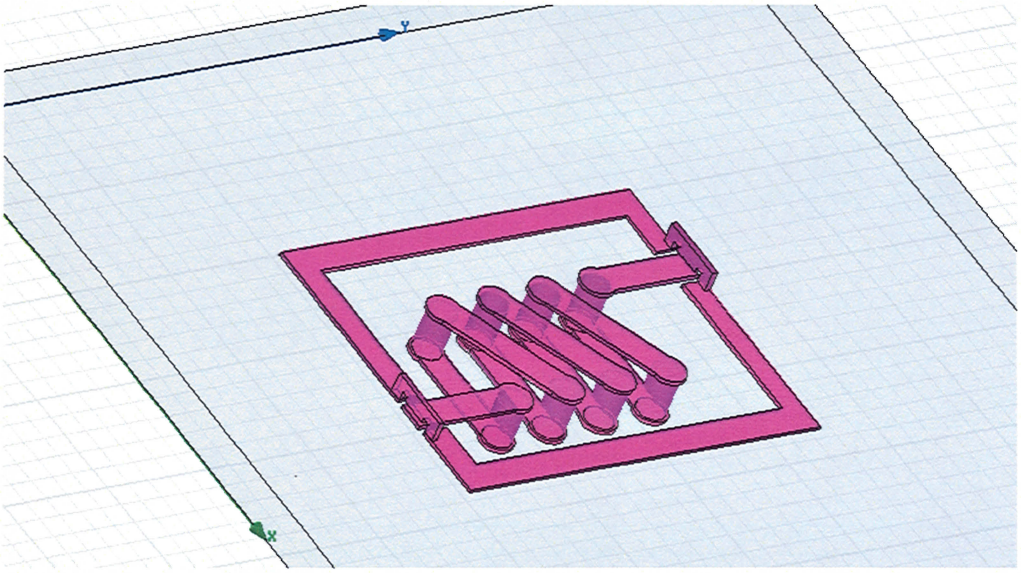

Figure 3.3 Ground pad created for a two-port network solenoid.

Excitation of the solenoid should be a driven terminal due to the conduction of the currents in the metal. As a result of that, two lumped ports need to be used. The lumped port shape must to be a small rectangle without thickness. Every rectangle should be put in between two high conductivity materials such as metals. The size on the connection side can be one half of the metallic side. Also the port should not be located near the corners of the inductor terminal. If the software did not make the excitation line through the lumped port, one needs to assign this vector in the middle of the rectangle, followed by choosing 50 ohm terminal impedance. The total metallic conductors including the excitations are in Figure 3.4.

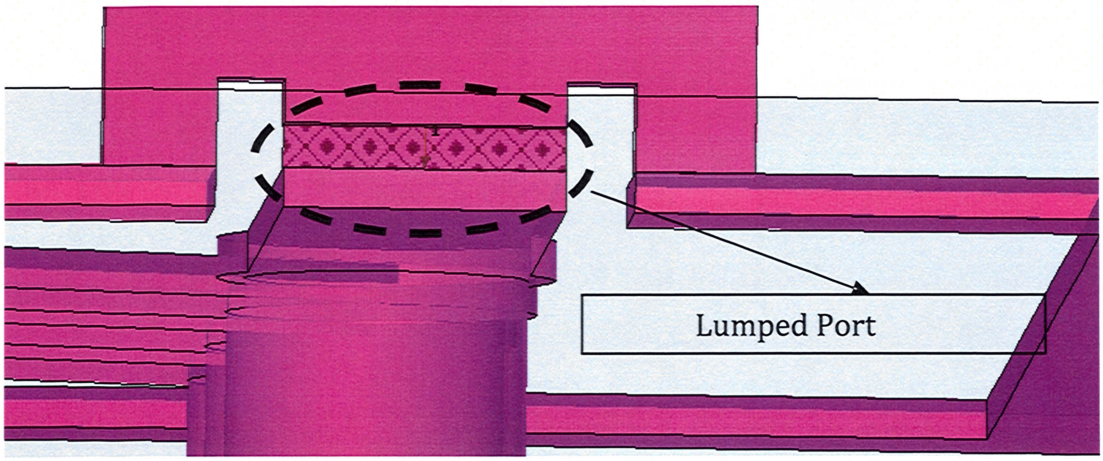

Figure 3.4 One of the lumped ports connected between the terminal and the pad.

The total created passive component needs to be put in a box for the simulation. This box can be made by choosing air or vacuum as the material and creating a large cube with dimensions that make the device at least $\lambda/4$ far from the cube walls. At the bottom of this cube, a rectangle can be made to show the effects of the measurement chuck. It should assign a perfect E in the boundaries setting to perform as a metallic ground chuck. The other boundaries are going to be all the other cube surfaces. These should be assigned in the boundary to radiation boundaries. The radiation boundaries will be considered as unlimited free space by the software. A picture of the related cube with the perfect ground and all its radiation boundaries is given in Figure 3.5.

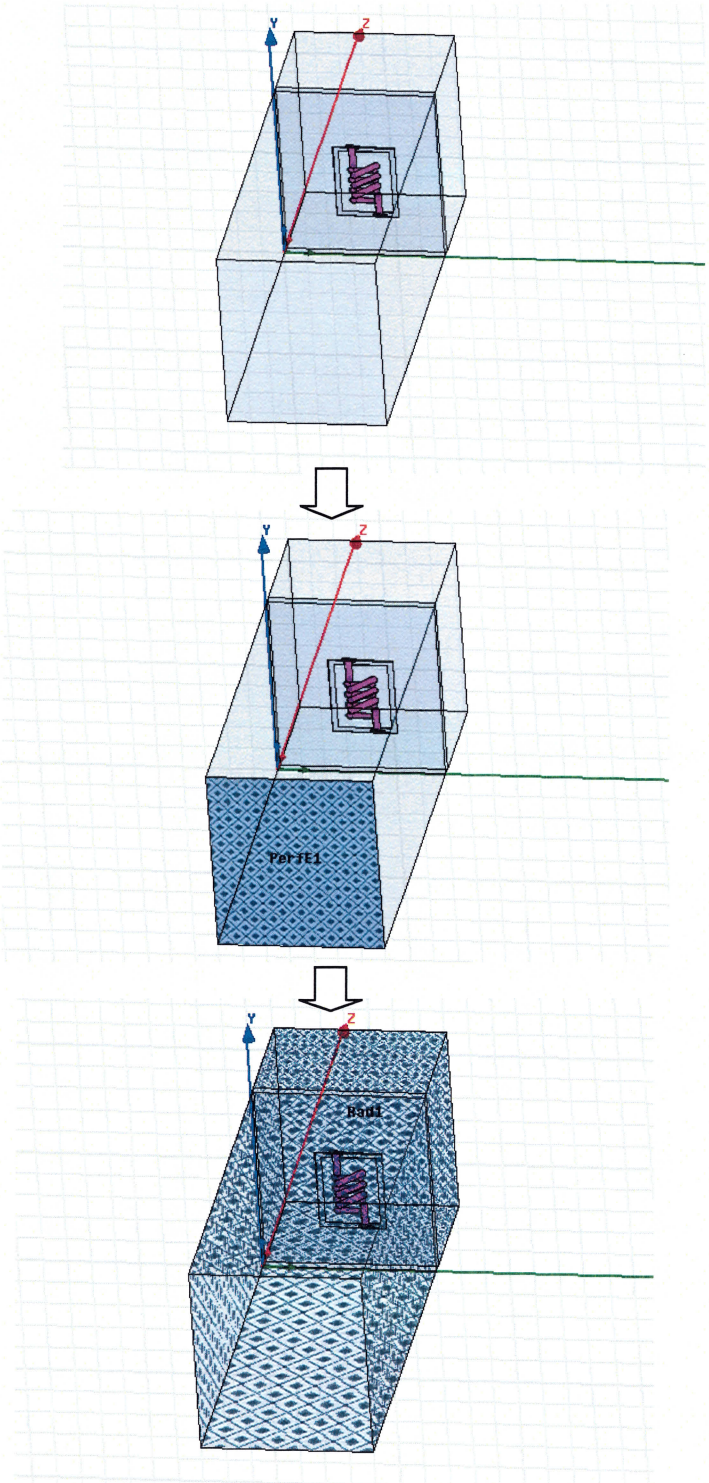

Figure 3.5 Boundary conditions and perfect E field effects are added to the solenoid design.

3.3 HFSS Analysis

Evaluation of the component will be done by creating an analysis setup in the general tab. A Solution frequency is going to be selected based on the resonance frequency of the component. For a three turn solenoid of thickness 0.380 mm, the resonance frequency can be estimated around 8 GHz. The rest of the settings are

- Maximum number of 20 passes.
- Maximum Delta of 0.02.
- Do lambda refinement with target of 0.05.
- Use lower order solution bases.

After making the analysis setup, one needs to add a sweep between the minimum and maximum target frequencies. The step number between these two frequencies should be such that it makes an integer number of steps between two limits. Error tolerance of 0.5% and a maximum solution of 20 are the last settings necessary for the sweeping.

When the simulation analysis setup is made, the circuit can be checked for validation and then start the analyzing. It will take a few minutes to a few hours to run the simulation due to the complexity of the component.

Simulation will automatically check the convergence of the resulted data. If the result is not converging, it will be documented in the message box window for consideration by the user. Drawing reports will be made by going to HFSS results and

choosing the related two port parameter such as admittances, impedances, and scattering parameters. In Figure 3.6 the S-parameters report of a three turns solenoid of 0.380 mm thickness is given. Other formulas can be added to make new reports using the two port network parameters. Any formula can be added in output variables. Then the new formula will available in the two-port matrix report window. Creating a report using that will be the same as every other two-port parameter.

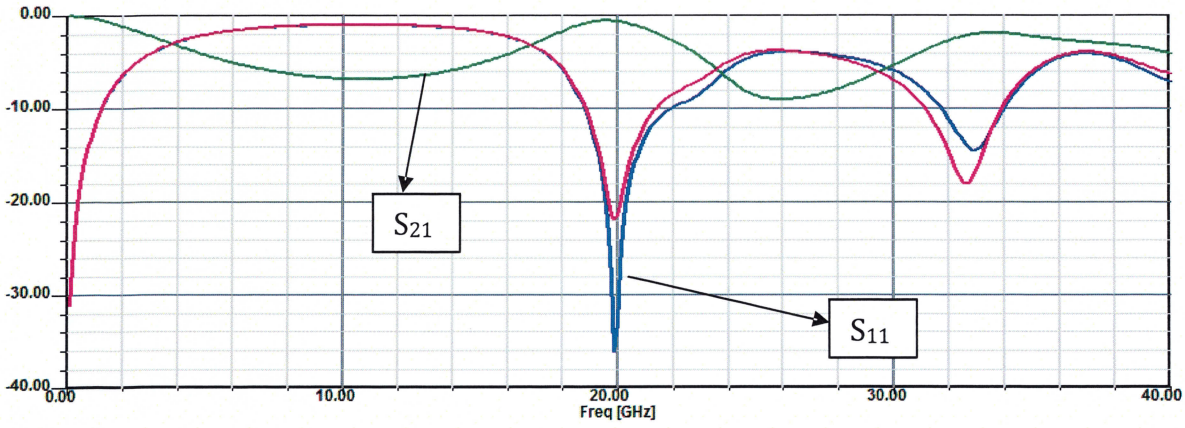

Figure 3.6 S-parameters of a three turns solenoid simulated by Ansoft HFSS.

CHAPTER 4

MICROWAVE MEASUREMENT THEORY

The accuracy of microwave measurement depends on the measurement system and calibration. High frequency measurement of electronic components is not easy to perform in the time domain. The reason is the lack of fast data acquisition systems to capture and process the multi Giga Hertz responses. Even using the fastest oscilloscope in the market, one can measure up to few Giga Hertz. On the other hand, the circuit dimensions are close to the wave length, so the signals are going to behave like traveling waves.

An alternative to analyzing a fabricated component is to consider the device like an N-port network. For an N-port network, one can apply the excitation signal over the terminals of the device and measure the effects of this wave on the terminals. This needs an RF-measurement station with the related set up and accurate calibration, to reduce the noises and errors after that. The two-port network parameters can be used to evaluate the other related variables, such as the inductance and capacitances of the circuit model in Figure 2.1-b.

In this chapter the high frequency parameters for an N-port network will be covered. Then the circuit model of high frequency inductors will be evaluated for extraction of every element. Finally the last section describes the measurement equipment and the calibration method.

4.1 N-Port network

Electrical and electronic circuits can be modeled as N-port networks for overall evaluation of the component as illustrated in Figure 4.1. Using that, measurement of the device can be done more easily especially for high frequency applications. If a known circuit model would be applied to the network, then every element of the circuit can be evaluated using the measurement results. Several different matrices are presented for the N-port networks like Impedance matrix, and admittance matrix [11]. The Z-parameters and Y-parameters are given as

Z-parameters:

$$Z_{ij} = \left.\frac{V_i}{I_j}\right|_{I_k=0 \, for k \neq j} \tag{4.1}$$

Y-parameters:

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0 \, for k \neq j} \tag{4.2}$$

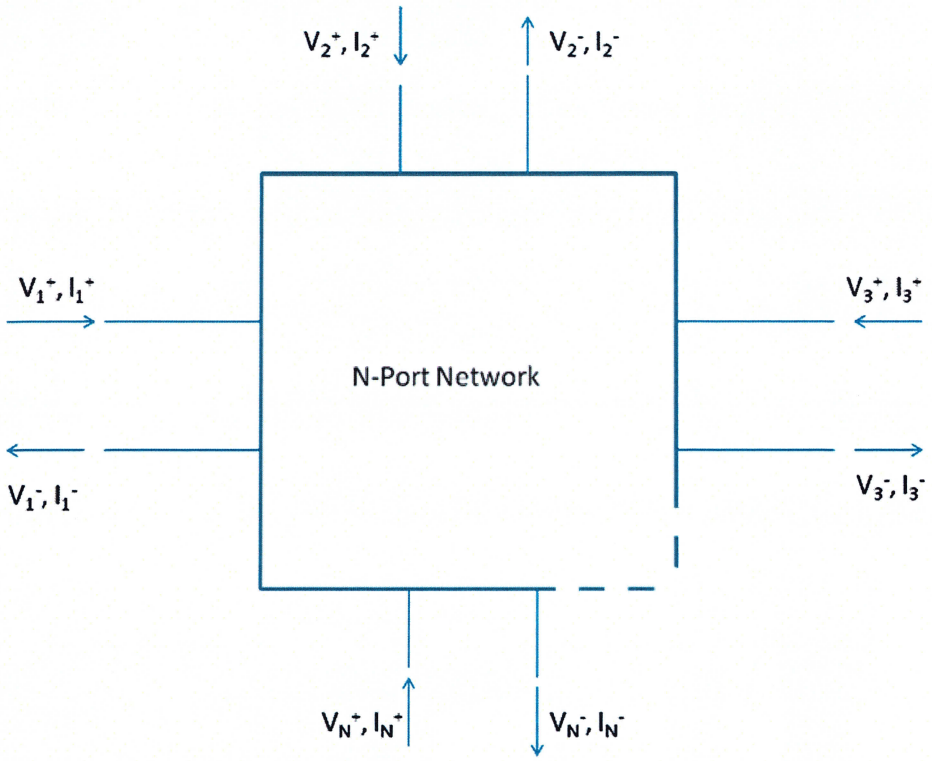

Figure 4.1 A microwave network model of N-port.

For reciprocal networks, the Z-parameters which relate every two-port together will be equal. In other words, the matrices will be symmetric [52].

In high frequency applications, the voltage or current is not a good measure of the terminal behavior, because the radio frequency signals will be considered only in a particular direction. Instead of these, one can use the reflection waves and characterize in the port using a scattering matrix. S-parameters or scattering matrices are defined by the incident waves and reflection waves. If the S_{11} and S_{22} are scattering parameters and S_{12}

and S_{21} are forward and reverse transmission parameters respectively, then these are given by [53], [54]

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{4.3}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \tag{4.4}$$

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+ = 0} \tag{4.5}$$

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+ = 0} \tag{4.6}$$

$$S_{12} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+ = 0} \tag{4.7}$$

$$S_{21} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+ = 0} \tag{4.8}$$

Every network parameter can be converted to the other desirable other parameter. Since the measurement results of a network analyzer is in S-parameters, it is frequently changed into Y-parameters for evaluation of the circuit models [55]. Also Yue

converted the S-parameters to the transmission matrix or ABCD-parameters for evaluation of the inductor circuits [17], [56]. The admittance matrix or Y-parameters of a two-port network can be calculated by S-parameters using [10], [57]

$$y_{11} = \frac{(1-s_{11})(1+s_{22})+s_{12}s_{21}}{Z_0(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.9}$$

$$y_{22} = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{Z_0(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.10}$$

$$y_{12} = \frac{-2s_{12}}{Z_0(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.11}$$

$$y_{21} = \frac{-2s_{21}}{Z_0(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.12}$$

The characteristic impedance of the line or Z_0 is 50 Ω. The S-parameters also can be evaluated using the admittance parameters by [11]

$$s_{11} = \frac{(1-y_{11}Z_0)(1+y_{22}Z_0)+y_{12}y_{21}Z_0{}^2}{(1+y_{11}Z_0)(1+y_{22}Z_0)-y_{12}y_{21}Z_0{}^2} \tag{4.13}$$

$$s_{22} = \frac{(1+y_{11}Z_0)(1-y_{22}Z_0)+y_{12}y_{21}Z_0{}^2}{(1+y_{11}Z_0)(1+y_{22}Z_0)-y_{12}y_{21}Z_0{}^2} \tag{4.14}$$

$$s_{12} = \frac{-2y_{12}Z_0{}^2}{(1+y_{11}Z_0)(1+y_{22}Z_0)-y_{12}y_{21}Z_0{}^2} \tag{4.15}$$

$$s_{12} = \frac{-2y_{21}Z_0{}^2}{(1+y_{11}Z_0)(1+y_{22}Z_0)-y_{12}y_{21}Z_0{}^2} \tag{4.16}$$

Another application for the two-port network parameters conversion is the de-embedding [58]. Effects of the pad are algebraically de-embedded from the measured values. To obtain the de-embedded values of inductor, the Y-parameters of the pad only should be subtracted from the measured values for solenoid with pad. The resulting values are the effect of inductor circuit without parasitic. Equation (4.17) shows the relation for de-embedding [58].

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{De-embedded\_Inductor} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{Inductor\_with\_Pad} - \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{pad} . \tag{4.17}$$

4.2 Measurement circuit model

Inductors are one of the fundamental components of every RF-circuit. It can be used either in parallel or series in the circuit. The series connection of an inductor means the two terminals of the inductor are used in the circuit; in other words, neither of these terminals are grounded. In the parallel connection, one of the junctions will be grounded

while the other one is being used in the circuit. Both models are reported for evaluation of the inductor performance [17], [27]. The series model was investigated in the current work. Then the result of the series inductor can be used to derive the parallel model.

For a solenoid inductor in the Duroid board, the same single π-circuit as discussed in Chapter 2 will be used. This network provides two capacitors, one inductor, and one resistor. De-embedded Y-parameters or ABCD-parameters were reported for the extraction of the circuit [17]. Yue used the transmission matrix for evaluation of the generic inductor circuits using (4.18)-(4.21) [11].

$$A = \cosh(ly) = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{2s_{21}} \tag{4.18}$$

$$B = Z_0 \sinh(ly) = \frac{Z_0(1+s_{11})(1-s_{22})-s_{12}s_{21}}{2s_{21}} \tag{4.19}$$

$$C = \frac{1}{Z_0}\sinh(ly) = \frac{(1-s_{11})(1-s_{22})-s_{12}s_{21}}{2s_{21}} \tag{4.20}$$

$$D = \cosh(ly) = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{2s_{21}} \tag{4.21}$$

The parallel and series branch of a π-network as given in Figure 4.2 is in Equations (4.22), and (4.23) respectively [17].

$$Z_p = \frac{2Z_0}{ly} \tag{4.22}$$

$$Z_s = Z_0 ly \tag{4.23}$$

The propagation path length multiplied by propagation constant (ly) is evaluated using the average of A and D. Then using the values of ly and B (also equation (4.19)), the characteristic impedance Z_0 is calculated. Having ly and Z_0, the parallel and series impedances are evaluated with (4.22) and (4.23).

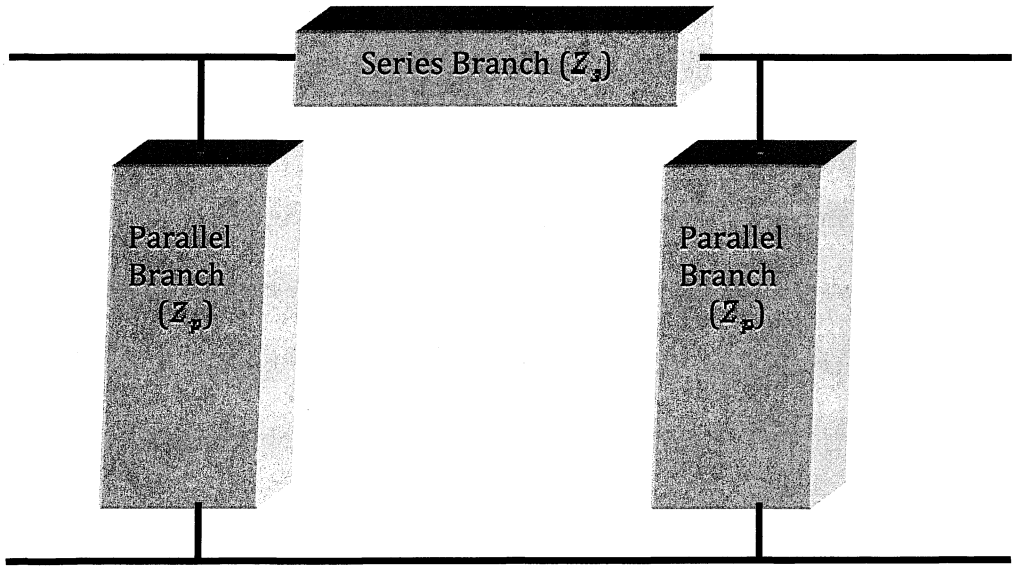

Figure 4.2 Block diagram of a single π-network.

Branch impedances show the characteristic of each arm in the π-network. To extract the values of every component in each arm, the π-network of Figure 4.3 is used [9].

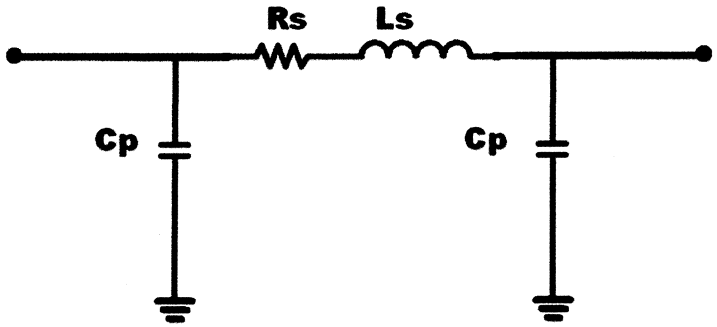

Figure 4.3 A simple π-circuit model of the inductor.

Then the network components can be evaluated with the following equations:

$$Z_s = R_s + j\omega L_s \tag{4.24}$$

$$R_s = \mathrm{Re}(Z_s) \tag{4.25}$$

$$L_s = \frac{\mathrm{Im}(Z_s)}{\omega} \tag{4.26}$$

$$Z_p = R_p - \frac{j}{\omega C_p} \tag{4.27}$$

$$R_p = \mathrm{Re}(Z_p) \tag{4.28}$$

$$C_p = \frac{-1}{\omega \,\mathrm{Im}(Z_p)} \tag{4.29}$$

S-parameters were converted to Y-parameters using (4.9) to (4.12). Then the parallel and series arms of the π-network can be evaluated with the Y-parameters. For a reciprocal circuit, the relation between the two-port admittance matrix and the π-network parameters is given in the following equations [11]:

$$y_{21} = y_{12} = \frac{-1}{Z_s} \tag{4.30}$$

$$y_{11} = y_{22} = \frac{1}{Z_s} + \frac{1}{Z_p} \tag{4.31}$$

The real and imaginary part of inversed y_{12} will be used for finding the R_s and L_s values respectively. Then the values of R_s and L_s to y_{11} will be applied and the real and imaginary parts of y_{11} will be used to find the R_p and C_p.

For a defined π-network model, the quality factor also can be calculated using the two-port parameters. If the second terminal of the inductor would be grounded, then the

first terminal can be used for the measurement of the input impedance. The input impedance using the π-network components is given by

$$Z_{in} = \frac{1}{\frac{1}{R_p} + j\omega C_p + \frac{1}{R_s + j\omega L_s}} \qquad (4.32)$$

The imaginary part and real part of the resulted impedance can be used to find the Q-factor using [27], [59]

$$Q \equiv \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} \qquad (4.33)$$

The impedance value of (4.32) can be measured using the Y-parameters of the two-port network. For a solenoid with a second terminal connected to the ground, Z_{in} can be evaluated by

$$y_{11} = Z_{in} \qquad (4.34)$$

The y_{11} was commonly used in literature for the calculation of quality factor and inductance as given in equations (4.35), and (4.36). However it is not reflecting the exact value for Q and L_s, but it is useful for the comparison of this work with the other published results.

$$Q \equiv \frac{\mathrm{Im}\left[\frac{1}{y_{11}}\right]}{\mathrm{Re}\left[\frac{1}{y_{11}}\right]} \tag{4.35}$$

$$L = \frac{\mathrm{Im}\left[\frac{1}{y_{11}}\right]}{\omega} \tag{4.36}$$

The circuit model described so far is an easy method for evaluation of the parameters using the measured values, but it is not valid for frequencies close to the resonance frequency. The reason is the lack of a stray capacitance element in the model. This capacitance is the representative of the turn by turn capacitances of a solenoid. Although the direct capacitance between the input and output terminals is very low in a solenoid, the turn by turn capacitance is not negligible and will rise in higher frequencies. A circuit model including the stray capacitance was offered in Figure 4.4. The two-port π-network including stray capacitance has a capacitance of C_s in parallel to the series branch.

The parallel arms in Figure 4.4 show the capacitance of solenoid to ground shielding as well as the resistance incorporated through the Duroid for the upper layer conductor's capacitance to the shielding (C_u in Figure 2.5).

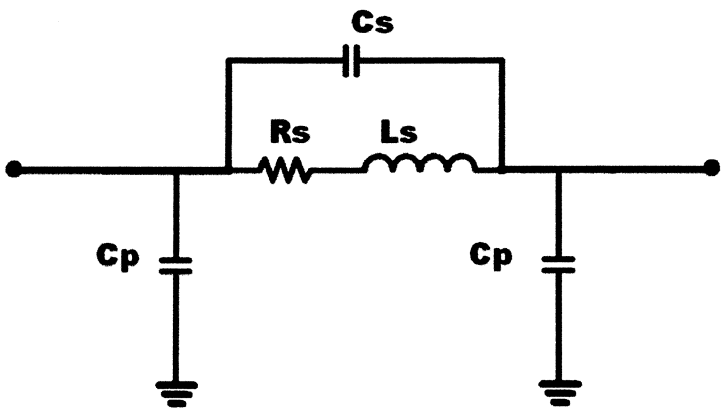

Figure 4.4 A two-port π-network for the solenoid design.

The magnetic energy is only stored in the series inductor. The electric energy is stored both in the parallel branch capacitors and the series branch capacitor. Dissipation of energy will happen in the parallel branch resistors and the series branch resistor. Increasing the peak stored magnetic energy will raise the quality factor, but increasing the peak stored electric energies or the parasitic dissipations of energy will decrease the quality factor. Every parallel arm provides a resistance of R_p and a capacitance of C_p. For a symmetrical solenoid circuit, the impedances of these parallel arms are the same. Therefore the values of parallel resistances are equal. Also, the values of the parallel capacitances are equal. Extraction of the parallel arm components is straightforward. The real part of the parallel impedance Z_p is the resistance R_p, as given in (4.34). The imaginary part of Z_p gives the capacitance C_p using equation (4.35).

$$R_p = \mathrm{Re}[Z_p] \tag{4.34}$$

$$C_p = \frac{-1}{\omega(\mathrm{Im}[Z_s])} \tag{4.35}$$

High frequency effects should be considered for the evaluation of the parameters in the series arm. When the frequency of the signal increases, the charge distribution in the conductor will change due to the skin effect. The skin depth, δ, and the change in the value of the series resistance were given in (3.13) and (3.14) respectively. Of course the stray capacitance value is due to the fringing field between conductors, so it was considered a frequency independent component [17]. The following procedure describes the extraction of the parameters in a series branch of the circuit. The real part of impedance in the series branch provides the series resistance of R_s and is given in equation (4.36). The imaginary part of impedance in the series branch gives the series inductance as in equation (4.37). After evaluation of L_0, which is the value of the inductance in low frequencies, the stray capacitance, C_s, will be evaluated using equation (4.38) at the resonance frequency. The resonance frequency can be measured using the peak value of the series branch impedance [60].

$$R_s = \mathrm{Re}[Z_s] \tag{4.36}$$

$$L_s = \frac{\mathrm{Im}(Z_s)}{\omega} \tag{4.37}$$

$$C_s = \frac{1}{L_0 \omega_0^2} \tag{4.38}$$

The series RC circuit can be altered to parallel RC in order to simplify the circuit model. Then the quality factor of the solenoid inductor can be calculated using the equivalent π-network of Figure 4.4. For easier measurement, the terminal two of the solenoid circuit was connected to the ground. The voltage drop across the inductor can be easily calculated using a voltage divider. Then the average magnetic power stored in inductor can be calculated using

$$Peak\_of\_Magnetic\_Energy\_Stored = \frac{V_{11-peak}^2 \omega L_s}{2[(\omega L_s)^2 + R_s^2]} \quad . \tag{4.39}$$

The average of electric power is the power stored in the capacitors and can be calculated using

$$Average\_ElectricEnergy\_Stored = \frac{V_{11-peak}^2}{2}(C_p + C_s) \quad . \tag{4.40}$$

The average power loss in the resistors is given by

$$Average\_Energyloss\_per\_Cycle = \frac{\pi V_{11-peak}^2}{\omega}\left(\frac{R_s}{[(\omega L_s)^2 + R_s^2]} + \frac{1}{R_p}\right) \quad . \tag{4.41}$$

The quality factor of inductor can be calculated by putting (4.39), (4.40), and (4.41) into (4.42) and the simplified Q_{Ind} is given in (4.43).

$$Q_{Inductor} = \frac{Average\_Magnetic\_Energy\_Stored - Average\_Electric\_Energy}{Energy\_Loss\_in\_Resistors\_per\_Cycle} \quad (4.42)$$

$$Q_{Ind} = \frac{\omega L_s}{R_s}\left[\frac{1}{1+\frac{R_s}{R_p}\left[\left(\frac{\omega L_s}{R_s}\right)+1\right]}\right]\left[1-\frac{R_s^2\left(C_s+C_p\right)}{L_s}-\omega^2 L_s\left(C_s+C_p\right)\right] \quad (4.43)$$

In equation (4.33) the quality factor of the inductor was measured using a direct measurement method and the Q was determined using the measured components of the lumped circuit model in equation (4.43). Both methods are reported in the literature for other types of inductors such as spirals and toroidals [17], [26]. The first one is easier and can be considered as the Q-factor of the total inductor circuit even if there is not a valid lumped model for the coil. The second one can be considered as the quality factor of the coil only and reflects the inductive features of the solenoid. Equation (4.43) shows three multiplied terms. The first term is the quality factor of an ideal inductor with a series resistor. The second term shows the loss factor that happens due to the dissipation of energy inside the Duroid substrate.

The Duroid substrate has a very high resistivity and it makes R_p close to infinity and the second term close to one If the second term would be one, then the maximum value of Q with respect to this term would be made. To increase the value of R_p in the model, there should not be any material other than the Duroid or an insulator with higher resistivity between the solenoid and the metallic chuck in the measurement setup. The third term is the self resonance effect and the total parallel and series capacitance of the circuit determine that.

4.3 Measurement setup

A microwave measurement station was designed and assembled to test the high frequency characteristics of the device under test (DUT). High frequency micro-probes were used to perform an accurate measurement in the radio frequency range. Micro-manipulators are used to position each probe. Probes are connected through SMA connectors and RF cables to a HP8363 Programmable Network Analyzer (PNA). This network analyzer is capable of taking up to 12000 samples in the frequency span. Figure 4.5 shows the microwave probe station and network analyzer used for the measurements.

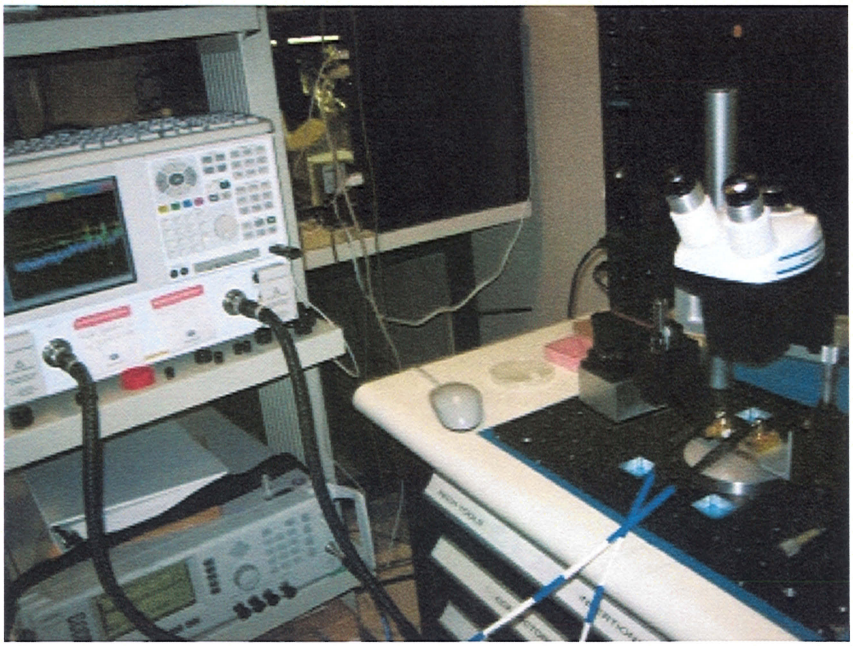

Figure 4.5 The microwave probe station with the PNA HP 8363 network analyzer.

To keep the accuracy as well as high speed scanning of the frequency span on the PNA, a sampling rate of 6000 was selected and applied. Using the micro-probes, the S-parameters can be extracted on-board. On-board measurement of DUT will eliminate the effects of fixtures, wires, and junctions. Ground pads were added to the micro-solenoid to make a two port network as depicted in Figure 4.6. The pad forms a ground signal ground (GSG) connection and connects the ground in the left terminal to the ground in right terminal. Pads are necessary to provide terminals for the connection of the inductor to the test probes and a ground connection for the two port device. Probes should be carefully positioned to touch the pads without extensive contact damage at the connection. Gold pads are very easy to damage, so the adjustments should be performed very slowly.

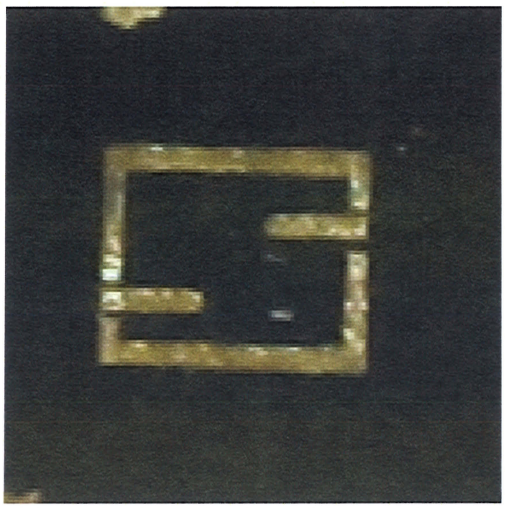

Figure 4.6 The ground pad without inductor is depicted.

The ground in microwave measurement is the return path, and it provides a closed loop for the circuit [61]. An unwanted parasitic of pad was taken out by de-embedding of the pad characteristics. To perform the de-embedding a dummy pad was made and measured. Then the effects of the PAD were subtracted out of DUT using equation (4.16).

4.4 Calibration

S-parameters were measured by sweeping frequency over the 100 MHz to 40 GHz range and measuring the reflections in each port [11]. Before starting the inductor measurement, the microwave station setup should be calibrated down to the tip of the micro-probes. The short-open-load-thru (SOLT) calibration was done by an Impedance Standard Substrate (ISS). A diagram of the short calibration is given in Figure 4.7-a. Then the probes are calibrated for open condition as depicted in Figure 4.6-b. The load test using standard 50 Ω load and Thru test for calibration using a delay line are illustrated in Figure 4.7-c and 4.7-d. The ISS made by Micro-tech was used for calibration. A calibration file was defined using the probe parameters and the software was up loaded to the network analyzer. Then the SOLT calibration procedure was followed using the ISS. De-embedding of the pads was carried out after conversion of the S-parameters to Y-parameters [58]. The GSG Cascade Micro-tech probes shown in Figure 4.8 were used for the on board measurements of micro-solenoid.

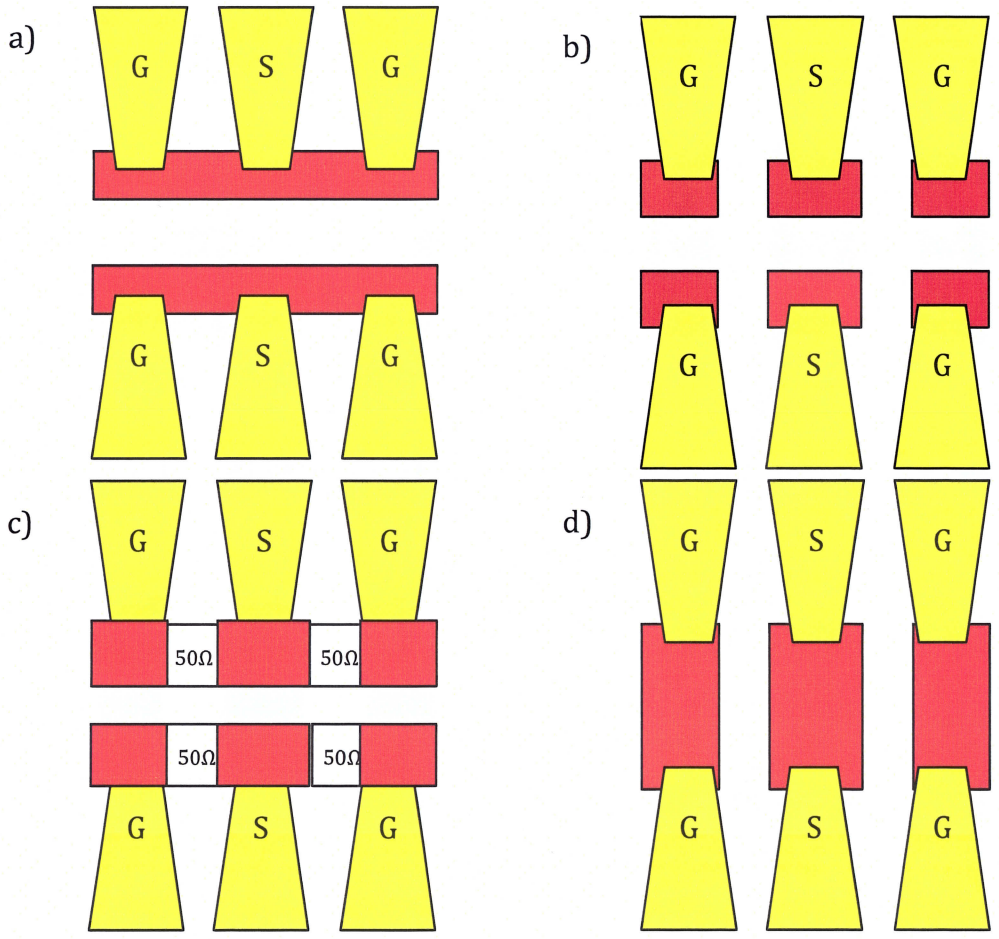

Figure 4.7 Diagrams for the SOLT calibration steps of a) short calibration, b) open calibration, c) 50 Ω load calibration, and d) Thru test calibration using a delay line.

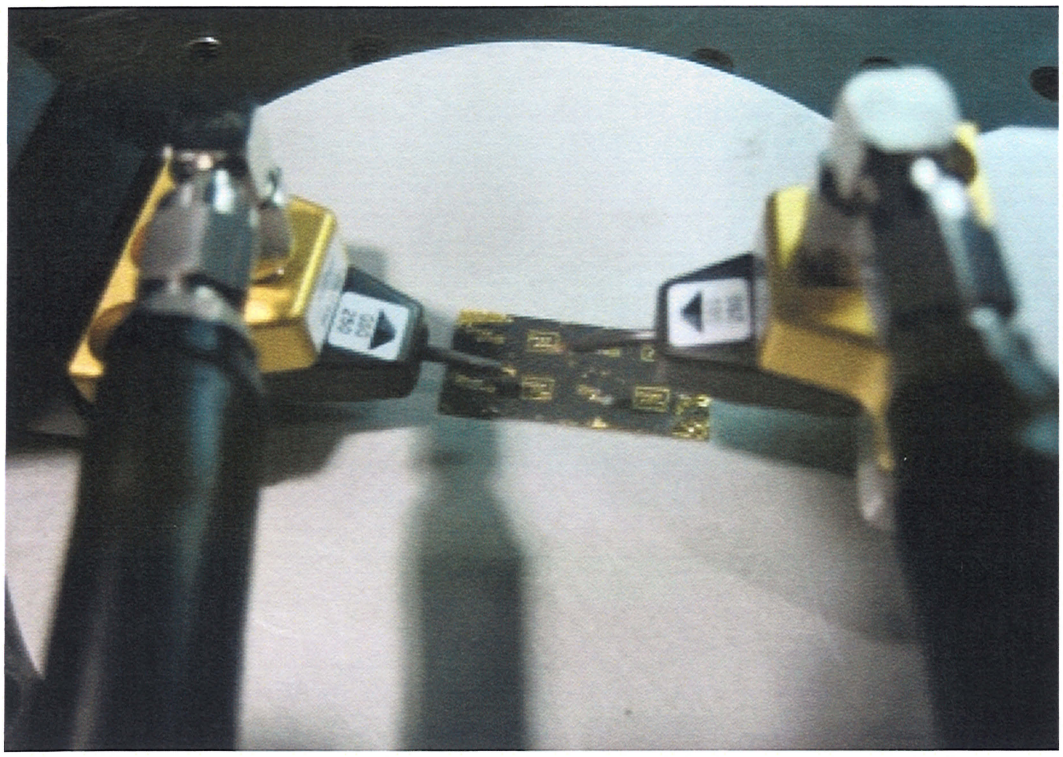

Figure 4.8 The GSG Cascade Micro-tech probes used for the on board measurements of micro-solenoid are illustrated .

CHAPTER 5

FABRIACTION OF OFF-CHIP MICRO-SOLENOID INDUCTORS USING THRU-HOLE VIAS

High quality factor inductors are key components in RF-circuits. Manufactured on-chip coils are costly and suffer from low Q-factors. In this chapter, the design, simulation, and fabrication of novel off-chip solenoid inductors with high quality factors is presented. The minimum commercial drilling size of standard PCB production was used to make embedded solenoids in a Duroid substrate with 2.2 relative permittivity. Different pitch sizes, conductor lengths, solenoid heights, and numbers of turns were simulated and produced. The maximum quality factor of 160.3 was received with a resonance frequency of 9.25 GHz. In addition to the very high Q-factor, the inductor benefits from facilitated design and ease of fabrication.

Analytical design is investigated by a lumped circuit model and electromagnetic simulation. Then the measurement of the fabricated samples is covered. The S-parameter measurements are compared to the simulation results and the analytical model. The resulting micro-solenoids had a higher quality factor compared to all other counterparts.

5.1 Micro-inductors and Micro-solenoids

Radio frequency micro-structured inductors are currently being developed to optimize the transmission and filtering features for microwave applications like radars, satellite communications, and medical sensors. This technology is also of interest in next generation wireless communication devices and biomedical instruments [62]. To fulfill these requirements, different design techniques have been developed for the miniaturization of inductors [63]-[67]. This chapter represents a new method for the design and fabrication of high quality factor micro-solenoids.

This chapter describes the design, fabrication, and testing of novel Off-chip solenoid inductors for RF frequency applications. The inductor consisted of a monolithic micro-solenoid embedded inside a RT/Duroid 5880 circuit board. The low relative permittivity of 2.2 in this substrate helped to keep a low stray capacitance as well as low loss for the fields inside it to yield high Q [39], [68].

Each turn of the solenoid inductor included one top conductor patterned through the copper cladding layer over the board and a couple of copper vias attached to the top layer to connect the two sides of the board, and then the bottom conductor layer under the PCB to make a loop. A schematic diagram of the solenoid is in Figure 5.1. Drilling high aspect ratio vias close to each other limited the drilling diameter and conductor distances to 0.250 mm in order to achieve the maximum possible resonance frequency. Various lengths, heights, and pitch sizes were modeled to find the best response.

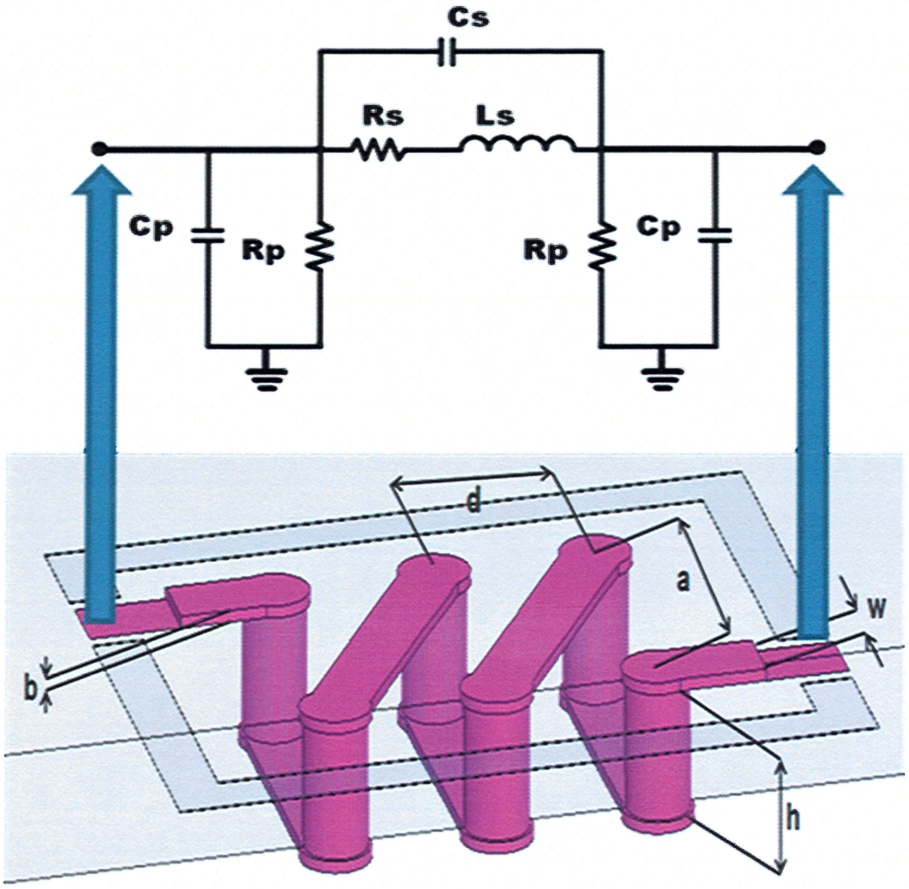

Figure 5.1 Schematic diagram of two turn solenoid in Duroid substrate.

A set of the resulting devices with different size parameters based on our modeling was used to optimize experimental resonant frequency and quality factor. Simulated results were compared to the S-parameters of the fabricated devices measured experimentally using a microwave probe station. Both the inductance and quality factor

were evaluated. Experimental data shows close agreement with modeling and simulation. Again, the low cost standard PCB production techniques decreased the cost and complexity of device commercialization when compared to micro-inductors counterparts.

5.2 Analytical circuit model of the Micro-solenoid

The single π-circuit model of Figure 5.1 was used for the analytical modeling of the micro-solenoid. All solenoid dimensions are shown in Figure 5.1. The height of the inductor is h, the thickness of the copper layers is b, the width of the segment is w, and the length is l. Using the inductor dimensions, the values for the circuit model components can be equated.

The total inductance of L_s is the algebraic sum of all self inductances and mutual inductances for m segments of the coil. The values of mutual inductances are reduced by the distance between segments, so the major mutual inductances happen between adjacent conductors. It helps us to evaluate the mutual and self inductance of one turn and simplify the formula due to the reoccurrence of the turns. The self inductance of a circular via and the self inductance of a rectangular conductor are given by equations (2.2) and (2.4) respectively. Also the mutual coupling between the segments is calculated with equation (2.5). As a result of these inductances, a total inductance of L_T was evaluated using equation (2.8).

The capacitive behavior of this device includes the two different capacitances of C_s, and C_p. The turn to turn capacitance between segments is called C_s and calculated using equation (2.18). The turn to turn capacitance is also called stray capacitance and depends on the cross section, distance, and the dielectric constant between the segments. The parallel capacitance of C_p is between the segments and ground. Based on the position of the segments, capacitances are in air or inside the Duroid substrate with the dielectric constant of 2.2. All segments and the capacitances between them have been considered in the following model. The value for parallel capacitance is given in equation (2.19).

The series resistance included the resistances of surface conductors in series with the resistances of the columns. The skin effect also should be considered for the calculation of the total resistance using equation (2.25). The equivalent π-model in Figure 2.1-b and the quality factor equation (2.28) were used for the evaluation of the inductor resolution.

The analytical model, the influence of the solenoid turns (n) on the Q-factor is illustrated in Figure 5.2. Also Figure 5.3 shows the result of the change in the height h and Figure 5.4 illustrates the effect of width w on the quality factor. Increasing the substrate thickness or height increases the quality factor, but the resonance frequency will decrease.

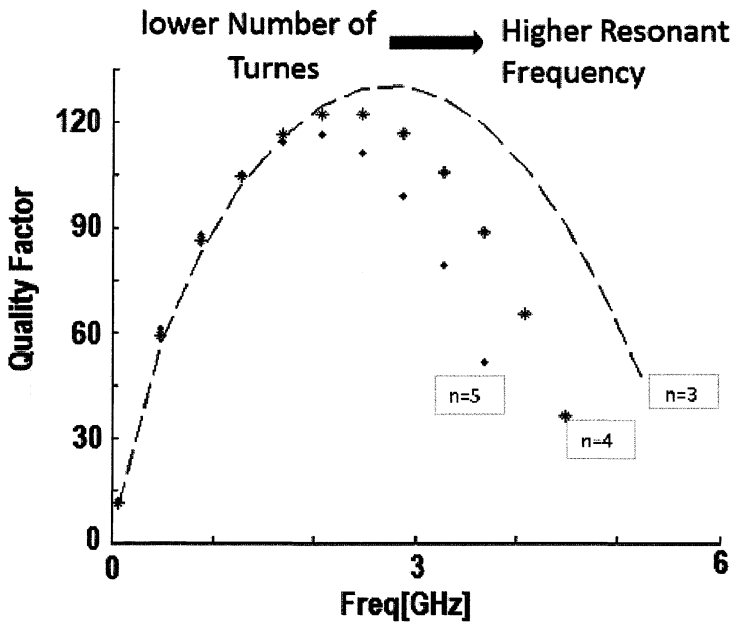

Figure 5.2. Quality factor and inductances of a = 1 mm, d = 0.5 mm, and w = 0.25 mm simulated micro-solenoids of 3 turns, 4 turns, and 5 turns.

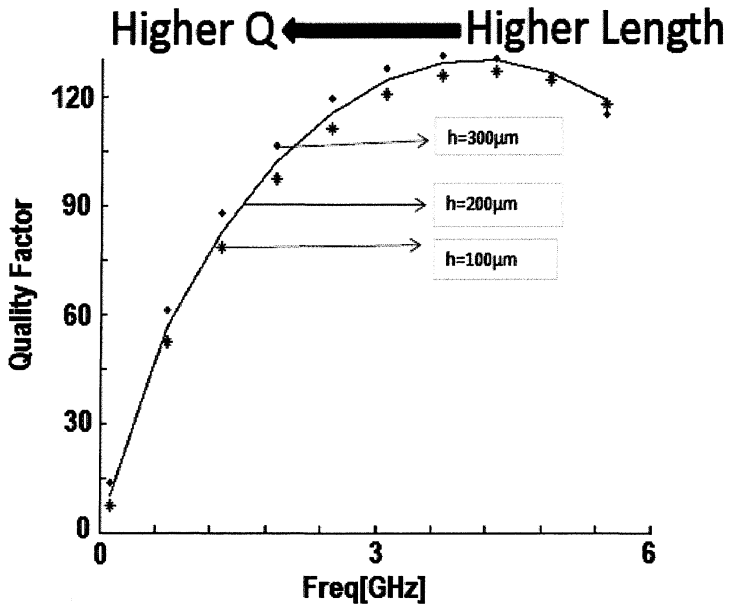

Figure 5.3. Quality factor and inductances of a = 1 mm, d = 0.5 mm, and w = 0.25 mm simulated micro-solenoids of h = 0.1 mm, h = 0.2 mm, and h = 0.3 mm.

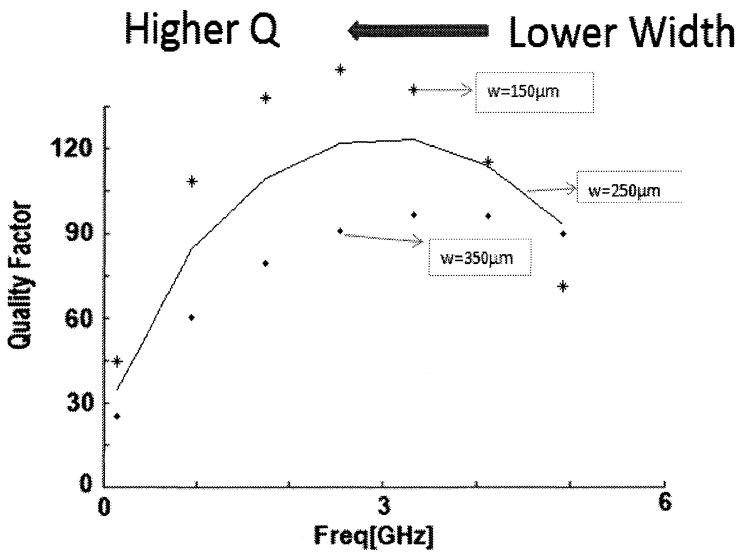

Figure 5.4 Quality factor and inductances of a = 1 mm, d = 0.5 mm, and w = 0.25 mm simulated micro-solenoids of w = 150 μm, w = 250 μm, and w = 350 μm.

5.3 Design and fabrication of Micro-solenoid

Based on the equation provided for the modeling, one can design a specific coil to match the Q-factor desired between the range of 2 GHz to 6 GHz. To achieve the highest resolution, this project is focused on the application RT/Duroid 5880 with the very low relative permittivity of 2.2. This makes the benefit of low loss through the entire thickness of the board. Making 3D structures in Duroid has different applications including high quality factor resonators, microstrip antennas, and interconnects [40], [68]. As such, the key to this design is to pattern the micro-solenoid through the Duroid to keep a highly uniform magnetic field through the coil. Fabrication of a high frequency embedded coil using a via also needs to keep a low resistivity on the surface and through

the inductors. It is also necessary to keep small size dimensions to increase the self resonance of the inductor.

In order to maintain the compatibility of the standard printed circuit board process, a drilling size of 125 μm radius was used. To match this requirement, the width of each conductor would be 250 μm and the minimum distance between two conductors was 250 μm. Copper or silver can be used as the cladding layers. Here copper cladding with silver immersion layer technology was used for the surfaces. A thin finishing layer of gold is added to avoid the oxide growth. The via was electroplated to make the columns. A two turn inductor is depicted in Figure 5.1, in which h is the height of the vias, w is the width of the surface conductors, a is the bottom layer conductor length, d is the pitch size, and b is the thickness of the cladding layer. The following variables were used to maximize the quality factor:

- Substrate thickness (h).
- Pitch size (b).
- Surface conductor length (a).
- Number of turns (n).
- Wire width (w).

To realize the effect of column height on the design, two Duroid thicknesses of 3.0 mm and 0.380 mm were provided. Finding the maximum value for Q, 32 different

sizes of solenoid have been designed, simulated and fabricated in 4 different models and 4 different number of turns for each model and 2 thicknesses.

One-port quality factor, Q_{11} (ω), is considered a measure for the performance of the coils in most literatures [25]. It has been defined as

$$Q_{Inductor} = \frac{\mathrm{Im}(Y_{11}^{-1})}{\mathrm{Re}(Y_{11}^{-1})} \tag{5.1}$$

Y_{11} can be calculated in port one, while the second port is short circuited. The inductance L is equal to

$$L = \frac{\mathrm{Im}[Y_{11}^{-1}]}{\omega} \tag{5.2}$$

Figure 5.5 shows the result of change in Q-factor by variation in number of turns using the electromagnetic simulation by Ansoft HFSS. It shows the lower the number of the turns, the higher the Q and self resonance frequency. Analysis of the inductance shows that for the frequencies lower than the self resonance, by increasing the number of the turns, a higher inductance would result. The influences of top conductor length, a, on the Q-factor is illustrated in Figure 5.6. Increasing length would decrease the quality factor. Also, Figure 5.7 shows that higher pitch sizes decrease the Q.

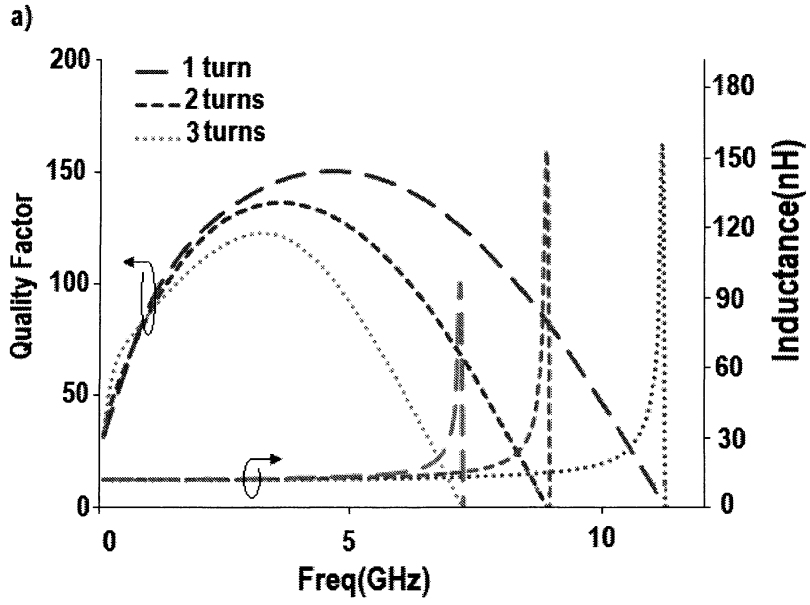

Figure 5.5 Quality factor and inductances of a = 1 mm, d = 0.5 mm, h = 0.38 mm, and w = 0.25 mm simulated micro-solenoids of 1 turn, 2 turns, and 3 turns.

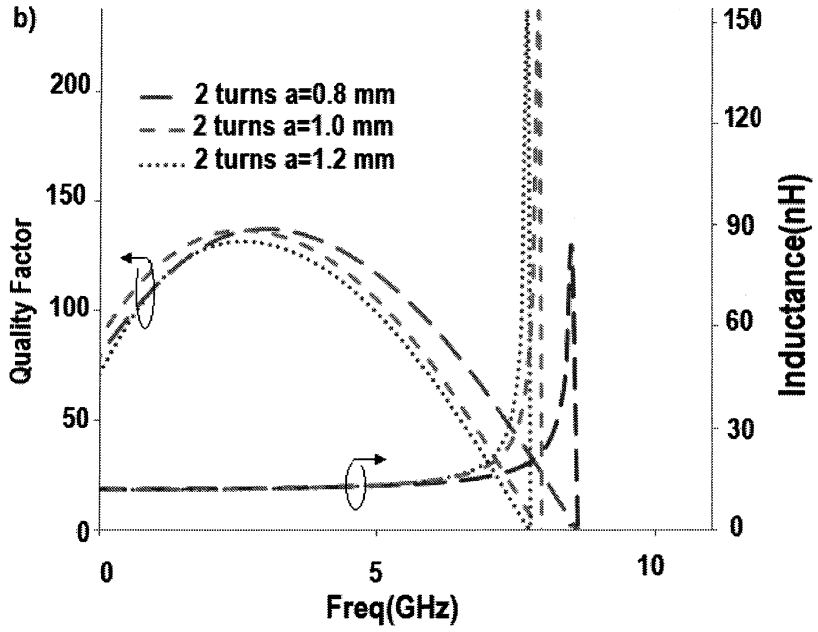

Figure 5.6 Quality factor and inductances of a = 1mm, d = 0.5 mm, h = 0.38 mm, and w = 0.25 mm simulated micro-solenoids of a = 0.8 mm, a = 1.0 mm, and a = 1.2 mm.

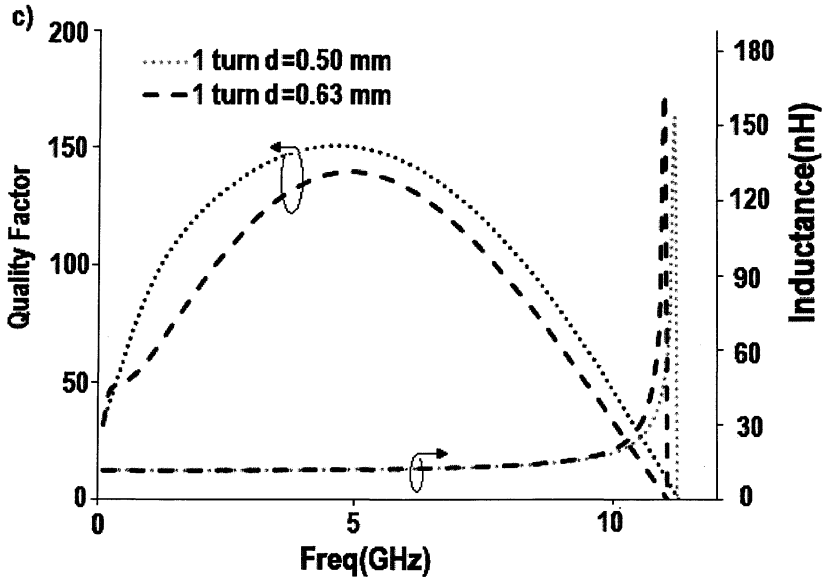

Figure 5.7 Quality factor and inductances of a = 1 mm, d = 0.5 mm, h = 0.38 mm, and w = 0.25 mm simulated micro-solenoids of d = 0.5 mm, and d = 0.63 mm.

EM-simulation results showed that any increase in the substrate thickness or height, increases the inductance but decreases the quality factor. Optimization of the results using the analytical modeling and electromagnetic simulation showed a 1 turn solenoid with 0.380 mm column height, 1 mm of the surface conductor length, and 0.250 mm pitch can provide the maximum Q-factor of 160.3. A copper conductivity of $4*10^7$ $S.m^{-1}$ was considered to make the simulation compatible with conductivity of our electroplated copper. A closed capture of the micro-solenoids is in Figure 5.8.

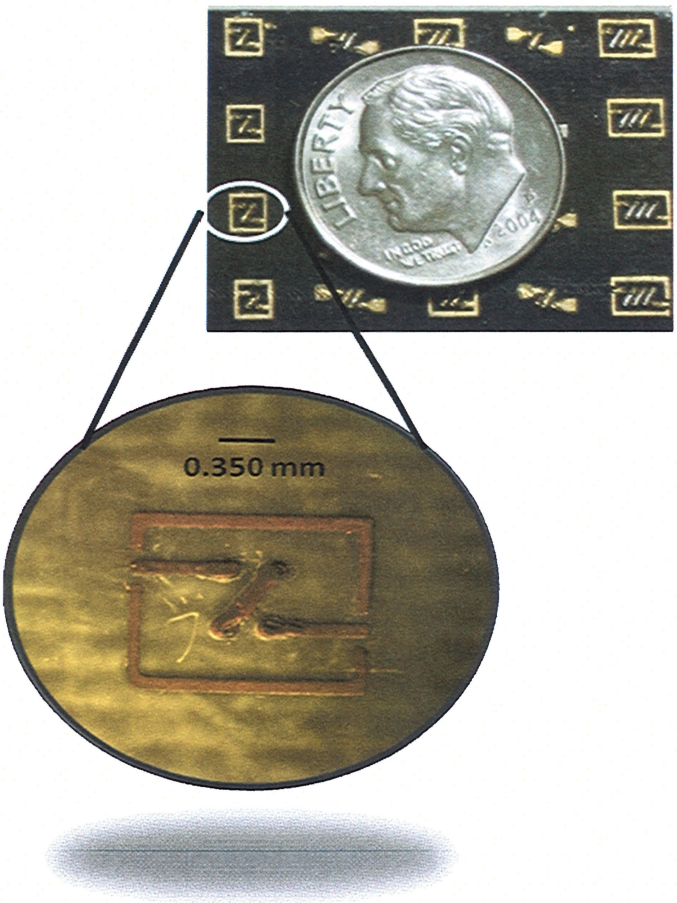

Figure 5.8 Top view of the micro-solenoids in their ground pad for a = 1 mm, w = 0.250 mm, and d = 0.500 mm.

5.4 Results and discussion

S-parameters of the fabricated resonators were measured using a HP8363 network analyzer and GSG Cascade Micro-tech probes. The short-open-load-thru (SOLT) calibration was done by an impedance standard substrate (ISS). The frequency span was measured using 6800 sampling points to increase the accuracy. Samples were put on a

striped Duroid board of 3.0 mm thick to decrease the ground capacitance during measurement. De-embedding of the pads was carried out after conversion of S-parameters to Y-parameters. The Y-parameters of a pad circuit without an inductor were subtracted from the same measured for a solenoid in the pad. Then the S-parameters were calculated using the new Y-parameters [11]. The Q-factors and inductances were evaluated using equation (5.1), and (5.2). Results of the measurement for one, two, and three turn inductors of model-1 including a = 1mm, d = 0.5 mm, h = 0.38 mm, and w = 0.25 mm are illustrated in Figure 5.9. The resulting measurement showed that the application of a low relative permittivity material like RT/Duroid 5880 did not degrade the quality factor due to the low dielectric permittivity. Furthermore the Duroid was a good supporting substrate to fabricate a reliable solenoid structure.

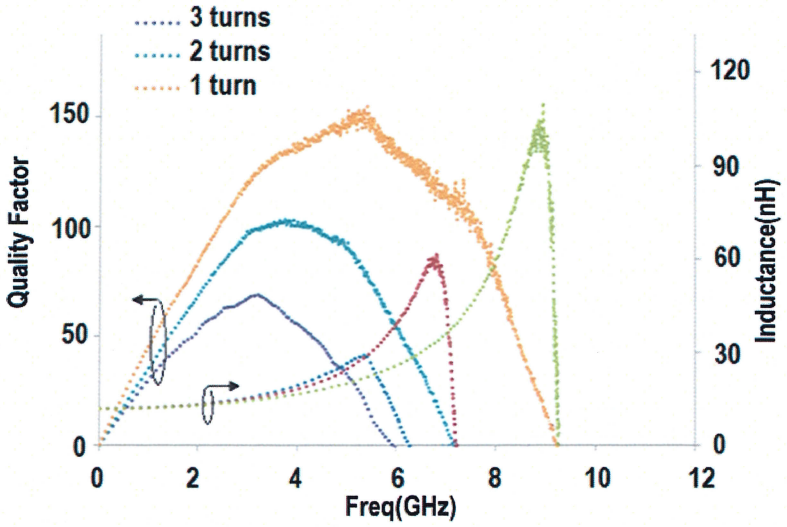

Figure 5.9 Measured quality factor and inductances of a = 1 mm, d = 0.5 mm, h = 0.38 mm, w = 0.25 mm simulated micro-solenoids of 1 turn, 2 turns, and 3 turns.

Optimization of the quality factor in the micro-solenoid resulted in closely spaced conductors that provide the highest coupling of the magnetic field. Besides that, the conductors should be wide enough to reduce the resistivity of the overall inductor. To show the compatibility of the measurement with the analytical modeling and EM-simulation, all three results for the one turn inductor are depicted in Figure 5.10 together. The measured sample in Figure 5.6 shows a quality factor of 160.3 for a 1 turn solenoid with 0.380 mm column height and 1 mm of the surface conductor length of 0.250 mm pitch size. The results of the measurement for one, two, and three turn inductors in two different thicknesses were used for evaluation of the circuit model components and are depicted in Table 5.1.

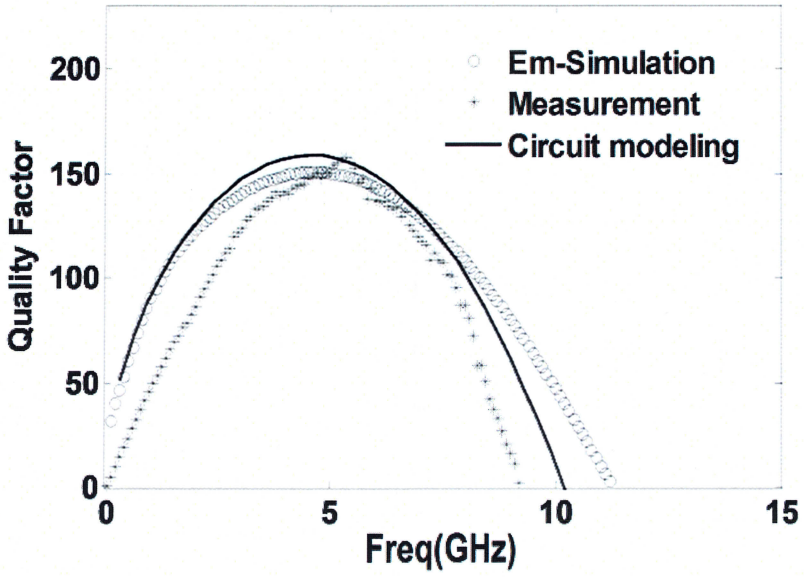

Figure 5.10 The results of measurement, EM-simulation, and analytical modeling of a single turn micro-solenoid inductor with a = 1 mm, w = 0.250 mm, h = 0.380 mm, and d = 0.500 mm are plotted together.

Table 5.1 The circuit parameter values for one, two, and three turns micro-solenoid inductors of model-1in two different thicknesses.

Turns	Height(h) (mm)	L_s (nH)	C_s (fF)	R_s (Ω)	F_{res} (GHz)	Q_{max}
1	0.380	3.5	84.0	0.19	9.26	160.3
2	0.380	4.5	90.1	0.28	7.91	104.0
3	0.380	5.9	115.6	0.35	6.48	68.9
1	3.010	9.8	164.9	0.21	4.21	122.1

The major restriction of increasing quality factor in the current designed Micro-inductor was the resistivity of the electroplated copper which was higher than the bulk copper and it degraded the quality factor. If a resistivity of close to bulk metal would be achieved in the electroplated vias, then quality factors higher than 200 can be obtained. Figure 5.11 illustrates the simulated and measured quality factor value for a thick one turn Micro-inductor. The measurement shows a lower quality factor due to higher resistivity in thick sample. Any improvement in the electroplating can result in a future enhancement in the quality factor of these micro-solenoids. A picture of the Micro-solenoid samples on a thick substrate is given in Figure 5.12.

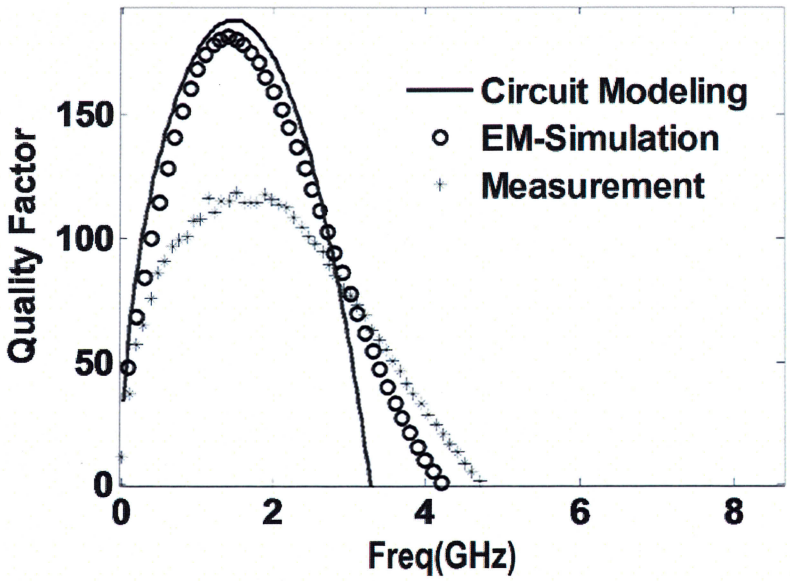

Figure 5.11 Measurement of a one turn 3.01 mm thick substrate micro-solenoid, EM-simulation, and analytical modeling with a = 1 mm, w = 0.250 mm, h = 0.380 mm, and d = 0.500 mm are plotted together.

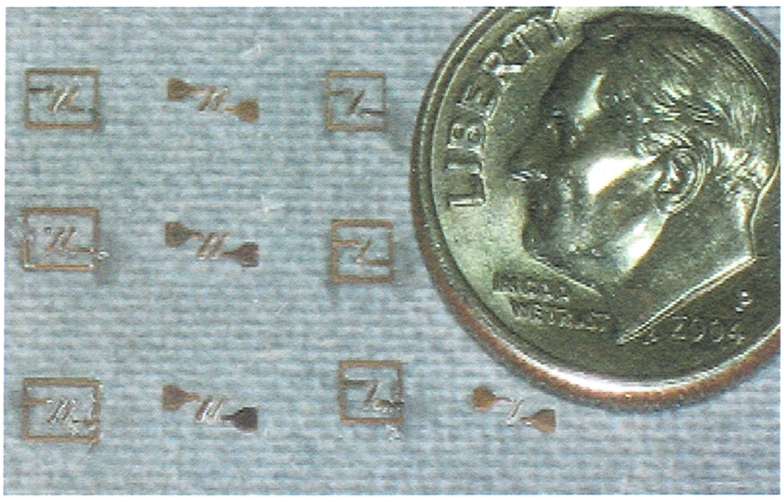

Figure 5.12 Fabricated samples on a thick substrate.

The device presented in this work also benefits from a commercial thickness for the board, higher frequency for the maximum Q, and easier monolithic fabrication. These advantages make the resulting micro-solenoid a good candidate for the miniaturization of the commercial Off-chip inductors. For example, if this research compared to the micro-spirals on the alumina substrate, helical resonators, and micro-coils using SOP structures not only benefit from higher quality factor but also have a commercial production method that can be realized [69], [61].

In contrast to the toroidal inductors reported by Philips and Settaluri with microstrip or stripline, the current results show the monolithic structures decrease the capacitive effects of a close grounding layer and increase the self resonance frequency of inductors.

CHAPTER 6

FABRICATION OF MICROWAVE RESONATOR USING THRU-HOLE VIAS AND EMBEDDED CAPACITOR

Resonators are key components in RF-circuits for the fabrication of filters and oscillators. Making on-chip resonators is costly and suffers from low Q-factors. To make high quality factor resonators, the new embedded Micro-solenoid introduced in Chapter 5 was used to make resonators in a Duroid substrate. The resonator includes a two turn inductor series with an embedded capacitor. The series capacitance was introduced in the via to move the poles toward higher frequencies. This provides significant enhancement in the quality factors, and it was realized using pole transfer. Furthermore, the resonator can be batch fabricated using conventional circuit board techniques.

This chapter presents the design, simulation, and fabrication of a novel high quality factor off-chip resonator using solenoid inductors. First the analytical design was investigated using both a lumped circuit model and electromagnetic (EM) simulation. Improvement of the quality factor was studied using the resonator dimension. Then the fabrication of device and measurement of the Z-parameters and S-parameters are covered. Finally in the discussion part, the simulation results, analytical model, and measurements were compared and a close match was realized.

6.1 Micro-resonators

As previously stated, wide demand for wireless communication has increased the requirement for high performance resonators and filters. While traditional solenoids are commonly used in the megahertz frequency range due to their high inductance and low parasitic capacitance, they cannot maintain their performance characteristics above a few gigahertz (GHz). This performance degradation is due to the skin and proximity effects that cause the resistance to increase and the inductance to decrease in higher frequencies. Thus the parasitic capacitance becomes a dominant factor in the overall design. Although there has been some improvement in the performance using the fabrication techniques for On-chip solenoid and spiral resonators, they cannot provide quality factors over 100. To overcome this limitation Off-chip resonators are currently developed using several of different techniques such as electromagnetic band gap (EBG) structures, low dielectric substrates, and low temperature co-fired ceramic (LTCC) multilayer circuits [69] to achieve Q factors up to 300. Cavity devices provide higher quality factors but suffer from large structural designs and complex fabrication process.

The new high quality factor Micro-solenoid explained in the previous chapter was considered a good candidate for the fabrication Micro-resonators. A combined approach was investigated using both inductive and capacitive cavity resonance to increase the resonator frequency into the 10s of GHz at quality factors over 300, while further reducing the size, and allowing for a low cost batch fabrication procedure. The new resonator consists of a micro-solenoid fabricated using vias in a printed circuit board.

One of the vias is separated into two single pieces using a small dielectric gap and provided two separate solenoid turns. An illustration of the new resonator is presented in Figure 6.1 for the one turn resonator. Each of these new single solenoid turns receives a fraction of the inductance based on the location of the dielectric gap. While the turn to turn capacitance for each side remains high because of its parallel capacitive contribution to the adjacent turn from the nearby micro-solenoid. On the other hand, by moving the dielectric gap along the via, the value of these new inductances and capacitances can be changed. As a result of that, the related pole-zero values in the equivalent impedance of the resonator is able to be changed. Pole-zero transfer was used to increase the performance of resonators in the previous applications [70]. It is utilized to maximize the quality factor in this chapter. To make the analytical model, a double π-circuit is investigated in the next part of this chapter.

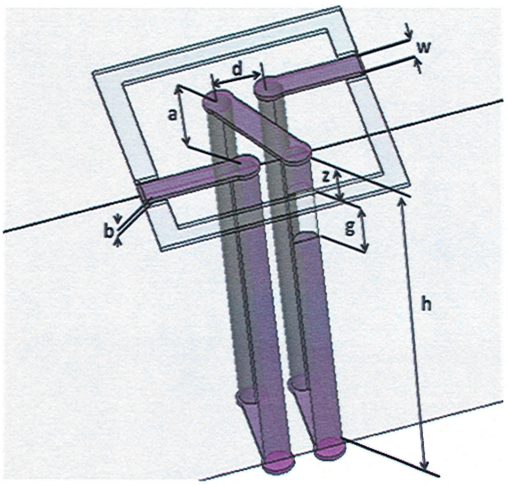

Figure 6.1 Schematic diagram of one turn resonator in Duroid substrate.

6.2 Analytical Modeling

To provide a theoretical model for the double zero double pole resonator, a comprehensive circuit description was considered. This methodology provided a total circuit using the device parameters. The suggested circuit model was justified by the same methodology introduced by Grandi et al. for evaluation of the stray capacitance in solenoids [15], [39]. The equivalent circuit model of the resonator is in Figure 6.2. The single and double π-model of microfabricated spiral and solenoid inductors and resonators have been extensively studied in the literature to evaluate the resonator components [19], [7]. Again the GreenHouse-Grover method was used to find the self inductance of each segment and also the mutual inductance between them [47], [49].

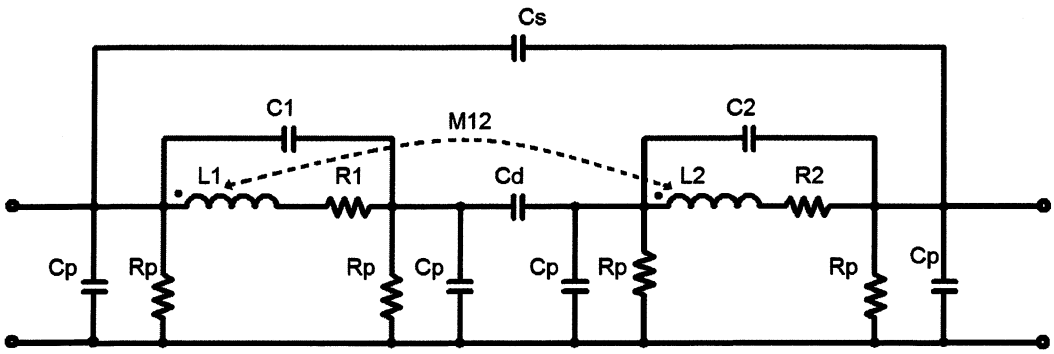

Figure 6.2 Schematic circuit of a double-zero double-pole resonator.

The contributed inductances were added to evaluate the overall inductance. Also, capacitances of terminals C_s, stray C_1 and C_2 , parallel C_p, and series in via C_d made the capacitive components of the model.

Resistance of the device consisted of series conductor resistances with the consideration of skin effect in high frequencies. After modeling of the circuit using components, the total circuit model would be reviewed using the zero and pole positions. The series capacitance was accommodated to divide the circuit into two circuits of the same structure in a single turn circuit. It also functioned as a pole added to the frequency response characteristic.

6.2.1 Inductances

The related equations for calculation of inductances were covered in Chapter Two equations (2.1) to (2.8). The inductance of partially filled segments in via would be evaluated by considering the filled area of the column for each side. Self inductances of L_1 and L_2 are evaluated by this method and the mutual inductance between the two individual inductances of the resonator is calculated using (2.5), and it is illustrated as M_{12} in Figure 6.2. In this circuit a large air gap between the resonators and ground made the parallel impedance large enough to make the current in series branches almost equal.

6.2.2 Capacitances

Based on the position of the segments, capacitances are defined across air or the Duroid substrate gaps with the relative dielectric constant, ε_r, of 2.2. Stray capacitances are C_1 and C_2; also the terminal capacitance is C_s between the input and output terminals. These capacitances are depicted in Figure 6.2. Parallel capacitance Cp is between segment and ground, and capacitance C_d was made using a dielectric layer between two conductors in the via.

Series capacitances located between the segments from the first terminal to the second depended on the cross section, distance, and the dielectric constant between the segments. In the calculation of C_s for the solenoid, the capacitance between all adjacent segments was considered to offer a close approach for the device value. Equation (6.1) was used for evaluation of terminal capacitance.

$$C_s \cong \varepsilon_0 \frac{\left[(n_1-1)\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}+2w+n_2 a\right]b}{(d-w)} + \varepsilon_r\varepsilon_0 \frac{2n_1 w\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}}{\left[h^2+(0.5d)^2\right]^{\frac{1}{2}}} + \varepsilon_r\varepsilon_0 \frac{(2n_3+1)hw}{\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}} + \varepsilon_r\varepsilon_0 \frac{0.5n_3 wh}{(d-w)} \tag{6.1}$$

The stray capacitances of C_1 and C_2 are formulated as follows:

$$C_1 \cong \varepsilon_0 \frac{\left[\left(n_1-1\right)\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}+2w+\left(n_2-1\right)a\right]b}{(d-w)}+\varepsilon_r\varepsilon_0\frac{n_1 w\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}}{\left[h^2+(0.5d)^2\right]^{\frac{1}{2}}} \qquad (6.2)$$

$$+\varepsilon_r\varepsilon_0\frac{(2n_3+1)hw}{\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}}+\varepsilon_r\varepsilon_0\frac{0.5(n_3-0.5)wh}{(d-w)}$$

$$C_2 \cong \varepsilon_r\varepsilon_0\frac{n_1 w\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}}{\left[h^2(0.5d)^2\right]^{\frac{1}{2}}}+\varepsilon_r\varepsilon_0\frac{(0.5n_3-0.5)hw}{\left[a^2+(0.5d)^2\right]^{\frac{1}{2}}}+\varepsilon_r\varepsilon_0\frac{(0.5n_3-0.5)wh}{(d-w)} \qquad (6.3)$$

where n_1 is the number of top layer conductors, n_2 the number of bottom layer conductors and n_3 is the number of via associated with the resonator in this model. The resonator dimensions are illustrated in Figure 6.1. Due to the close voltage value in the parallel vias of the same turn, the contribution of the capacitance made between these vias was not considered for the evaluation of total capacitance.

In a single turn model, the value of n_3 depends on the position of dielectric in the via and it will be substituted by n' for the first inductor circuit including the top surface segment.

$$n' = n_S + 1 + z/h \qquad (6.4)$$

And, it will be n'' for the second inductor circuit including the bottom side surface segment:

$$n'' = n_S + [1 - (z+g)/h] \quad , \tag{6.5}$$

where the value of n_s will be equal to one for a single turn model. Also, each segment makes a capacitance to the ground. They made parallel capacitive features of the two port network (C_p). It consisted of the lower segment capacitances of C_L and upper segment capacitances of C_U. The relative permittivity for ϵ has been considered as ϵ_0 due to the large distance between the resonator and ground. The equivalent value for C_p is in equation (2.19).

The series capacitance in the via is formulated below using two circular conductors of the copper column and the dielectric of thickness g between them. It is given by

$$C_d = \frac{\varepsilon_0 \pi \left(\frac{w}{2}\right)^2}{g} \quad . \tag{6.6}$$

6.2.3 Resistances

The series resistance included the resistances of surface conductors in series with the resistances of the columns and is given in equation (6.7). The skin effect δ is considered for this calculation.

where μ and f are permeability of copper conductor and working frequency, respectively. The circuit parameters evaluated for different dielectric locations have been evaluated and illustrated in Table 6.1.

Table 6.1 The parameter values of the circuit for different dielectric locations on analytical modeling of double pole, double zero resonators.

	Location of the dielectric in z				
	0.035 mm	0.187 mm	0.375 mm	0.75 mm	1.50 mm
C_1(fF)	24.57	24.81	25.68	32.26	45.26
C_2(fF)	24.25	23.78	23.09	19.39	12.09
C_d(fF)	0.67	0.67	0.67	0.67	0.67
L_1(nH)	7.35	7.42	7.54	7.84	8.53
L_2(nH)	6.73	6.57	6.37	5.98	5.24
R_1@1GHz(Ω)	0.176	0.179	0.181	0.188	0.201
R_2@1GHz(Ω)	0.147	0.145	0.141	0.135	0.122

6.3 Circuit model

In the double π-circuit model, two parallel LC tank circuits are introduced as a series branch of the two port network. These LC tanks are illustrated in Figure 6.2. The transfer function of the series branch is derived with the following characteristic matrix:

$$\begin{bmatrix} \frac{1}{j\omega C_1} + R_1 + j\omega L_1 & j\omega M_0 & \frac{-1}{j\omega C_1} \\ j\omega M_0 & \frac{1}{j\omega C_2} + R_1 + j\omega L_1 & \frac{-1}{j\omega C_2} \\ \frac{-1}{j\omega C_1} & \frac{-1}{j\omega C_2} & \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + \frac{1}{j\omega C_d} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad . \quad (6.8)$$

Using equation (6.8) the equivalent impedance of the series branch was evaluated. Figure 6.3 shows the equivalent impedance of a one turn resonator for the conductor length of 1 mm, pitch size 0.250 mm, and height 0.380 mm. This plot shows two resonance peaks in the impedance value. In other words, the model has two complex conjugate poles that can be altered by changing the location of the dielectric gap. Resonance frequencies of the circuit model were simulated by Matlab using the Z_{21} parameter. The change in the resonance frequencies for five different values of dielectric gap locations of z = 0.200 mm, 0.225 mm, and 0.375 mm are depicted in Figure 6.3. The most common definitions for quality factor are given in equation (1.1) and the quality factor of resonator can be evaluated using that [71], [5, equation (5)]

$$Q_{resonator} = \frac{\omega_0}{\Delta\omega_{3dB}} \quad .$$

$$Q_{resonator} = \frac{\omega_0}{\Delta\omega_{3dB}}$$

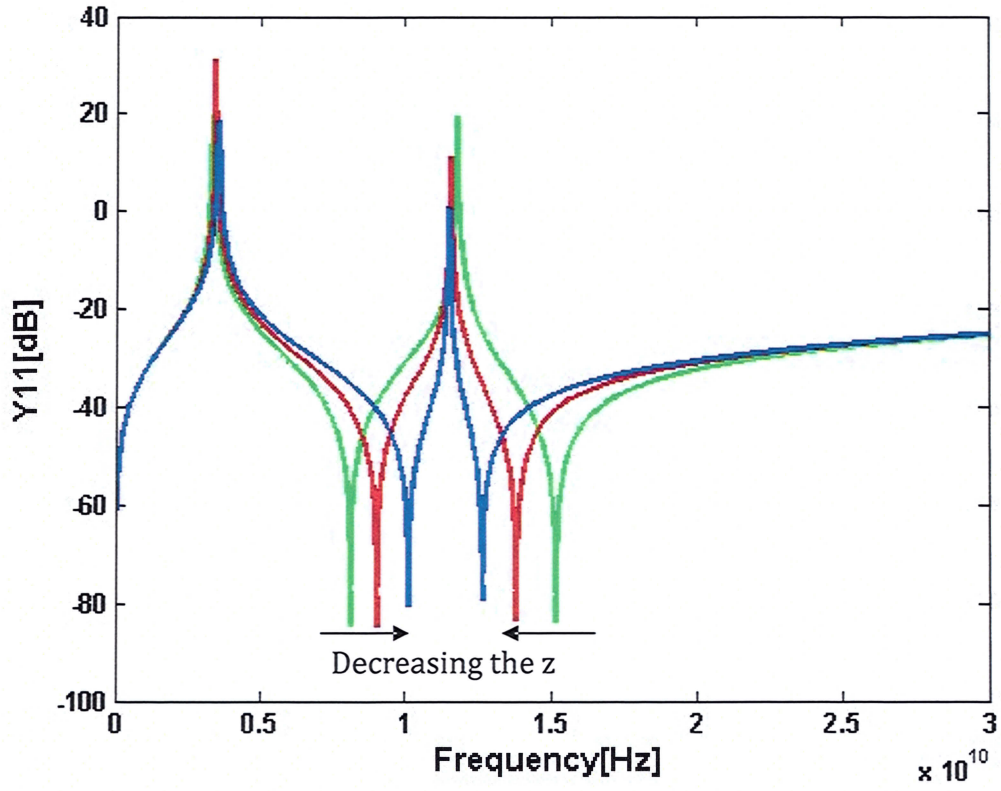

Figure 6.3 The change in the resonance frequencies for three different values of dielectric gap locations of a) green line z = 0.200 mm, b) red line 0.225 mm, and c) blue line 0.375 mm.

Any pole close to the imaginary axis would make a local maximum in the transfer function, and the pole frequency is considered as a resonance frequency [72]. This happens due the fast change in the phase value of the overall function. Figure 6.4 illustrates that when the frequency passes near the first pole in this circuit, it makes the highest change in the phase variation, and the phase angle needs to change from $-\theta_1$ to θ_2.

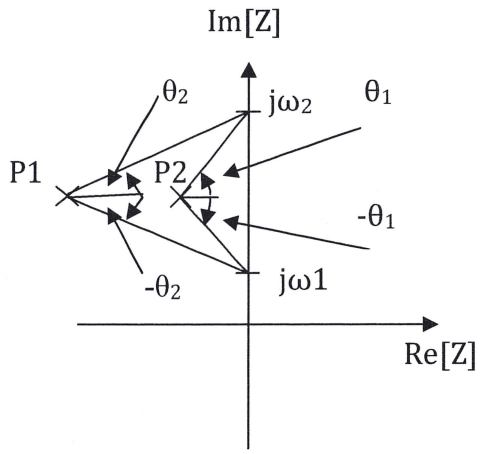

Figure 6.4 Variation of the phase angle near the pole close to imaginary axes shows more phase change as the frequency moves from ω_1 to ω_2.

The other poles also make a local change in the phase value, but they are under the influence of the previous poles and they are not close to the imaginary axes; therefore, they provide a lower quality factor as frequency moves into higher values. Evaluation of the quality factor using equation (6.9) is independent of application, and it has been used for the extraction of the Q.

Analytical modeling of the circuit in Figure 6.2 using equation (6.8) showed that the circuit had five poles and four zeros. One of the poles was in the origin and it was neglected due to its very low effect on the dominant pole. Therefore one must consider the other zeros and poles. By moving the capacitance dielectric along the column, the location of poles and zeros would be changed. The values of poles and zeros for different

dielectric locations are illustrated in Figure 6.5. In Figure 6.5, the change in the distance between poles is depicted as the dielectric goes to higher z values.

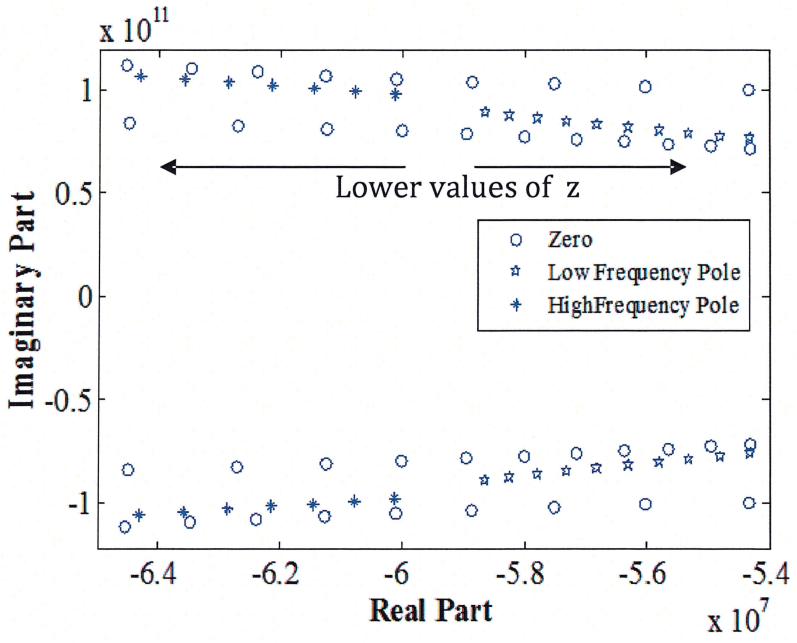

Figure 6.5 Location of non-zero poles and zeros for different values of z.

If the low frequency pole is near to zero, then the pole-zero cancelation could dampen the quality factor. When the dielectric moves to the middle of solenoid, or in the other words it possesses lower values of z, then the lower frequency pole moves to higher frequencies. It would also go to farther distances with respect to the imaginary axes. Even though it is farther, it remains the dominant pole until it is very close to the high frequency pole. Figure 6.6 is used to show the variation of the none-zero poles for the transfer function of the circuit.

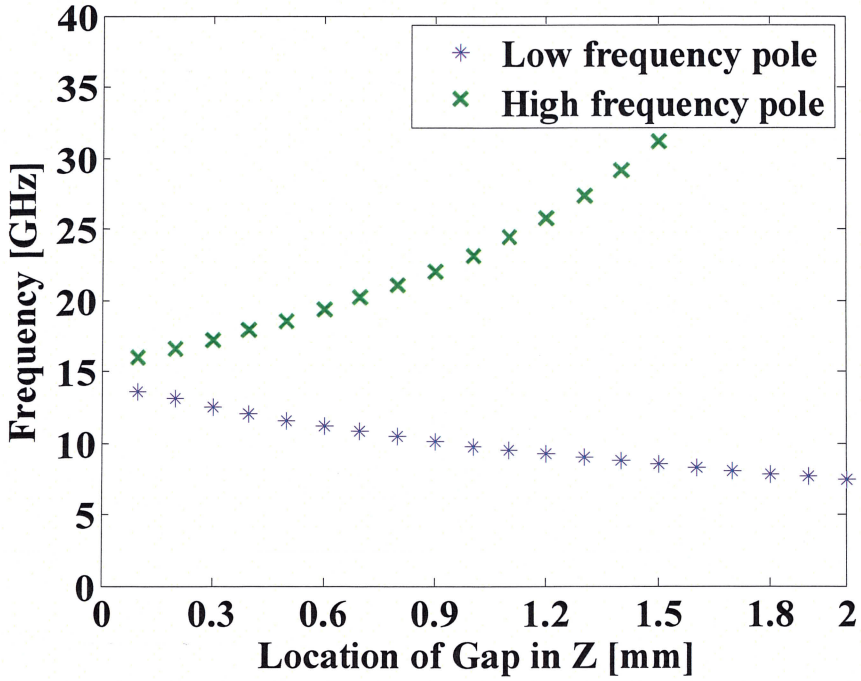

Figure 6.6 Schematic diagram of one turn resonator in Duroid substrate.

As is given in Figure 6.3 and confirmed by Figure 6.6, by changing the location of the dielectric gap, the poles will move close to each other. Making the poles close to each other degrades the quality factor. The frequency distance between the low frequency pole and the closest zero to it was named FD1 and is given by

$$\mathrm{FD1} = \frac{1}{2\pi}(\mathrm{Im}\,aginary[low\_frequency\_pole] - \mathrm{Im}\,aginary[low\_frequency\_zero]) \quad . \tag{6.10}$$

It is illustrated in Figure 6.7 that the low frequency pole could go far from the nearest zero to it whenever the dielectric reached lower z values.

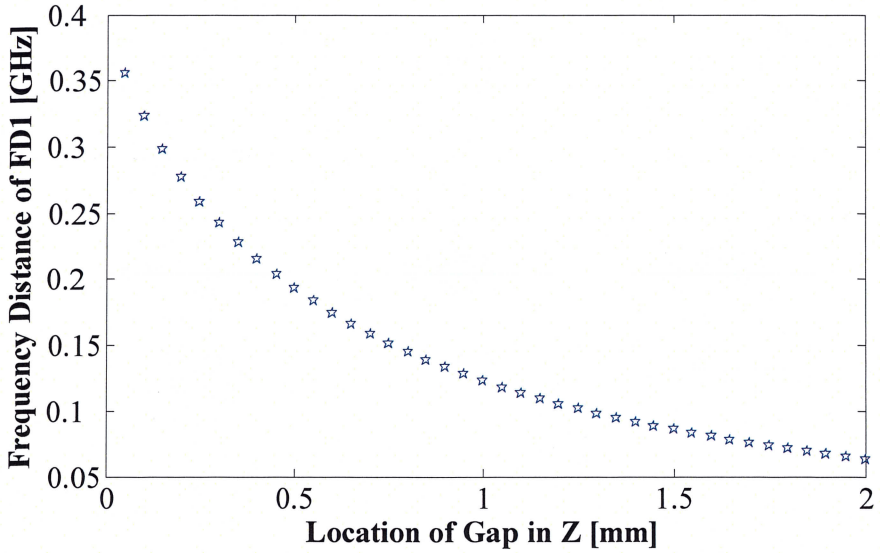

Figure 6.7 The change in frequency distance between low frequency pole and the nearst zero to it (FD1) versus the location of dielectric in the column (z).

Getting far from the nearest zero would improve the quality factor until the dominant pole (low frequency pole) became close to the second pole. This was supported by the experimental test result when the value of z became less than 0.3 mm.

6.4 Electromagnetic simulation of the resonator

Analytic modeling of the circuit has been investigated using a π-circuit model for the poles and zeros location in the equivalent impedance of the circuit [73]. Moving the dielectric gap along the inductor via transferred the dominant resonant pole far from the nearby poles and zeros. This provided the ability to optimize the resonant frequency and quality factor of the coil. Also the electromagnetic simulation of the device was performed with Ansoft-HFSS software. Results of the EM-simulation were compared directly with π models and showed negligible differences. Changing the device dimensions was investigated to find the maximum quality factor for the resonator. Figure 6.8 shows the S-parameters of the resonators for two different resonator heights of h = 3.175 mm and h = 2.54. Increases in the resonator height resulted in increases in the quality factor, but decreases in the resonance frequency. Also to increase the working frequency of the resonator, the lowest commercial drilling radius available was used. The diameter of the vias was considered 0.250 mm for the EM-simulations.

Figure 6.9 shows the S_{21} parameters for the one turn resonator dimensions of a = 0.250 mm, h = 3.175 mm, z = 0.375 mm, and two different widths of w = 0.500 mm and w = 0.250 mm. The result shows the lower width for the conductor will make the higher quality factor and the higher resonance frequency.

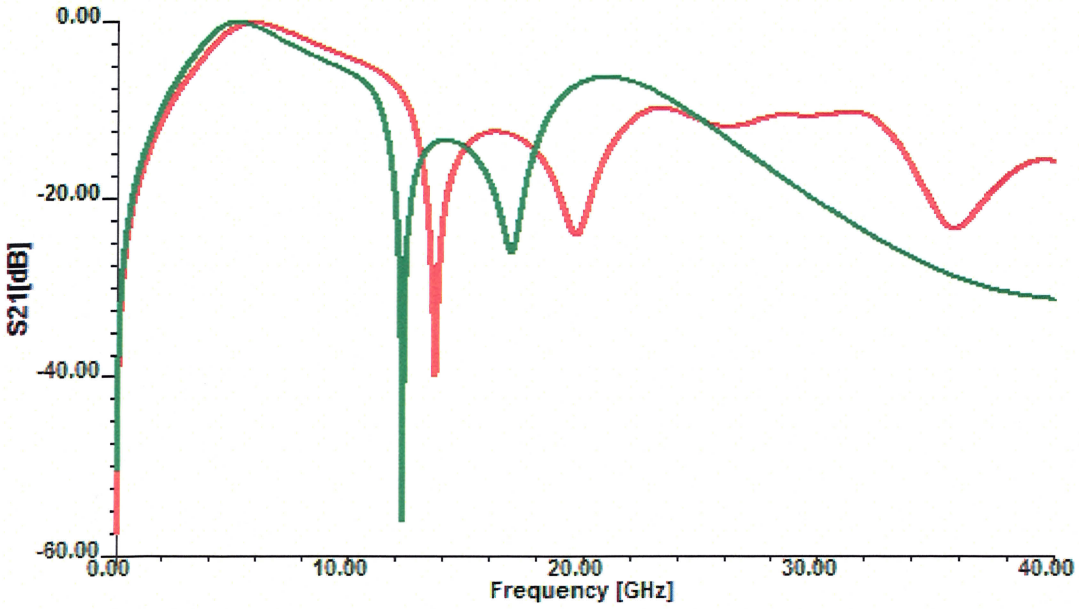

Figure 6.8 S_{21} parameters for a one turn resonator dimensions of a = 0.250 mm, w = 0.250 mm, z = 0.375 mm, and a) green line in h = 3.175 mm, b) red line in h = 2.54 mm.

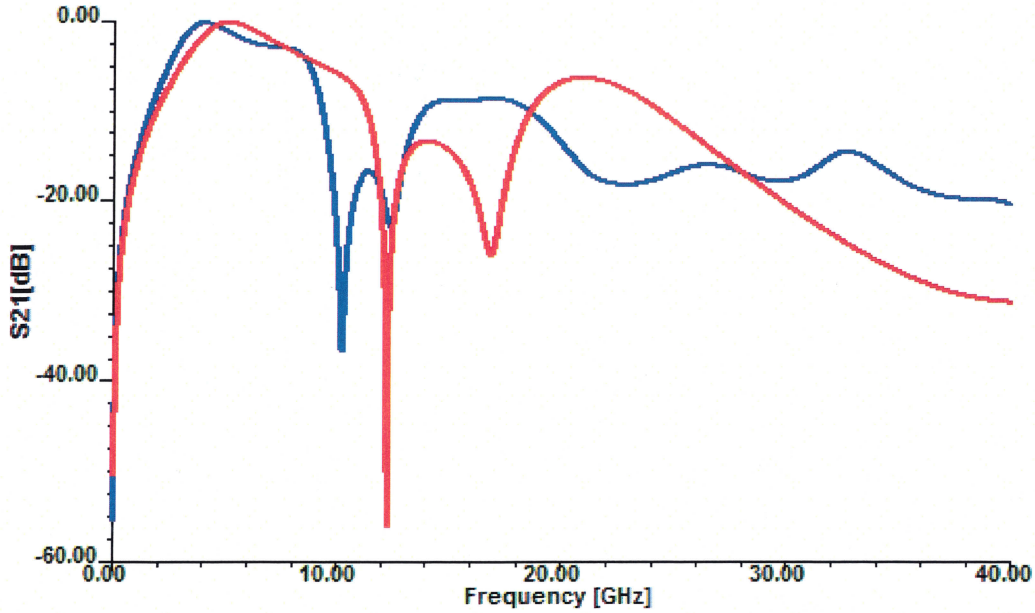

Figure 6.9 S_{21} parameters for a one turn resonator dimensions of a = 0.250 mm, h = 3.175 mm, z = 0.375 mm, and a) blue line in w = 0.500 mm, b) red line in w = 0.250 mm.

To investigate the effects of dielectric capacitance location, a capacitance is added to the top conductor as in Figure 6.10. The device dimensions for the one turn resonator are a = 0.250 mm, h = 3.175 mm, and w = 0.250 mm. The S_{21} parameters for the device with the capacitance on the top and the dielectric capacitance in z = 0.375 mm are given in Figure 6.11. The capacitance located on the top did not make the high quality factor resonance as it was predicted using Figure 6.3 for the two poles close to each other.

The scaling effect on the resonator was investigated by changing the total dimension. All dimensions are doubled and the results of S_{21} parameters are given in Figure 6.12 for the one turn resonator of a = 0.250 mm, h = 3.175 mm, w = 0.250 mm, and z = 0.375 mm and for a resonator of dimensions a = 0.500 mm, h = 6.350 mm, w = 0.500 mm, z = 0.760 mm.

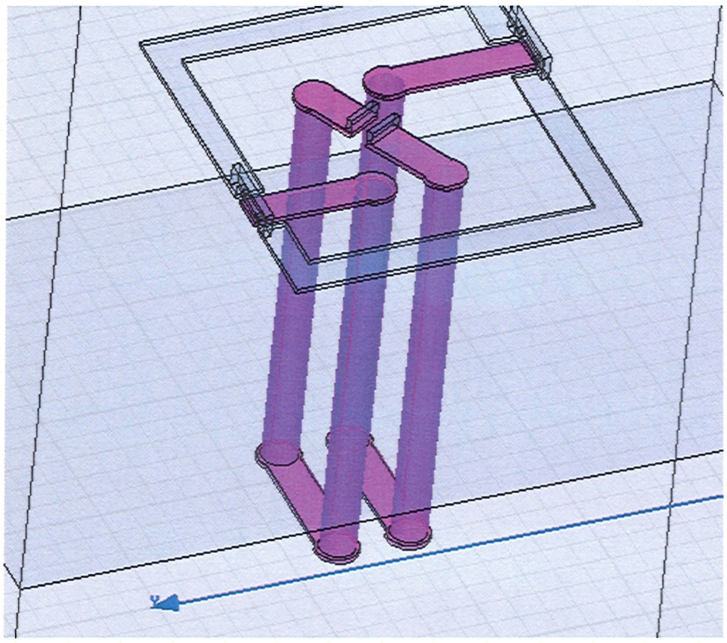

Figure 6.10 A schematic model of a one turn resonator with the capacitance C_d in the middle of the top surface conductor.

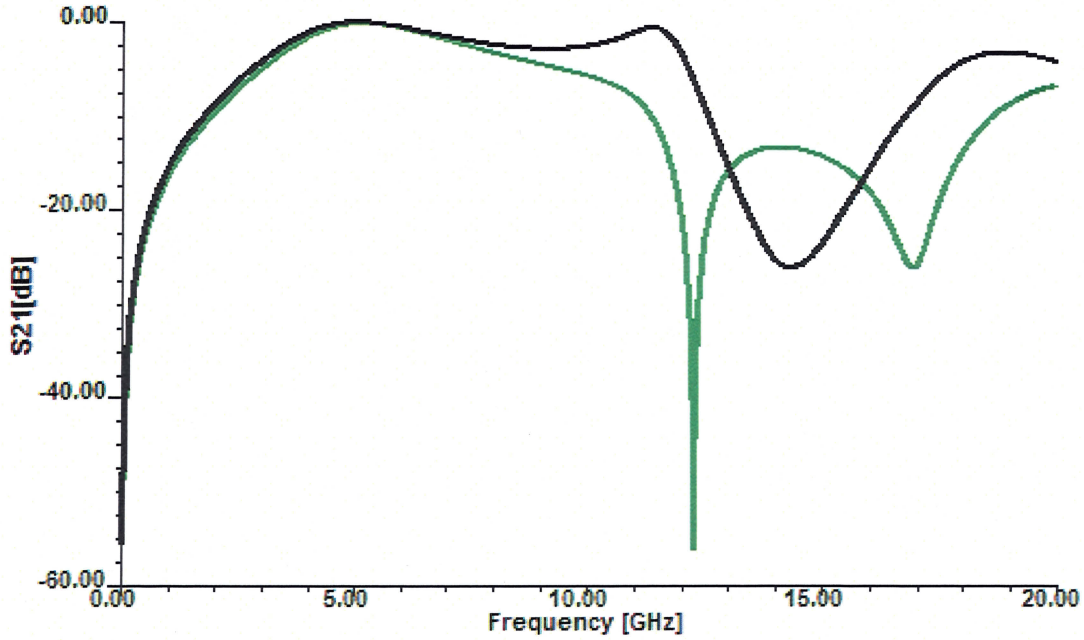

Figure 6.11 S_{21} parameters for a one turn resonator dimensions of a = 0.250 mm, h = 3.175 mm, w = 0.250 mm, and: a) green line z = 0.375 mm, b) black line z = 0.0 mm or the capacitor of C_d on the top.

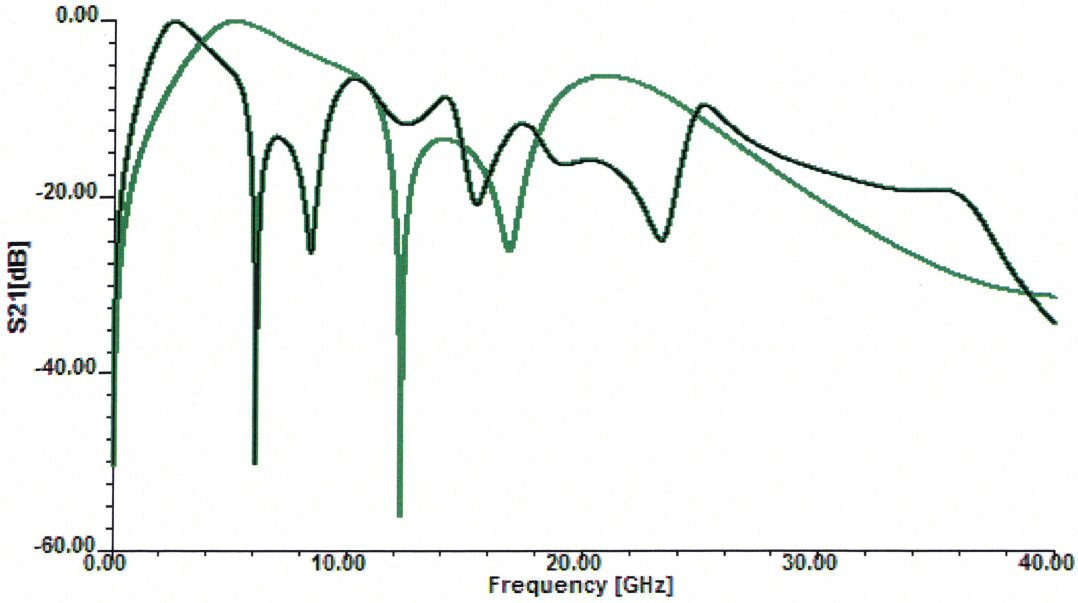

Figure 6.12 S_{21} parameters for the one turn resonator dimensions of: a) green line a = 0.250 mm, h = 3.175 mm, w = 0.250 mm, z = 0.375 mm, b) black line a = 0.500 mm, h = 6.350 mm, w = 0.500 mm, z = 0.760 mm.

To study the effect of turns number on the resonator, a three turn resonator with the dielectric capacitance located in the first column is given in Figure 6.13. The three turn resonator has the device dimensions of a = 0.250 mm, h = 3.01 mm, and w = 0.250 mm. The S_{21} parameters for the device with the three turn and dielectric capacitance in the first column and the same device with dielectric capacitance in the second column are given in Figure 6.14. The resonance frequencies of both resonators are decreased, and the quality factor is lower than a one turn resonator. As result of this decrease in quality factor, one can say the higher turns will not increase the quality factor.

Also, the quality factor of a two turn resonator inductor without dielectric gap is simulated in Figure 6.15. The resonance frequency is 7.5 GHz with a quality factor of 78. It shows lower resonance frequency and lower quality factor due to higher total inductance.

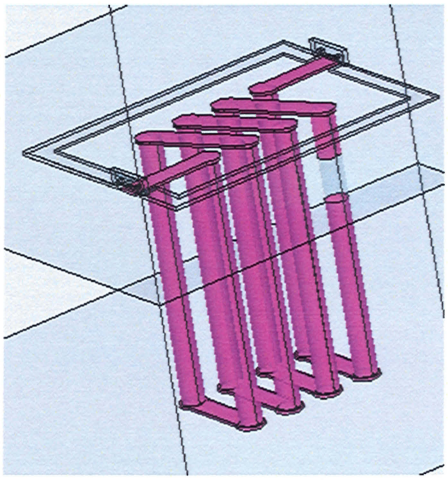

Figure 6.13 A schematic model of the three turn resonator with the capacitance C_d in the first column.

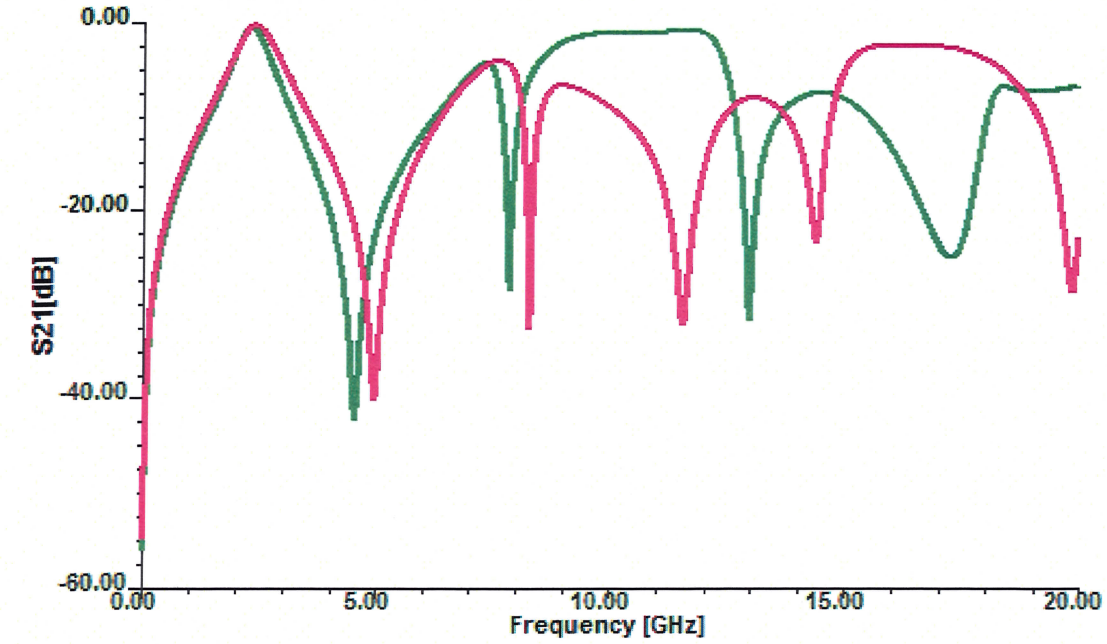

Figure 6.14 S_{21} parameters for the three turn resonator dimensions of a = 0.250 mm, h = 3.175 mm, and w = 0.250 mm, z = 0.375 mm with a) green line dielectric gap in the first column, and b) red line dielectric gap in second column.

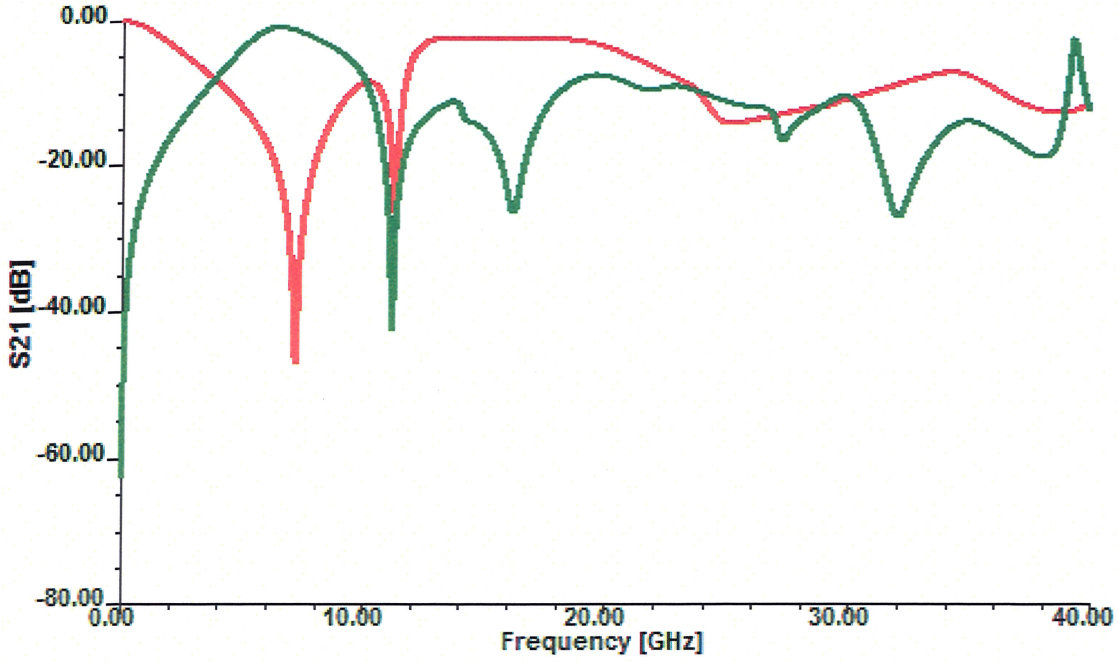

Figure 6.15 S_{21} parameters for the two turn resonator dimensions of a = 0.250 mm, h = 3.175 mm, and w = 0.250 mm with a) green line with dielectric gap, and b) red line without dielectric gap.

The change in the dimension shows that a one turn resonator with the thickness of the 3.01 mm gives the highest quality factor. If the location of the dielectric gap is changed along the via, the resonance frequency and the quality factor will change. The effects of dielectric location of z in the resonator are investigated in Figure 6.16 for dielectric gap locations in z = 1.5 mm, z = 0.75 mm, z = 0.375 mm, z = 0.187 mm, and z = 0.035 mm respectively.

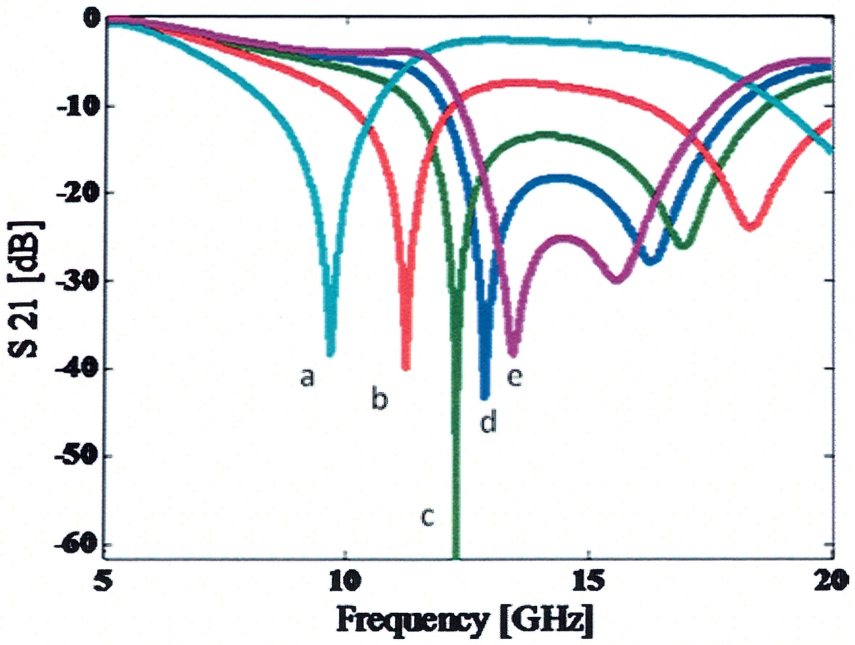

Figure 6.16 Simulated response of dual frequency resonators for different dielectric capacitor locations of z at a) 1.5mm, b) 0.75 mm, c) 0.375 mm, d) 0.187 mm, and e) 0.035 mm.

The Y_{11} parameter of the EM-simulations is given in Figure 6.17 for three different dielectric gap locations of z. Comparing the EM-simulation results in Figure 6.17 and the Y_{11} parameters evaluated by Matlab in Figure 6.3 shows the same variation in the resonance frequency. A close match between the circuit model results and EM-simulation confirms the analytical modeling of the resonator.

The simulations showed that the maximum quality factor was possible for a resonator of via height 3.08 mm, surface conductor length 1 mm, conductor width 0.250 mm, capacitor length 0.500 mm, and a capacitor location of 0.375 mm.

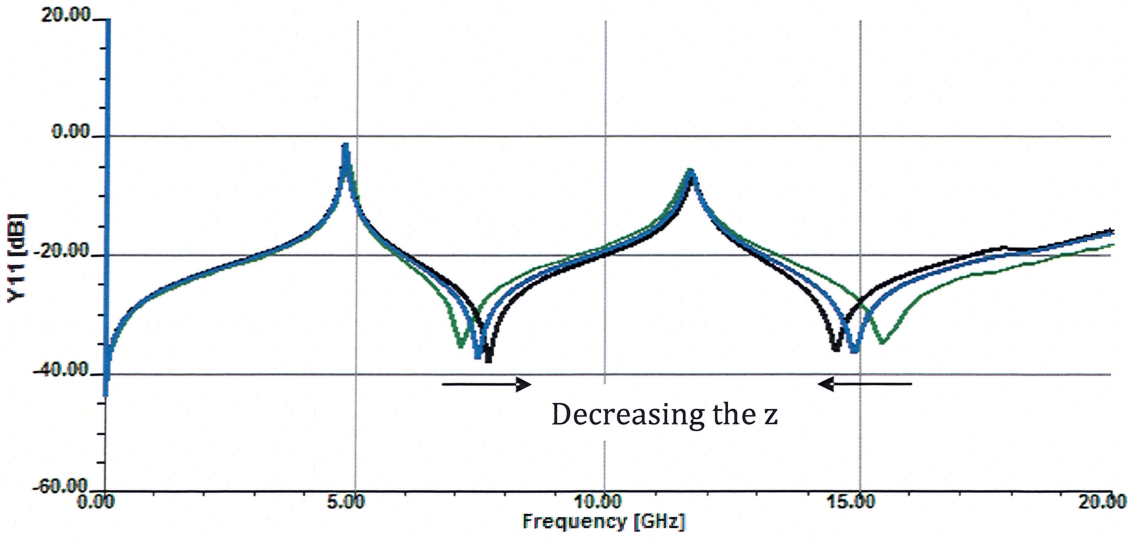

Figure 6.17 The Y_{11} parameter of the EM-simulations is given for the three different dielectric gap locations a) black in z = 0.1875 mm, b) blue in z = 0.375 mm, c) green in z = 0.75 mm.

6.5 Fabrication of the resonator

Fabrication of 3D structures in Duroid has different applications including microstrip antennas, interconnects, and cavity resonators [40]. Very low relative permittivity of 2.2 in RT/Duroid 5880 results in a high fringing field in microwave frequencies with lower loss in a electromagnetic field. To fabricate an efficient coil using a via in the microwave range, it is necessary to keep a low resistivity and small size dimensions. For the compatibility of the method with standard printed circuit board fabrication, a drilling size of 125 μm radius was used. As a result of that, the width of each conductor would be 250 μm and the distance between the two conductors made the pitch size 250 μm. Copper cladding of 35 μm followed by silver immersion layer technology was used for the surfaces. Vias were electroplated to make the columns. Previous experiments resulted in higher Q-factors for tall solenoids [34], so a Duroid substrate of 3.08 mm thick was used. Photolithography and gold sputtering followed by copper electroplating of the surface conductors made the top layer and the measurement pad. Figure 6.18-a to 6.18-f illustrates the generic steps for the fabrication and Figure 6.18-g shows the fabricated device.

6.6 Measurement and discussion of the resonator

Fabricated resonators were measured using a HP8363 network analyzer and GSG Cascade Micro-tech probes. The short-open-load-thru (SOLT) calibration was done by an impedance standard substrate (ISS) [74], [75]. De-embeding of the pads was carried out after conversion of S-parameters to Y-parameters.

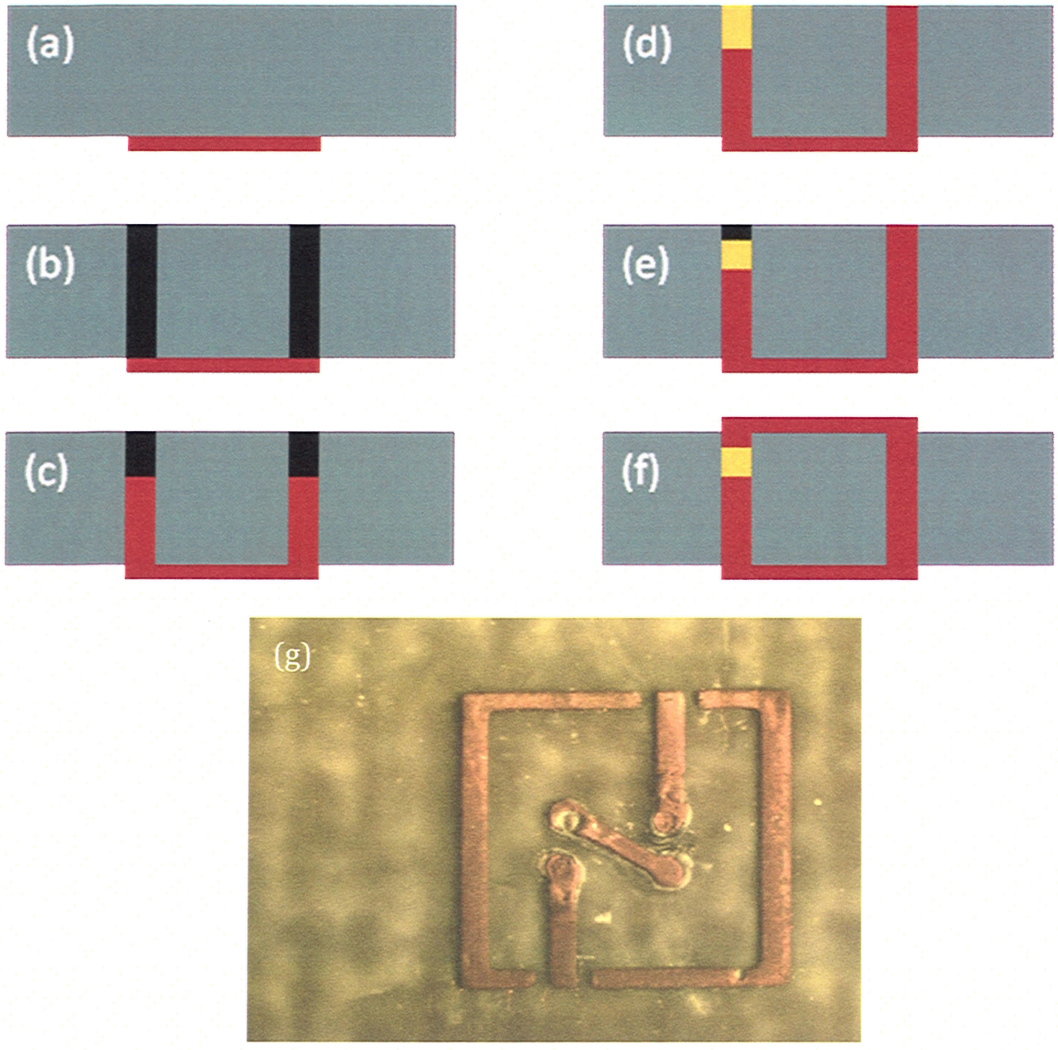

Figure 6.18 Generic proccessing steps for the fabrication of resonator include a) patterning of copper clad, b) Drilling the via, c) Electroplating in the via, d) Filling the dielectric with photoresist and electroplating the other via, e) Drilling, f) Sputering and electroplating of the top conductor, g) Close-up image of the fabricated single turn solenoid resonator.

The Y-parameters of an open pad were subtracted from the same measured parameters for a resonator in the pad. Then the S-parameters were calculated using the new Y-parameters. The results show that putting a series capacitor in the middle of an embedded solenoid divided the resonator with two complex conjugate poles into a resonator with four complex conjugate poles. The quality factor for five different dielectric locations using simulation and measurement is in Table 6.2.

Table 6.2 Frequency and quality factor of resonance poles for different dielectric locations in a double pole, double zero resonator.

		P_1	P_2
Z = 0.035 mm	f	13.41 GHz	15.6 GHz
	Q	60.95	18.35
Z = 0.187 mm	f	12.87 GHz	16.25 GHz
	Q	214	24.25
Z = 0.375 mm	f	12.27 GHz	16.89 GHz
	Q	480	25.59
Z = 0.75 mm	f	11.22 GHz	18.32 GHz
	Q	187	25.09
Z = 1.5 mm	f	9.65 GHz	17.25 GHz
	Q	120.62	6.43
Z = 0.375 mm Measurement	f	12.25 GHz	16.15 GHz
	Q	306	20.44

The capacitor size provides the minimum frequency in which the device starts to transfer the signal. Design concepts showed that fabrication of very thin dielectric layers of less than 0.4 mm prevented the solenoid from making double resonator circuits. The results illustrated that the resonance frequency would become near to double for this application in a double turn solenoid. The resonance frequency cannot be doubled in higher turns because it has more than one resonance frequency and as its first resonance would be suppressed the second resonance would be dominant. The modeling shows close agreement with the simulation in which a quality factor of 480 was approached in 12.27 GHz. The results show the sensitivity of the circuit to the position of its zeros and poles.

Figure 6.19-a illustrates the measured and simulated S_{21} of a one turn resonator. It shows that the first poles of simulation and measurement happen in the 12.27 GHz and 12.25 GHz respectively, which makes a close match between simulation and fabrication, while the second poles are in different frequencies. Measurement results showed a second pole in 16.15 GHz. It happened 740 MHz before the same pole in the simulation which was in 16.89 GHz. This could have happened due to any inaccurate drilling making a smaller dielectric size. The Unwanted increase in the z while decreasing g can lower the frequency of the second pole. This happens due to the rise in the values of L_2 and C_2. Evaluation of the Q-factor for the fabricated device is possible by equation (7.9) and can be done using Figure 6.19-b. Extraction of the quality factor using S_{21} results in a maximum quality factor of 306 in the 12.25 GHz for a two turn solenoid. This is lower than the value of 480 that was calculated in the simulation. The main reason is the

movement in the second pole toward the first pole in the measurement circuit, which reduces the quality factor of the dominant pole.

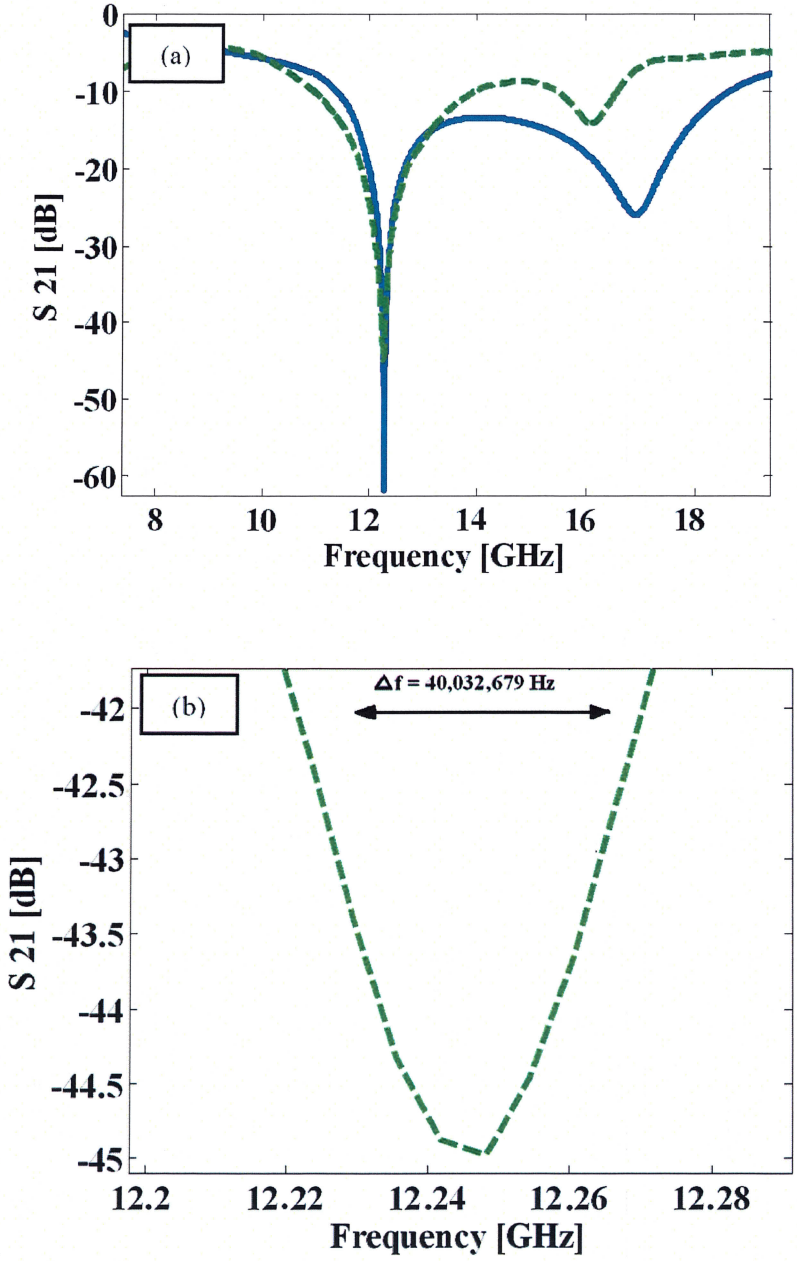

Figure 6.19 Measurement result (dashed line) and simulation data (solid line) of a one turn solenoid resonator with a capacitor at z = 0.375 mm is given in a, and the enlarged view of S_{21} measurement data for Q-factor illustration at resonance frequency is illustrated in b.

Indeed the sensitivity of the resonator was limited to the copper plating and attained higher values than that of bulk copper. The quality factor of a double pole resonator is very sensitive to the position of the poles with respect to each other. Figure 6.20 shows the measurement of the phase angle of S_{21} for three different samples of different dielectric gap locations (z) and the EM-simulation with z = 0.375 mm. The fast change in the phase angle shows the resonance frequency. The highest quality factor of 306 was measured in the 12.25 GHz. The result of this experiment shows how a high quality factor resonator can be designed using the poles close to the imaginary axis and far from each other. The highest Q-factor for both poles would be achieved when they are at least 5 GHz far from each other.

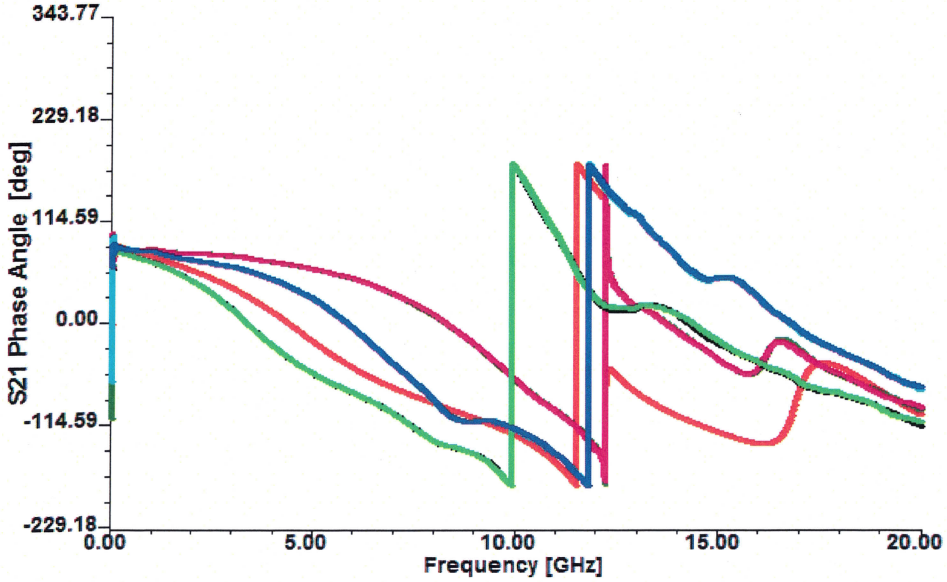

Figure 6.20 The phase angle of S21 parameter for a) red colored line is the EM-simulation for z = 0.375 mm, b) magenta colored line is the measurement sample for z = 0.375 mm, c) green color line is the measurement for a sample with z less than 0.375 mm, and d) blue color line is the measurement for a sample with z higher than 0.375 mm.

Tuning of the resonator has been previously reported by Zhang using the transmission of zeros to fabricate band pass filters [76]. In this paper, not only zero and pole transmission has been studied but also the resonator dimension and optimization of the quality factor by the resonator elements. Using a series capacitor added to an inductor circuit, a Micro-resonator structure was fabricated. A capacitor was made in the solenoid via and its location had influence on the poles and zero locations. The quality factor was optimized by the adjustment of the poles on the target locations.

This work presents a commercially manufacturable inductive resonator with a quality factor of 306 at a resonance frequency of 12.25 GHz, which is more than three times the quality factor reported by Melik for an On-Chip resonator at 15 GHz [19]. Also the current resonator made 3.75×10^{12} for the f.Q product, while the Rinaldi measured a maximum 1.7×10^{12} for Contour-Mode resonators [77].

Fabrication of such a narrow band microwave filter can increase the efficiency of high frequency circuits. This resonator captures 10 mm^2 of the printed circuit board. Compared to a ring resonator with 625 mm^2 captured area for the same working frequency, it is very small, and it can be easily fabricated near the integrated circuits using standard PCB fabrication.

CHAPTER 7

CONCLUSIONS AND FUTURE RESEARCH

This work introduced and developed a novel method for fabrication of the Micro-solenoids and Micro-resonators. This new method of design and fabrication will greatly enhance the miniaturization and resolution of the passive components. The new Micro-solenoids and Micro resonator have excellent quality factors and have high potential for the application in the front ends of the radios for wireless communication. The new devices were individually designed, optimized, and then fabricated.

7.1 Summary

Micro-solenoid: Design, simulation, and fabrication of novel off-chip micro-solenoids with high quality factors was presented. A low cost standard PCB production was used. S-parameters of the fabricated models were measured using a microwave probe station and the quality factor has been extracted. A maximum quality factor of 160.3 was recorded for a one turn solenoid. It shows close agreement with modeling. The results have a potential application in microwave circuits to enhance performance with a very high quality factor.

Micro-resonator: The new Micro-solenoid was used for design and fabrication of an off-chip resonator with a high quality factor. Transmission of the poles was used to optimize the resonator for a maximum quality factor. The agreement between analytical modeling and electromagnetic simulation proves the accuracy of this technique. The application of low cost standard PCB fabrication makes the technique available and easy to implement. This new design resulted in a resonator with a high quality factor of 306 at 12.25 GHz. It was fabricated and the S-parameters of the fabricated models were measured. The measurement and modeling are in close agreement for the dominant resonance frequency and with a small frequency shift for the second resonance frequency. Improvement in quality factor and resonance frequency made a high f.Q product. The results have potential applications in microwave circuits to increase their resonance frequency with a very high quality factor. It would also decrease the cost and complexity of fabrication compared to ON-chip inductors and resonators and MEMS structures.

7.2 Future work

The new passives introduced in this work are useful for RF applications. One approach is to improve and make new devices such as a Band Pass RF-filter, Matching Network, and Tunable-filters. The developed fabrication processes in this work are believed to be useful for providing new zeros and poles to the transfer characteristic function of the RF transmission line in a 3D fashion structure. This can miniaturize the device dimension and by moving the zeros and poles, the filtering features of the device

will be changed. For example a via is embedded close to the Micro-solenoid for providing a zero in the S_{21} parameter of the device. The result is a band-pass filter. The same methodology can be used for changing the bandwidth and insertion loss of the filter. An extension to the resonators fabricated using this method is to fabricate cascaded resonators to make a wide band notch-filter. This high quality factor resonator can also be used in active circuits for applications such as Phase Locked Loops (PLLs) and voltage controlled oscillators (VCOs).

The high Q in the feedback circuit of the oscillator decreases the phase noise in the out-put frequency. Another suggested extension is to fabricate a tunable resonator filter. This can be done by adding a varactor diode in parallel to the circuit. This diode can change the parallel capacitance of the total circuit and change the resonance frequency as well.

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