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Testing Metal-Ferroelectric-Semiconductor Field Effect Transistors

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TESTING METAL-FERROELECTRIC-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

ABSTRACT

In this project, the Metal-Ferroelectric-Semiconductor Field Effect Transistor is examined. First, the current characteristics are observed through the collection of data and the construction of hysteresis plots detailing the ferroelectric transistor's behavior. Next, we look at how the switching of the voltage at the gate of the ferroelectric transistor may affect the behavior as well and how the current through the transistor decays with time due to the molecules in the ferroelectric material moving up and down. Finally, in a simple amplifier setup the voltage across a variable load and the phase difference between the input and output are measured for different input frequencies, amplitudes, offsets, and polarizations on the transistor. The data from the experiments determining the effects of how long the input is kept active support the data from the amplifier, which state as a general trend increasing frequency and load resistance increase the voltage. However, in the case of increasing the load resistance, the current decreases, though at a lessened rate.

INTRODUCTION

For this project, several Metal-Ferroelectric-Semiconductor Field Effect Transistors were examined as stand alone elements and as components in a simple amplifier circuit. While in these test setups, the input frequency, input voltage, load resistance, and polarization vary according to our test plan, and we look at the effects of
these variations on the output of the ferroelectric transistor. These outputs are unique and different from the traditional Metal-Oxide-Semiconductor Field Effect Transistors in that the present output depends on past inputs as well as the present input. Since these interesting components are largely unstudied, yet sometimes used in a very narrow spectrum of applications, with more research it is believed that they can become an integral part in a diverse set of fields.

The unique characteristics of these ferroelectric transistors come from the use of ferroelectric material above the channel. Through this addition, a memory of past inputs is created by the polarization of the ferroelectric material, which affects the drain current during active operation and continues after the gate voltage has been removed. All of the transistors used in our experiments were manufactured with lead zirconate titanate (PZT) acting as the ferroelectric material. When applying a voltage on the gate, the zirconate titanate molecule at the center of the box of lead atoms can move up or down, thus creating a dipole. This dipole is then able to influence the channel of the transistor in the same manner as a small charge being placed at the gate. During active operation, if a positive voltage is applied to the gate, the ferroelectric material aligns to give a small negative charge on the gate. The effective charge at the gate can then be considered approximately the gate voltage since it overwhelms the small polarization of the ferroelectric material. It is worth noting, however, that the ferroelectric material would be adversely affecting the transistor's current in this situation. When the gate voltage is removed, the polarization of the transistor remains and continues to affect the drain. Now since there is no active gate voltage being applied to act on the channel, the transistor is able to operate according to the ferroelectric voltage and a current as if a smaller,
negative charge was applied to the gate is produced. The result of this inverting of the active gate voltage causes the current through the transistor after a positive voltage is applied and removed to approach zero since we are dealing with n-channel transistors.

After the active gate voltage is removed, the molecule at the center of the box or ball does not remain fixed either up or down indefinitely. Instead, over time the ball begins to move towards an equilibrium, the lowest possible energy being a situation with the balls alternating up and down positions. Therefore assuming most of the balls are pushed down or pulled up, the balls will begin migrating to the opposite location to avoid the stacking of positive charges next to each other. This depolarization occurs logarithmically with respect to time and can be observed by the decay of the current down to a near zero state.

Since ferroelectric transistors have such interesting and unique behavior, we wanted to first simply characterize the behavior by looking at the affects of applying different voltages on the gate and observing current changes with these fluctuations in gate voltage and with the gate floating, or having no active voltage. Using the laboratory and equipment supplied by NASA, we were able to look at the different outputs of the ferroelectric transistor. We wanted to first characterize the ferroelectric transistor by finding the general operation behavior it exhibits. To do this, we placed the ferroelectric transistor in a simple current measuring circuit and applied a range of voltages to the gate.

Next, we wanted to examine a simple amplifier circuit with a ferroelectric transistor. In looking at this, we also wanted to observe the roles that input frequency, load resistance, initial polarization, and input DC offsets played in the final output of the
ferroelectric transistor. Since the output changed with respect to several variables, each variable had to be altered with all others being held constant.
LITERATURE REVIEW

Since this field does not have much preexisting research, most information was gathered through instruction from Dr. Fat D. Ho and Mr. Todd MacLeod. Additionally, papers published on the subject were supplied as reference material and to give further insight to the operation of the ferroelectric transistors.

- "A Study of the Characteristics of Ferroelectric Devices for use as Memory Circuits" - Todd C. MacLeod. This Master's Thesis dealt with several experiments we performed, such as characterizing the transistor through the hysteresis and finding the current decay, along with many others that we did not look at for this project. As such, it was valuable as a tool against which results were compared. However, since the transistors used in our experiments had different channel widths the results showed paralleling trends but not the same values. Additionally, the parameters of our experiments usually differed in terms of voltages applied.

- "Design of a Multi-Level/Analog Ferroelectric Memory Device" - Todd C. MacLeod, Thomas A. Phillips, and Fat D. Ho. This paper develops an idea for ferroelectric transistors to be used in memory with four logic states, rather than two. The paper goes in-depth discussing the hysteresis and decay of current, as these are integral parts in the idea of four state memory device.

- "Modeling Ferroelectric Field Effect Transistor Characteristics from Micro to Nano" - Todd C. MacLeod and Fat D. Ho. In this paper, the ideas of the operation of the ferroelectric transistor is explained in-depth. The physics behind the ferroelectric transistor is given through the discussion on threshold voltages with respect to the ferroelectric material's force opposing the voltage applied at the
gate. Any drain current will reflect these effects and so this is compensated for in the derived equations.

- "Characterizing an Analog Amplifier Utilizing a Ferroelectric Transistor" - Todd C. MacLeod, Thomas A. Phillips, and Fat D. Ho. The paper looks at a setup much like the one in our experiments for the simple amplifier circuit set up using the ferroelectric transistor. Additionally, the size of the transistor used in this setup was also a 10µm x 10µm, like the ones used in the latter portion of our testing. Plots detailing drain current for each point along the hystereses for both gate voltage active and the remnant current are shown.

- "Modeling of Metal-Ferroelectric-Semiconductor Field Effect Transistors" - Todd C. MacLeod and Fat D. Ho. A model for the operation of the ferroelectric transistor is put forth for the setup described herein. An overview of the transistor is presented, and a discussion of how the polarizing effects or remnant current affected the model.

- "Integrating Partial Polarization into a Metal-Ferroelectric-Semiconductor Field Effect Transistor" - Todd C. MacLeod and Fat D. Ho. An addition is made to the model presented in "Modeling of Metal-Ferroelectric-Semiconductor Field Effect Transistors" that accounts for the polarization of the ferroelectric transistor.
METHOD

Throughout the semester, different methods of data collection were used in collecting the various types of data. All of the experiments were carried out under the guidance of Dr. Fat D. Ho and Todd MacLeod while at the National Space Science and Technology Center (NSSTC) in one of the laboratories. All of the equipment, including the ferroelectric transistors, used were supplied by NASA.

Hysteresis

To begin understanding the ferroelectric transistor, the transistor was first characterized through obtaining a hysteresis of the current output, both when the gate-to-source voltage was active and inactive. To do this, the transistor was setup in a simple current measurement circuit (Figure 1).

![Circuit Diagram](image)

Figure 1: Circuit diagram showing the setup for the current measuring circuit used to obtain the current hystereses.

Setting a power supply at -8V, the switch separating the gate and the -8V power supply input was closed and the current read and recorded. After having recorded the value, the switch was then toggled to the off position and the resulting current measured. Having made the first set of measurements, the power supply voltage was increased by 1V to -7V
and the process repeated. This cycle was executed as quickly as possible, without allowing the data to be adversely affected in any way by the speed of the operation. By toggling the switch rapidly, the transistor was placed in saturation mode; however, if the switch was toggled slowly the transistor would not reach saturation and the output was noticeably lower. When the power supply reached the maximum of +8V, it was reversed by reducing the voltage by 1V down to 7V. This was then carried out until the voltage once again arrived at -8V and that measurement was also taken. The data was then put into a spreadsheet where the current for the gate voltage being on or off could be plotted against varying values of $V_{GS}$. This process produced two hystereses, one for the gate voltage being active (Figure 3) and the other for the gate voltage being inactive (Figure 4).

**Time-On Effects**

While using the same setup from the hysteresis collection, we decided to measure the effect of leaving the gate voltage on for extended periods of time. The input voltage was left in the on position for 20 seconds, after which the switch was toggled to the off position and the current recorded. This was repeated for time lengths of 1, 2, 3, 5, 7, 10, and 15 seconds. Next, we tried having the voltage toggle off after 0.5 seconds and as near instantaneous as possible by simply flipping it on and immediately afterwards to the off position. With the data plotted, no discernable pattern could be found, except the changes experienced when the time on approached zero. Without more data points on the curve, we could not find a fitting trend line even after taking the $\log_{10}(\text{seconds})$. 
Current Decay

Again, the setup used for the hysteresis collection was used here. First, the gate was pulsed with the a polarizing voltage of -8V or an input strong enough to drive the balls to the desired state, usually the magnitude of the input voltage is at or above 5V. Having pulsed the transistor sufficiently many times to be certain the balls have moved if desired to do so (usually two to three times), the timer is started and measurements taken at specified intervals. Since the decay was thought to be logarithmic with respect to time, as time progressed the measurements were further spaced. Once enough time had passed with the current changing little between measurements or an amount of time passed to allow for an accurate trend line (30 to 45 minutes depending on measurement spacing), the experiment was halted. This data is then placed into a spreadsheet and the current output plotted against the $\log_{10}(\text{time in seconds})$ for each measurement. A trend line was added to the plot of this data and from the equation a probable point where the current will approach 0µA, though actually achieving zero current will not be likely due to the balls being allowed to fall in any order, i.e. rather than alternating in position for the length of the ferroelectric material, which would be the ideal state in terms of lowest energy, the balls may fall in such a way that two adjacent balls are left at the top or bottom.

Amplifier

The amplifier circuit was set up differently from the original current measuring circuit (Figure 2).
By adding in a variable load, we could now test for effects on the current due to load resistance. In addition, we now used an oscilloscope connected at node 1 rather than an ammeter in series with $V_{DS}$. However, the current could still be determined easily by dividing the voltage across the load by the load resistance. We also employed the use of the function generator as $V_{GS}$, resulting in several new variables at which we must look.

First, the frequency of the input, which is a sine wave, varied to show the effects on the output. Additionally, the amplitude and DC offset of the signal could then be explored as well.

First, we set $V_{DS} = 0.5V$ and placed a load of $700k\Omega$ in the circuit for the first phase of the testing. Next, we varied the frequency ranging up to 5kHz down to 600Hz with $V_{GS}$ having an amplitude between 1 and 8V. For each frequency used, peak voltage and the phase shift were recorded. After having taken several sets of data, a resistance decade box was substituted for the resistor, which allowed sets to have much greater variation in resistance. With the new setup, we now moved $V_{DS}$ up to 0.705V for the
remainder of the experiments. In each set, the frequency and amplitude were held constant while the resistance was varied. These resistance values ranged between 35kΩ and 9MΩ. Eventually, the number of resistances measured were shortened to five logarithmically spaced values ranging between 35kΩ and 9MΩ, that is 35kΩ, 140kΩ, 560kΩ, 2.25MΩ, and 9MΩ. Frequencies ranging up to and including 1MHz were now examined.

Once the sets measuring these frequencies were completed, the idea of having a polarizing pulse before each measurement was introduced. This allowed for the determination of which section of the hysteresis on which the amplifier would operate. The polarizing pulses were ±8V, switched on while the sinusoidal input signal was not connected. Immediately after having pulsed the gate, the sinusoidal input was reconnected and the data collected. Thus, each set now became two, each with a different polarizing pulse value.

Next, we looked at having a DC component to the input signal, or a DC offset. The magnitude of the input voltage was not to exceed 8V. With this in mind, we began with a V_{offset} of 2V and lowered V_{GS} amplitude to 2V as well. The offset and amplitude were then both lowered to 1V, with the amplitude increasing to 3V for later sets. Finally, we wanted to experience the current approaching 0µA with one polarization, while observing a sinusoidal output if the opposite polarization is used. To do this, we decreased the amplitude and increased the offset, finally reaching 0.5V amplitude and 4V offset. After this data was collected, the opposite was examined by changing the offset to -2V in hopes of finding this switching state.
RESULTS and DISCUSSION

_Hysteresis_

Using the current measuring circuit (Figure 3), a range of gate voltages were applied while keeping $V_{DS}$ at 0.5V.

![Graph showing gate voltage active](image)

Figure 3: With the gate voltage active, starting at -8V the gate was applied with voltages ranging from -8V to +8V in 1V increments. Once +8V was achieved, the voltage was decreased in 1V increments back to -8V. The resulting shape shows the movement from -8V to +8V along the top and from +8V to -8V along the bottom. The 4 x 400μm transistor is used here.
Figure 4: Having pulsed the gate with an input voltage, the switch is opened once again and the resulting drain current exhibits behavior very much the opposite of the active gate operation. After pulsing from -8V to +8V and returning to -8V all in 1V increments, the hysteresis is much wider and more level than the one seen in Figure 3.

<table>
<thead>
<tr>
<th>( V_{GS} )</th>
<th>Active ( I_D ) (( \mu A ))</th>
<th>Not Active ( I_D ) (( \mu A ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>-8</td>
<td>3</td>
<td>362</td>
</tr>
<tr>
<td>-7</td>
<td>3.7</td>
<td>366</td>
</tr>
<tr>
<td>-6</td>
<td>4.55</td>
<td>360</td>
</tr>
<tr>
<td>-5</td>
<td>5.4</td>
<td>350</td>
</tr>
<tr>
<td>-4</td>
<td>7.15</td>
<td>315</td>
</tr>
<tr>
<td>-3</td>
<td>10.8</td>
<td>278</td>
</tr>
<tr>
<td>-2</td>
<td>25.6</td>
<td>67</td>
</tr>
<tr>
<td>-1</td>
<td>22.9</td>
<td>75.7</td>
</tr>
<tr>
<td>0</td>
<td>78.3</td>
<td>78.3</td>
</tr>
<tr>
<td>1</td>
<td>98</td>
<td>24.8</td>
</tr>
<tr>
<td>2</td>
<td>152</td>
<td>11.8</td>
</tr>
<tr>
<td>3</td>
<td>143</td>
<td>7.4</td>
</tr>
<tr>
<td>4</td>
<td>171</td>
<td>5.25</td>
</tr>
<tr>
<td>5</td>
<td>70</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>420</td>
<td>5.4</td>
</tr>
<tr>
<td>7</td>
<td>510</td>
<td>5.2</td>
</tr>
<tr>
<td>8</td>
<td>590</td>
<td>4.95</td>
</tr>
</tbody>
</table>
Somewhat expectedly, Figures 3 and 4 do not represent pure hystereses. Instead, the trend of the curve is evident with some anomalies. In Figure 3 at 4V with the movement back towards -8V, the output current spikes unexpectedly. Also, the rising portion of the curve seems to move slower than usual. On Figure 4, the hysteresis has a small bucket at -1 and -2V on the decreasing (top) path. Buckets were observed in many of the characteristic plots obtained during the semester, most occurring between ±1 and ±3V. At $V_{GS} = 0V$, the input voltage at the gate has no effect on the transistor and so the beginning of the trial (top curve) value for $V_{GS} = 0V$ during active operation (Figure 3) equals the beginning of the trial (top curve) value for $V_{GS} = 0V$ during inactive operation (Figure 4) as well. The same is true for the concluding curve in the trial (bottom curve).

Table 1: The table containing the values used in the Figures 3 and 4. It details the voltage iterations used on $V_{GS}$ to cycle from -8V to +8V and back to -8V.

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>560</td>
<td>5.8</td>
</tr>
<tr>
<td>6</td>
<td>453</td>
<td>5.2</td>
</tr>
<tr>
<td>5</td>
<td>261</td>
<td>5.4</td>
</tr>
<tr>
<td>4</td>
<td>180</td>
<td>5.5</td>
</tr>
<tr>
<td>3</td>
<td>24</td>
<td>5.8</td>
</tr>
<tr>
<td>2</td>
<td>13.9</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>19</td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>8.9</td>
<td>8.9</td>
</tr>
<tr>
<td>-1</td>
<td>10.9</td>
<td>34.2</td>
</tr>
<tr>
<td>-2</td>
<td>5.6</td>
<td>26.1</td>
</tr>
<tr>
<td>-3</td>
<td>3.8</td>
<td>33.1</td>
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<td>-4</td>
<td>3.7</td>
<td>44.9</td>
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<tr>
<td>-5</td>
<td>3.7</td>
<td>277</td>
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<tr>
<td>-6</td>
<td>3.3</td>
<td>324</td>
</tr>
<tr>
<td>-7</td>
<td>2.9</td>
<td>343</td>
</tr>
<tr>
<td>-8</td>
<td>2.6</td>
<td>352</td>
</tr>
</tbody>
</table>
In Table 1, the current measurements for active and inactive operation at $V_{GS} = 0V$ are shown to be the same.

Achieving inactive saturation mode for the ferroelectric transistors proved to be difficult in some cases. To move the ferroelectric transistor into inactive saturation mode, the switch controlling the input voltage had to be closed and opened rapidly. In throwing the switch in this way, the majority of the balls were forced to either down or up position. From this, it was concluded that the rate at which the input voltage changed was the basis for the balls’ operation, rather than the length of time it stayed at a particular value.

**Time-On Effects**

After observing the ferroelectric transistor’s behavior with rapid closing and opening of the switch, we wanted to experiment with changing the time the switch was closed before it was again opened. In this trial, $V_{DS}$ was increased to 1V, up from 0.5V, but $V_{GS}$ remained at -8V for maximum polarization. The result is more than doubled saturation currents. Using a simple timer to determine the time, data was finally collected (Figure 5 and Table 2).
Figure 5: Plot showing the various output currents with respect to the length of time the switch was closed.

<table>
<thead>
<tr>
<th>Time Active (s)</th>
<th>Inactive Drain Current (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>824</td>
</tr>
<tr>
<td>15</td>
<td>850</td>
</tr>
<tr>
<td>10</td>
<td>839</td>
</tr>
<tr>
<td>7</td>
<td>849</td>
</tr>
<tr>
<td>5</td>
<td>873</td>
</tr>
<tr>
<td>3</td>
<td>870</td>
</tr>
<tr>
<td>2</td>
<td>882</td>
</tr>
<tr>
<td>1</td>
<td>890</td>
</tr>
<tr>
<td>0.5</td>
<td>906</td>
</tr>
<tr>
<td>0.1</td>
<td>1588</td>
</tr>
</tbody>
</table>

Table 2: List of the times used and the corresponding currents used for Figure 5.

For the trial using 0.1 seconds active, the switch was toggled as quickly as possible, but there is still some delay estimated to be 0.1 seconds. Obviously, allowing more time to pass between the alternating of the switch has an adverse effect on the drain current. For very small times, less than 0.5 seconds, the transistor goes into saturation mode and
nearly doubles in current from the previous times. The trend for decreasing the active
time for an increased inactive current runs through nearly all of the data. Those two
readings that do not adhere to this rule could simply be anomalies for this one trial.

*Current Decay*

For a pulse of the input voltage on the gate, the current was measured at various
intervals, spaced somewhat logarithmically. From the decay line, a trend line is set and
the resulting equation analyzed.

![Drain Current Decay - VGS = -8V, VDS = 0.5V](image)

Figure 6: With $V_{GS} = -8V$ and $V_{DS} = 0.5V$, the current measurements show a nearly linear
decrease in current with respect to $\log_{10}(t)$. The trend line here fits very closely to the
actual line and is almost not visible as a result.

A initial time, $t_0$, was added to the time to form a linear line from the data
collected. In this case, only 9 seconds were needed to make the line linear. For values less
than 9, the beginning of the line curves down, below the trend line, whereas for values greater than 9, the beginning of the line curves up, above the trend line.

The final equation from the trend line is $Y = -50.554 \times X + 610.59$, making the theoretical maximum saturation current 610.59μA for this setup. Trying to find the point at which the line hits the x-axis, or becomes zero, the intercept is divided by the magnitude of the slope of the line, giving 12.07798. Raising 10 to this power to remove the logarithm function placed on the x-axis, the zero current point occurs at 1,196,674,469,447 seconds. This amount of time translates to roughly 37,920 years.

Another trial, this time run with $V_{GS} = -5V$, yielded similar results.

Figure 7: Current decay data line and trend line mimicking the data for corresponding values of $\log_{10}(\text{time})$. 
In this case, $t_0$ is 28 seconds. This arises from the fact that -5V is used as an input voltage instead of -8V. The resulting polarization is less than that achieved while using -8V. However, the currents largely coincide as if a 19 second delay happened after inputting -8V to the gate (since the -8V plot started at 9 seconds).

Again, the trend line closely follows the output of the ferroelectric transistor. However, a slightly different equation arises this time, $Y = -56.904 \times X + 652.14$. Using the same method as before to find the x-intercept or zero current point, the value is found to be 11.46035. Again, we want to convert this back to seconds, which becomes 288,638,514,604 seconds. This is approximately 9,146 years.

**Amplifier**

With a 700kΩ load on the ferroelectric transistor, we began testing by varying frequency and measuring the voltage across the load and the phase shift of the output signal.

![Frequency Effects on Output](image-url)
Figure 8: Displays the output voltage across the load for varying input frequencies for $V_{DS}$ held constant at 0.5V and $V_{GS}$ being a sine wave with amplitude 5V.

The trend line added here is a close fit to the experimental data. This shows a relatively linear relationship with frequency for the output’s voltage. This correlates with the idea that the length of time the voltage is in either the higher or lower state does not increase the output current; how quickly the voltage changes at the input is the controlling element. In this case, the increasing frequency represents an increasing rate of change of the input voltage and thus a larger current is produced at the output.

Figure 9: Figure showing the decreasing phase shift for an input increasing in frequency.

The phase shift is positive, reflecting the fact that the output is leading the input.

In Figure 9, there are two trend lines, one representing an exponential fit and the other being a linear fit to the data points. For this set of data, the exponential trend seems
to fit better, though the linear trend is not a bad approximation for the middle and end

data points. The linear approximation estimates a maximum phase shift of $178.5^\circ$, and $0^\circ$

occurring at 5.2kHz. As frequency increases, the phase shift approaches zero.

![Table 4: A table detailing the information gathered from the trial. Shown here is also the
gain, obtained by dividing the output by the input voltage (5V).

Since the input voltage was held constant at 5V through the trial, the gain is
simply 1/5 of the output. With only a few exceptions, the output voltage rises with each
successive increase in frequency. The phase shift is measured to be negative in all samples.](Image)
Figure 10: Plot showing data from all trials of $V_{DS} = 0.5V$ with a load of 96kΩ.

The four voltages displayed in Figure 10 all show a linear region of operation followed by a leveled off portion. This is most evident with $V_{GS} = 7V$. Starting at the frequency of 1kHz, this plot closely resembles that of the MOSFET characteristics I-V plot. However here, all voltages start at roughly the same output for 100Hz, and increase exponentially to a point of linearity, after which the output continues linearly until it levels off in saturation mode. The function generator used has a maximum frequency of 1MHz, but with a higher frequency generator the ferroelectric transistor may be able to exhibit a more substantial saturation region. At 1MHz input frequency, the final outputs are separated by 240-295mV.
Figure 11: Plot showing the increase in phase shift with increasing frequency with four $V_{GS}$ values appearing. For these trials, $V_{DS} = 0.5V$ with a load of 96kΩ.

For low and high frequencies, the curves split apart nicely, as they did with the peak output voltage plot. However, for frequencies ranging between 1kHz and 31.6kHz they seem to overlap. It is interesting to note that the $V_{GS} = 5$ and 7V curves have a hump at the 1kHz, whereas the $V_{GS} = 1$ and 3V curves have a slight bucket effect at 10kHz. In these trials, the phase shift crosses the x-axis with increasing frequency. Again, since the function generator is limited to 1MHz, the phase shift may be a leveling off or it may continue moving more negative.
Figure 12: Screen capture of the output (red) leading the input (yellow) for $V_{GS} = 5\text{V}$, $V_{DS} = 0.5\text{V}$, $F = 3.16\text{kHz}$, and $R = 96\text{k}\Omega$.

The output has a slight bucket effect on the rising portion of the waveform that occurs around where the input crosses the time-axis. It is evident that for a given input, the output is not necessarily, and in fact rarely, a pure sinusoid. Here the output is measured to be leading the input by $91^\circ$ based on the time the waveforms cross the time-axis.

With the decade box in place, we now held the frequency and amplitude constant on the input and instead varied the load resistance. Also, for these and the following trials, the ferroelectric transistor used was instead a $10 \times 10\mu\text{m}$ channel, rather than the $4 \times 400\mu\text{m}$ channel transistor used earlier.
Figure 13: Plot showing the effects of increasing load resistance on the output voltage for several frequencies. These trials were conducted with $V_{GS} = 6V$ and $V_{DS} = 0.7V$.

The current for these output voltages can be obtained by simply dividing the output by the load resistance for that trial. In all cases, with increasing resistance the current decreased, but not so rapidly to cause voltage decline. With almost every successive load increase the output voltage tended to increase. In Figure 13, it can be seen that there seems to exist some upper limit on the voltage output. For higher frequencies, the voltage starts close to this upper bound, whereas the lower frequencies tend towards it with increasing load resistance. The lowest frequency, 100Hz, levels off around 2/3 the voltage of other frequencies.
Figure 14: Plot showing the changing frequency with increasing load resistance.

The highest frequency, 1MHz, lies completely below the x-axis in this plot. This reassures the idea that increasing frequency will tend toward the negative phase shift. The 10kHz trial seems to have large fluctuations looking from the initial and final values obtained. It was proposed that this may be a resonant frequency, allowing many balls to move. Finally, the load is completely resistive, so it is interesting to see changes in phase from these alterations.
Figure 15: Screen capture of the output (red) and input (yellow) with $F = 10\text{kHz}$, $R = 50\text{k}\Omega$, $V_{GS} = 6\text{V}$ and $V_{DS} = 0.7\text{V}$.

The output appears to be somewhat sinusoidal, though slightly misshapen for the positive portion of the output. Also, there now appears a small bump in the output that occurs at the instant the input reaches the peak value. An almost unnoticeable bump is also present when the input reaches the minimum value, though the effect is not as exaggerated.
For this higher frequency, the phase shift has just passed over to the negative side, making the output lag the input by 7°. The output is now very sinusoidal and relatively in phase with the input. Both of these effects are chiefly due to the increase in frequency.

Now, using $V_{GS} = 2V$, we first used a polarizing pulse of -8V on the gate. This served to move the majority of the balls down in the ferroelectric material, thus giving a pre-existing mode of operation on the hysteresis.
Figure 16: Plot of the output voltage with respect to the load resistance attached to the ferroelectric transistor. Here, $V_{GS} = 2\text{V}$, $V_{pol} = -8\text{V}$, and $V_{DS} = 0.7\text{V}$.

Here the curves are somewhat mixed together making it difficult to discern a set pattern. With smaller loads, a distinct separation in output voltages is apparent. However, around $R = 1\text{M}\Omega$ the curves converge to single location, with the $F = 1\text{kHz}$ line eventually increasing to the maximum on the plot. It is interesting how steady the $F = 100\text{kHz}$ and $1\text{MHz}$ data lines are.
Figure 17: Plot showing the phase shift that occurs with the increasing load resistance. Here, too, a polarization pulse was used before switching on the sine input.

\[ V_{GS} = 2V, \ V_{pol} = -8V, \ \text{and} \ V_{DS} = 0.7V \]

We now began measuring the phase shift from peak to peak rather than when the waveforms cross the time-axis due to very non-sinusoidal output signals. The phase shift never went into the negative area of the plot for these values. Also, for \( F = 10\text{kHz} \), \( 100\text{kHz} \), and \( 1\text{MHz} \), the phase shift was 0° for half or more of the trials. Both \( F = 100\text{Hz} \) and \( 1\text{kHz} \) trials experienced a jump in phase shift at \( R = 1\text{M}\Omega \).
Figure 18: Screen capture showing the output (red) and input (yellow) for

\( F = 10\text{kHz}, V_{\text{Pol}} = -8\text{V}, V_{\text{GS}} = 2\text{V}, \text{and } V_{\text{DS}} = 0.7\text{V}. \)

Measuring the phase shift here from peak to peak gives a 39.6° shift with the output leading the input. The output is somewhat sinusoidal, if slanted to towards the input slightly. The bumps occurring at the maximum and minimum of the input signal are still present as well.

Switching the polarization pulse from -8V to now +8V, we again ran all of the trials.

![Output Voltage vs. Load Resistance with 8V Polarization](image)

Figure 19: Plot showing the output voltage with respect to the load resistance for

\( V_{\text{Pol}} = 8\text{V}, V_{\text{GS}} = 2\text{V}, \text{and } V_{\text{DS}} = 0.7\text{V}. \)

Again three of the voltages show upward trends at the onset whereas the other two are largely level throughout. As the \( F = 1\text{kHz} \) and \( 10\text{kHz} \) curves approach the \( F = 100\text{kHz} \) and \( 1\text{MHz} \) curves, both level out as well, while the \( F = 1\text{kHz} \) curve continues upwards for some time. We can see a rounding off of the \( F = 1\text{kHz} \) curve, however.
Figure 20: Plot illustrating the phase shifts for the different frequencies while $V_{\text{Pol}} = 8\text{V}$, $V_{GS} = 2\text{V}$, and $V_{DS} = 0.7\text{V}$.

As with the -8V polarization, the $F = 10\text{kHz}$, 100kHz, and 1MHz curves all are near or at $0^\circ$ for most of the duration of the trials, and again none of them move over to lag the input at any time. $F = 100\text{Hz}$ remains steady, however, and $F = 1\text{kHz}$ decreases somewhat linearly.
Figure 21: A screen capture showing the output (red) and input (yellow) for $F = 100\text{kHz}$, $R = 35\text{k}\Omega$, $V_{\text{pol}} = 8\text{V}$, $V_{\text{GS}} = 2\text{V}$, and $V_{\text{DS}} = 0.7\text{V}$. Again, the output is quite sinusoidal, but it still leads the input by 16°.

The bump occurring at the minimum of the input signal is unnoticeable, while the bump in the output at the maximum of the input is still slightly present. The signal has a much stronger resemblance to the input signal (sine wave) than at lower frequencies.

Now, adding a DC voltage component to the input signal, $V_{\text{GS}}$, we are able to view the effects on the output.

![Graph showing output voltage vs. load resistance, varying $F$ and $V_{\text{pol}}$.](image)

Figure 22: Plot showing the differences between outputs with input signals that have DC offsets. $V_{\text{GS}} = 1\text{V}$, $V_{\text{off}} = 1\text{V}$, and $V_{\text{DS}} = 0.7$.

From the $F = 100\text{Hz}$ curves, the large difference that the polarization pulse makes on the output is very noticeable. However, the $F = 10\text{kHz}$ curve dips below the $F = 100\text{Hz}$ curve for the last two loads.
Figure 23: Plot showing how the phase shift changes with differing loads when the input signal has a DC component. $V_{GS} = 1\,\text{V}$, $V_{Off} = 1\,\text{V}$, and $V_{DS} = 0.7$.

Both $F = 100\,\text{Hz}$ curves have large phase shifts, both leading the input signals, but the $F = 10\,\text{kHz}$ output signal is now able to move across into lagging the input by up to $7^\circ$. The polarization pulse difference moves the two $F = 100\,\text{Hz}$ curves away from each other.

Figure 24: Screen capture showing the output (red) and the input (yellow) for a 1V offset, $V_{Pol} = 8\,\text{V}$, $F = 10\,\text{kHz}$, $V_{GS} = 1\,\text{V}$, $V_{DS} = 0.7\,\text{V}$. 
The output now resembles the charging of a capacitor on the rising portion of the output. However, the falling portion looks very much like a sine wave. Bumps at the input signal's maximum and minimum are both present.
CONCLUSION

Hysteresis

The inactive gate hysteresis plots turned out very well when looking at the saturation current. When toggling the switch slowly, the ferroelectric transistor was not quite achieving saturation mode and thus the currents, while steady, were less than expected. Both plots are important as they illustrate the different operating modes, linear and saturation, of the ferroelectric transistor.

The dip in the hysteresis is most likely due to the gate voltage pulses not being strong enough to move the balls at that point. For $V_{GS} \leq 3V$, the voltage will only influence the output current, rather than direct it. While the input voltage is low, it depends on the previous state of the ferroelectric material to determine the current.

Time-On Effects

The time-on plot, Figure 5, shows the relationship between the frequency of switching the voltage and the output current of the transistor. Though not well seen for high frequencies from this plot, the later figures detail how well the higher frequencies make the ferroelectric transistor perform.

Current Decay

Our figures, 6 and 7, show the decay rate to be linear with time. While the trend seems correct, the data seems to over-estimate the lifetime of a charge on the transistor. It was interesting to see how the current will fall and remain constant for some time and fall again during the decay measurements. From the plots, we were able to find the theoretical
maximum saturation current, which is somewhat in line with our results from the hysteresis testing.

Amplifier

For low frequencies, we still expect some output, though diminished. So for more, lower frequency data points the trend line may become more parabolic than linear (Figure 8). This figure primarily looks into low to mid-range frequencies since it does not go below 600Hz or above 5kHz. As such, this figure would benefit from higher frequencies being added in as well. As we saw in later graphs, higher frequencies still would be preferable, but the shape of the current trends is noticeable.

For Figure 9, the phase shift plot closely resembles that of the phase shift of a Bode plot for a first order high-pass filter. In the Bode plot, there is an upper and lower limit for the phase shift, which is similar to the tail ends of the curve seen in Figure 9.

The output in Figure 12 has the bucket effect present in the hysteresis plots created earlier. It is interesting that the bucket appears at roughly the same input voltage, thus determining it is based on the input voltage, perhaps when the voltage is not able to drive the ferroelectric material balls and they begin to move to equilibrium.

One idea that I believe could hold some ground is that in Figure 14, the load resistance is advancing the curve in a manner similar to that of the frequency. Therefore,
the different curves being viewed could be thought of as a large curve and both frequency and load resistance slide along the curve.

The curves on Figure 22 show the effects of the polarization of the ferroelectric material. Though only the two $F = 100\text{Hz}$ curves are the same frequency, they truly show the current differential between the two polarizations. We would expect if the transistor were left alone for some time the balls to gravitate towards and equilibrium. If the input voltage were then applied then the output voltage would be somewhere between the two curves.

Finally, we determined that as a general rule, with increasing frequency the output voltage will also increase, but logarithmically. Also, the increasing load resistance increases the output voltage. Here, however, the current tends to decrease, be it at a slower rate. Additionally, the $8\text{V}$ polarizing pulses increase the active current. After the gate is disconnected, however, the $-8\text{V}$ polarizing pulses setup would give more current, due to the location of operation on the hysteresis curve for the inactive mode.
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