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Ferroelectric capacitance memory: characterization of an autonous non-volatile ferroelectric memory latch

Caroline Sangeetha John

FERROELECTRIC CAPACITANCE MEMORY: CHARACTERIZATION OF AN AUTONOUS NON-VOLATILE FERROELECTRIC MEMORY LATCH

by

CAROLINE SANGEETHA JOHN

A THESIS

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We, the undersigned members of the Graduate Faculty of The University of Alabama in Huntsville, certify that we have advised and/or supervised the candidate on the work described in this thesis. We further certify that we have reviewed the thesis manuscript and approve it in partial fulfillment of the requirements of the degree of Master of Science in Engineering.

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ABSTRACT

The School of Graduate Studies
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Name of Candidate Caroline Sangeetha John

Title Ferroelectric Capacitance Memory: Characterization of an Autonomous Non-Volatile Ferroelectric Memory Latch

The basic operation of an autonomous non-volatile ferroelectric memory latch was determined. The circuit was laid out using discrete components which was used to characterize the design. The process of reading and writing data '0' and '1' onto the memory latch were tested and shown experimentally. Electrical characterization of the latch was also performed experimentally by measuring the voltages and currents at different stages of memory operation. Useful characteristics of the memory circuit were its ability to retrieve data and write data even after power was removed were analyzed. The advantages of the studied ferroelectric memory over conventional flash memories were also postulated. Finally the data retention times of the data stored in the ferroelectric memory were analyzed and predicted using a mathematical model developed in Microsoft Excel.

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Commit your way to the LORD; Trust also in Him, And He shall bring it to pass.

Psalm – 37:5

I am extremely thankful to God Almighty who has been so faithful and merciful in enabling me to pursue my Masters' and successfully put forth this thesis.

I would like to acknowledge Dr. F.D. Ho for providing the motivation, guidance and constant support throughout my entire research work. Without him, this thesis would not have been possible. I am indebted to him for his time, support and invaluable insight he has given me into integrated circuit techniques.

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Finally, I would like to thank my family, whose encouragement and dedication to my future have been indispensable to me. I would like to dedicate this thesis to my parents. I am always indebted to them for all the sacrifices they have made to mold me into who I am today.

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LIST OF SYMBOLS

A	Area of the capacitor
C	Curie constant
C	Capacitance
C_{eff}	Sample effective capacitance
C_{data}	AB White ferroelectric capacitor
C_{sense}	Linear sense capacitor
D	Distance between the capacitor plates
E	Coercive field
I_{BE}	Base-emitter current of transistor
I_{CE}	Collector-emitter current of transistor
I_{Data}	Current across the ferroelectric capacitor
I_{Load}	Load current
K	Sample dielectric constant
P	Polarization of the material
P_{max}	Maximum polarization
P_r	Remnant polarization
P_s	Spontaneous polarization
$P_{S[UP]}$	Spontaneous polarization during UP state of ferroelectric capacitor
$P_{S[DOWN]}$	Spontaneous polarization during DOWN state of ferroelectric capacitor
P*	Switched polarization
P^*_r	Remnant switched polarization
P^	Non-switched polarization
$P^\wedge_r$	Non-switched remnant polarization

Q	Charge
Q_{data}	Charge stored in the ferroelectric capacitor
$R_{b(NPN)}$	Resistor at the base of transistor T1
$R_{b(PNP)}$	Resistor at the base of transistor T2
R_{in}	Input resistance
R_{load}	Load resistance
t	Thickness of the capacitor
T1	NPN junction transistor
T2	PNP junction transistor
T_c	Curie-Weiss temperature
V	Volume
V	Voltage across the conductor plates
V_{BE}	Base-emitter voltage of transistor
V_{CB}	Collector-base voltage of transistor
V_c	Coercive Voltage
V_{data}	Voltage across the ferroelectric capacitor
V_{load}	Voltage across the load
V_{max}	Maximum input voltage
V_{output}	Output voltage
V_{power}	Voltage at power supply
X	Free space permittivity
μ	Dipole Moment
ε	Dielectric permittivity of the material
ε_o	Permittivity of vacuum
β	Gain or amplification factor of transistor

CHAPTER I

INTRODUCTION

Ferroelectricity is defined as the spontaneous alignment of electric dipoles within a material under the influence of an electric field, resulting in a hysteresis loop when the direction of electric field is switched [1]. The characteristic properties of ferroelectric materials are their reversible, spontaneous polarity and non-linearity. The basis of the ferroelectric capacitance memory operation relies on the principle that when an electric field is applied to a ferroelectric capacitor, the positive and negative remnant polarization charge states of the capacitor are denoted as either data ‘0’ or data ‘1’. The main focus of this thesis is to study and characterize the operation of an autonomous non-volatile ferroelectric memory latch that employs a ferroelectric capacitor coupled with a sense capacitor in a Sawyer tower to function as the memory and latching components of the device. The applications of the studied memory latch may include:

a. State Machine.

b. Automotive and Aerospace Applications [2].

c. FPGA configuration control [2].

A. Motivation for Research

Since the late 1980's, there has been a growing interest in ferroelectrics for standalone and non-volatile memory operations [3]. The ferroelectric memory array and latch circuit that have been suggested and analyzed to this day embed ferroelectric capacitors within a cocoon of clocks, control signals and programming lines [4, 5]. This structure does not fully utilize the data storage properties of the ferroelectric capacitor which is the ability to hold its memory state within those changes of its crystal lattice with or without an external circuit. The ferroelectric capacitance memory latch circuit studied in this thesis fully exploits this ferroelectric property and has the ability to operate without any clocks or control lines which makes it fully autonomous. The properties of the ferroelectric material to store an electric polarization in the absence of an electric field make the device non-volatile. The circuit which is used to characterize the design was laid out using discrete components. This thesis analyses the electrical characterization and data retention of the latch circuit.

B. Advantages of Ferroelectric Memory

Ferroelectric memory is an emerging non-volatile memory technology that has several key advantages over the most mundane, extensively used flash memories. Ferroelectric memories offer greater program erase endurance which exceeds over 10^{13} programmable erase cycles [6]. Ferroelectric memories have faster write speeds as they work on symmetrical read / write cycles. Ferroelectric memories can be programmed with voltages which are low as 2 volts. Flash memories require relatively large program and erase voltages in the order of approximately 10 volts [7]. Also, ferroelectric memories possess the capability of being designed using CMOS technology. Further, the

autonomous ferroelectric memory latch discussed in this thesis is asynchronous as it does not employ any external clocking circuitry for its operation.

C. Scope of Work

This thesis is organized in a manner such that it devotes a chapter to each of the following subjects: Ferroelectric theory, Ferroelectric capacitance memory, Non-volatile ferroelectric memory latch and Electrical characterization of the latch. Chapter II focuses on basic ferroelectric properties including crystal structure, polarization and hysteresis. Chapter III discusses capacitance theory with special importance to the electrical behavior of the AB white type ferroelectric capacitor. Chapter IV analyses the design and device functionality of the autonomous non-volatile ferroelectric memory latch. The electrical characterization and data retention properties of the latch are extensively discussed in chapter V.

CHAPTER II

FERROELECTIC THEORY

The theory of ferroelectricity dates back to ancient times. They were merely a curiosity until the start of the twentieth century when these materials were introduced to practical usage. Although ferroelectric materials can be used in many forms, the bulk crystal form was the first to be put to practical use due to the fact that they occurred naturally.

A. History

Pyroelectricity is the ability of materials to generate current in response to a change in temperature. Studies were carried out in the eighteenth and nineteenth centuries to characterize the properties of such materials like tourmaline [8]. It was also seen that such materials could attract objects when heated. The first ferroelectric material to be identified was Rochelle salt, sodium potassium tartrate tetrahydrate ($NaKC_4H_4O_6$-$4H_2O$). Rochelle salt had been in use for its medicinal properties since the seventeenth century; however its physical properties were not extensively studied until the late nineteenth century [9]. In 1880, the piezoelectric property of Rochelle salt was identified by the Curie brothers. Piezoelectricity is the phenomena where charge generates on the

surface of the material when the material is subjected to an external stress [10]. Below a certain temperature the material spontaneously became polarized. This temperature is known as the Curie point. Ferroelectricity is an electrical phenomenon by which certain materials exhibit a spontaneous dipole moment, the direction of which can be switched by the application of an electric field [11]. All ferroelectric materials have a transition temperature which is the Curie point, T_c. At $T < T_c$, the crystal exhibits ferroelectricity while for $T > T_c$, it is not ferroelectric.

However it was only in 1920 that Valasek discovered the ferroelectric property of Rochelle salt [4]. The polarization of the Rochelle salt material could be reversed when an electric field was applied to it. The ferroelectric property was considered exclusive to Rochelle salt until Bush and Scherrer in 1935 discovered that potassium dihydrogen phosphate (KH_2PO_4) also exhibited the same property [9].

Study of crystals with crystal structure similar to that of KH_2PO_4 led to the discovery of a family of materials known as ammonium salts which were also found to display ferroelectric properties. A typical ferroelectric salt, ammonium dihydrogen phosphate ($(NH_4)H_2PO_4$) was found to show Antiferroelectrics properties. This meant that the adjacent crystal structures had opposite polarity below the Curie Point thus rendering the overall polarity of the crystal to be zero. ($(NH_4)H_2PO_4$) was widely used as a SONAR transducer on ships during World War II. This extensive application of a ferroelectric material greatly increased the amount of research performed in this area [12]. The discovery of ($(NH_4)H_2PO_4$) greatly simplified the study of ferroelectrics as its crystal structure was much simpler when compared to Rochelle salt (16 atoms versus 112 atoms).

Later in the 1940's Ferroelectricity was discovered in Barium titanate BaTiO3 [13]. Barium titanate had a Curie Point of 120^{o}C which was well above room temperature. This in turn led to the discovery of Lead zirconium titanate ($Pb(Zr_xTi_{1-x})O_3$) also known as PZT which was found to have a much higher transition temperature of 215^{o}C. Since its discovery PZT has become the most widely used ferroelectric material today. Ferroelectric research has extended to liquid crystals and high polymers, which is a major development since Ferroelectricity was considered as a property specific to solids for over fifty years [13].

B. Crystal structure

The ferroelectric material utilized in this research is lead zirconium titanate. The molecular formula of PZT given as $Pb_1Zr_xTi_{1-x}O_3$ corresponds to its Perovskite ABO_3 crystal structure. There are 8 lead atoms at the corners which are shared by 8 adjacent cells which gives one lead atom per cell. The six faces of a cell have one centrally located oxygen atom that is shared by two cells which gives 3 oxygen atoms per cell. A zirconium or titanium unshared atom is contained within each cell. In a perovskite there are no metal to metal bonds. Every metal atom is bonded only to the nearby oxygen atoms.

Ferroelectrics are polar materials that possess at least two equilibrium states i.e., spontaneous polarization state in the absence of an electric field, and the state in which the spontaneous polarization, P_s may be switched between those orientations by an external electric field [14]. Most ferroelectric materials are found to undergo a structural phase transition from a higher temperature non-ferroelectric phase into a low-temperature

ferroelectric phase. The phase transition temperature is the Curie point. Above the Curie point the dielectric permittivity of the material falls off with temperature in accordance with the Curie – Weiss Law [15].

$$\varepsilon = \varepsilon_0 + \frac{C}{T - T_0} \approx \frac{C}{T - T_0} \tag{2.1}$$

where, ε = dielectric permittivity of the material, ε_0 = permittivity of vacuum (8.85 * 10^{-12} F/m), C = Curie constant, $T_0 (T_0 \leq T_c)$ = Curie-Weiss temperature.

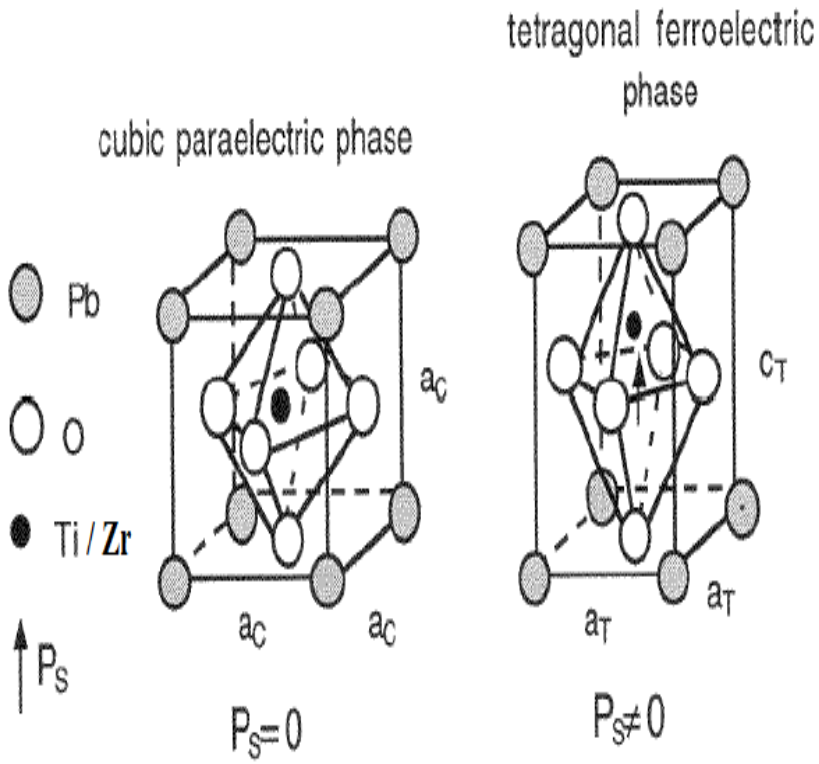

Figure 2.1 Crystal structure of PZT in Paraelectric (Ps=0) and Ferroelectric Phases (PS≠0) [15]

PZT has a cubic structure in the non-ferroelectric, Paraelectric phase and a tetragonal structure in its ferroelectric phase as shown in the Figure 2.1[15]. Although PZT is ferroelectric, and lead titanate is also ferroelectric, lead zirconate is actually anti-ferroelectric and has a transition to the paraelectric cubic state at 230° C [16]. In lead zirconate, displacements of Pb atoms in adjacent unit cells are in equal but opposite directions, thus making it anti-ferroelectric. By applying an electric field, lead zirconate can be forced into the ferroelectric state.

The titanium atom is off center which causes its bonds with the four center faced oxygen atoms to be tilted upwards. Further the electrons of these four bonds tend to hang around the oxygen atoms more that the titanium atoms giving every metal – oxygen pair a net electric dipole. This explains the basic structural unit of electric dipole that is always present in each of the cells due to the displaced cation. Since dielectric constant depends on this displacement, PZT can have a high dielectric constant. The titanium atom can be made to force its way to the other side by applying an electric field in the same direction of the naturally occurring dipole. This forces the natural dipole to point downward. Thus material can have any combination of up or down dipoles. Each of the dipoles will combine with others to form groups called domains which in turn can be forced to switch directions. The cumulative direction of all the domains renders the material its memory component.

C. Polarization

Polarization of the ferroelectric material can be defined as the total dipole moment per unit volume [17].

$$P = \sum \mu / V \qquad (2.2)$$

Where, P = Polarization of the material

μ = Dipole Moment

V = Volume

Ferroelectric materials demonstrate a spontaneous non zero polarization when the applied electric field is zero. This spontaneous polarization can be reversed by an applied electric field [18]. The polarization is spontaneous at the Curie temperature; the crystal structure of the ferroelectric material is transformed from a nonpolar to a polar state [19]. The regions of the crystal with the spontaneous polarization oriented in a uniform direction are called ferroelectric domains. The area between two ferroelectric domains is referred to as the domain wall. When the direction of the spontaneous polarization throughout the material is random in such a way that the net polarization is zero, the pyroelectric and peizoelectic effects corresponding to the individual domains will cancel each other. In such cases polycrystalline ferroelectric materials may be bought to their polar state by applying a strong electric field at elevated temperatures. This process of reorienting domains within individual crystal grains in the direction of the applied field is called poling [14].

D. Hysteresis

The domain wall switching in response to an applied electric field in ferroelectric materials results in the occurrence of the ferroelectric hysteresis loop. Hysteresis is the relationship between the externally applied electric field and the resulting polarization.

The polarization is not only dependent on the current electric field but also on its past values [16].The hysteresis loop can be measured experimentally by using a Sawyer – Tower Circuit. Figure 2.2 [14] shows the ferroelectric hysteresis effect with the applied electric field on the x-axis and the measured polarization. The circles with arrows represent the polarization state of the material at indicated electric fields. The Figure displays several segments and points of interest. As the intensity of the applied field increases the domains which have unfavorable direction start to switch to the direction of the electric field as seen in segment B-C. All the domains are aligned at point C then the relation becomes linear as seen in segment C-D. Spontaneous polarization, Ps is measured as the intercept of extrapolation of this segment with the y-axis.

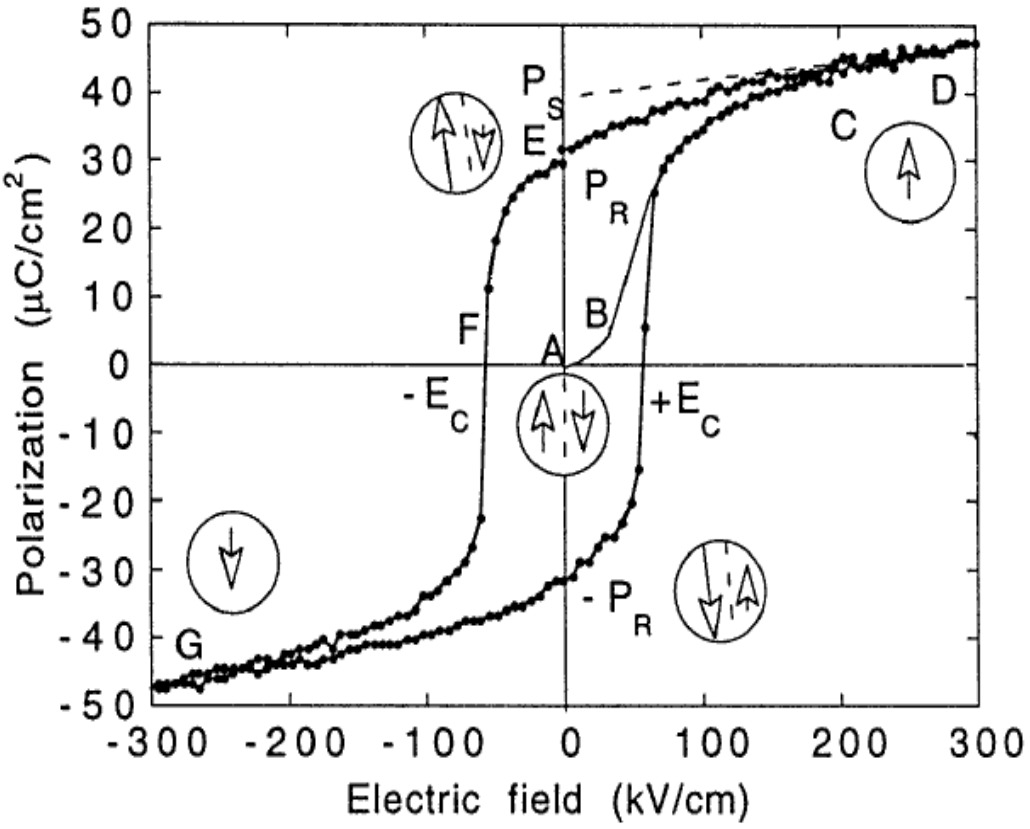

Figure 2.2: Ferroelectric Hysteresis loop [14].

Beyond point D the electric field decreases and the polarization starts to switch back, but when the electric field becomes zero the polarization is non-zero as indicated by point E. The polarization value at which the applied electric field is zero is termed as remnant polarization; $P_{r.}$ In order to bring the polarization to zero the electric field has to be reversed. The applied electric field required to cause zero polarization is called the coercive field $E_{c.}$ Point G is the maximum polarization that can be achieved when the applied electric field is reversed.

CHAPTER III

FERROELECTRIC CAPACITANCE MEMORY

The vital part of the memory latch that is to be characterized is the ferroelectric capacitor. In this chapter we go through the capacitance theory of linear, paraelectric and ferroelectric capacitors with importance to the behavior of AB white ferroelectric capacitors along with its need to be used in the memory latch configuration.

A. Linear and Paraelectric Capacitors

A capacitor is a passive electrical component that consists of two conductor plates separated by a dielectric material. When voltage is applied across the conductor plates an electric field generated across the dielectric causing positive charge to be collected on one plate while negative charge collects on the other plate. The capacitance of is the measure of the charge that is contained within a unit volume of the capacitor. It is measured in farads.

$$C = Q/V \tag{3.1}$$

where,

C = Capacitance

Q = Charge

V = voltage across the conductor plates.

When the dielectric between the plates is vacuum, the capacitance is given by the equation

$$C = \varepsilon_0 A/t \tag{3.2}$$

where

ε_o = dielectric permittivity of vacuum = 8.84 x 10^{-14} Farads/cm

A = area of the capacitor

t = thickness of the capacitor

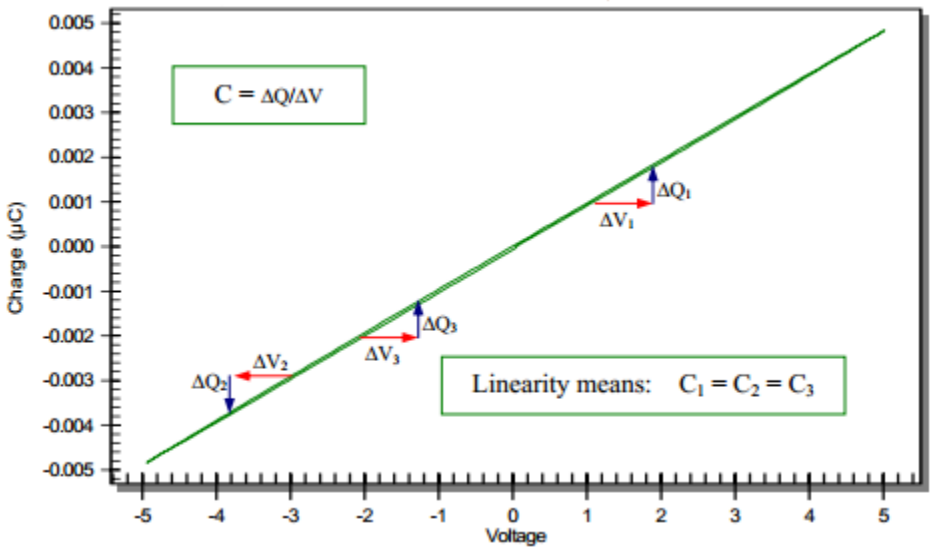

Figure 3.1: Relation between charge and voltage in a linear capacitor [20].

Combining the two equations we get $Q = (\varepsilon_0 A/t)V$ which represents the equation of a straight line $Y = mX + b$ where Y is the charge Q, m is the slope of the straight line given by C and b is the Y – intercept which is zero. A linear capacitance is one in which the capacitance, $C = \Delta Q/\Delta V$ is constant for all voltages [20]. A paraelectric capacitor is one with a non-linear plot in the relation between the charge on the conductor plates and the applied voltage. Paraelectricity is the ability of many materials to become polarized under an applied electric field.

Unlike ferroelectricity, this can happen even if there is no permanent electric dipole that exists in the material, and removal of the field results in the polarization in the material returning to zero [21]. In the linear capacitor the relative dielectric constant is due to the displacement of the electrons on the application of the electric field. On the other hand the crystal lattice of paraelectric materials is so compact that there is a displacement of entire atoms on the application of the electric field giving rise to the non-linear plot in the relation between charge and voltage. Paraelectric materials have a relatively high dielectric constant.

B. Ferroelectric Capacitor

A ferroelectric capacitor is one in which the material between the two conducting plates is ferroelectric. Ferroelectric capacitors exhibit non- linear properties and tend to have very high dielectric constants. As explained in chapter 2 Hysteresis occurs in the polarization Vs voltage plot of the ferroelectric capacitors due to the fact that their internal dipoles can be switched with the application of an external electric field.

Polarization in ferroelectric capacitors is the ratio of the total charge stored on the plates of the capacitor to the area of the plates.

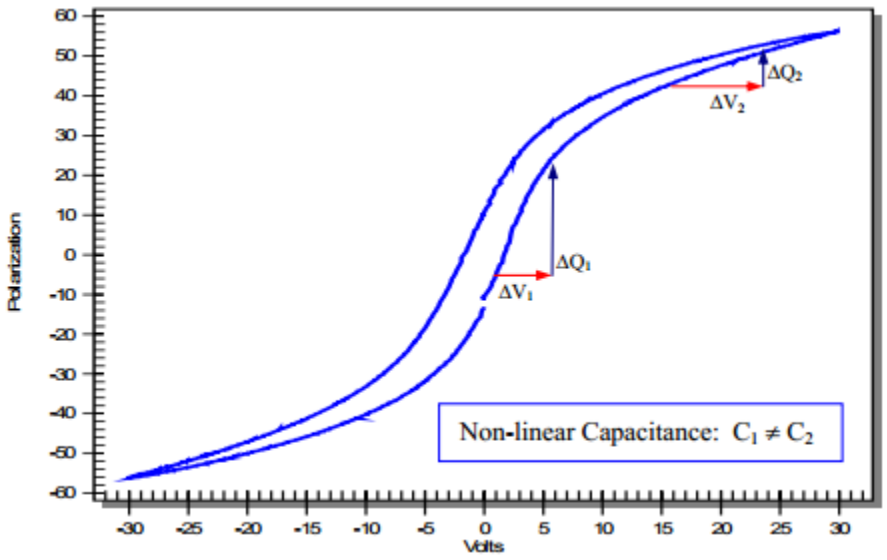

Figure 3.2: Relation between charge and voltage in a paraelectric capacitor [20].

The amount of charge flow in the ferroelectric capacitor when electrically pulsed is measured using a Sawyer- Tower circuit [15]. The circuit consists of a voltage source that can generate both positive and negative pulses, a ferroelectric capacitor and a sense capacitor. The sense capacitor acts as an integrating capacitor that stores the charge released by the ferroelectric capacitor during a pulse from the source.

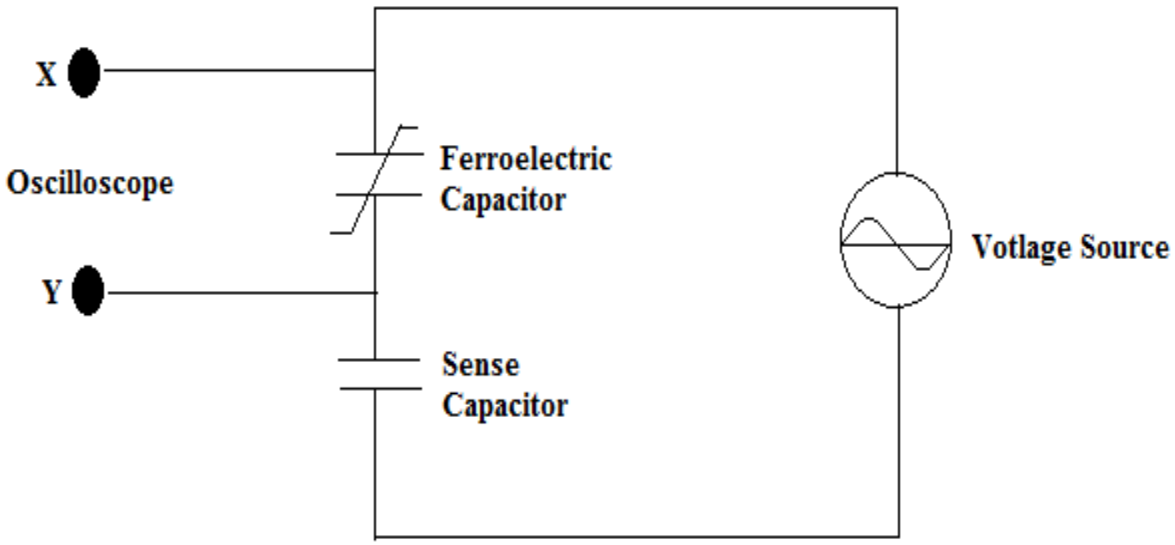

Figure 3.3: Sawyer Tower Test Circuit

C. Type AB white Dual Ferroelectric Capacitors

The ferroelectric capacitor used in this research is an AB white capacitor from Radiant Technologies. The Type AB package contains two identical 2550Å thick, 20/80 PZT capacitors. Each die (Die RC2-AAA) is packaged in a four-lead TO-18 header. One package lead connects to the case and is labeled GND. The two capacitors share a single COMMON but have separate leads for their other electrodes. The COMMON lead connects to their bottom electrodes. The total PZT lead content per die is 1.7 milligrams [22]. The detailed packaging is seen in figure 3.4.

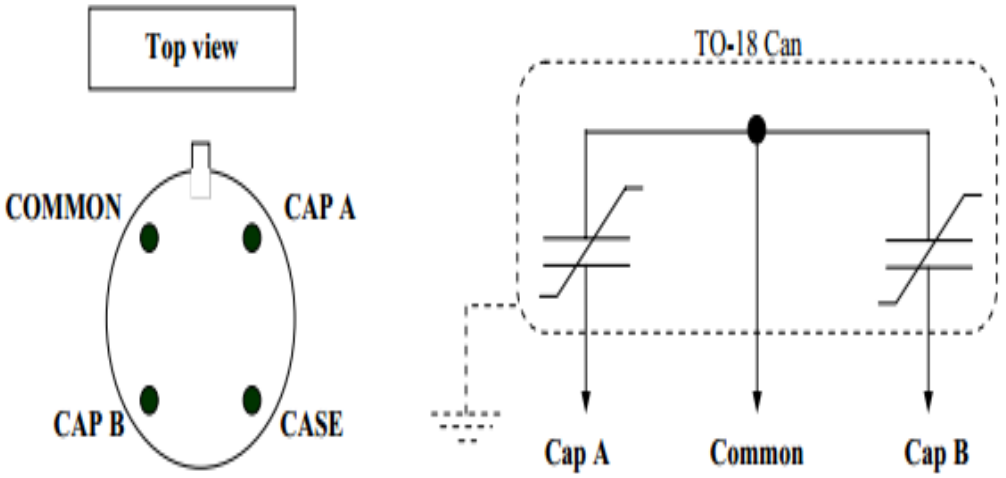

Figure 3.4: AB white capacitance packaging [22]

The AB white capacitor structure is shown Fig 3.5. The polycrystalline platinum bottom electrode has a thickness of 1500 Å whereas the top polycrystalline electrode measures 1000 Å. The 20/80 PZT is deposited in seven layers to 2550 Å. The metal interconnect is made using 200 Å chromium and 5000 Å gold.

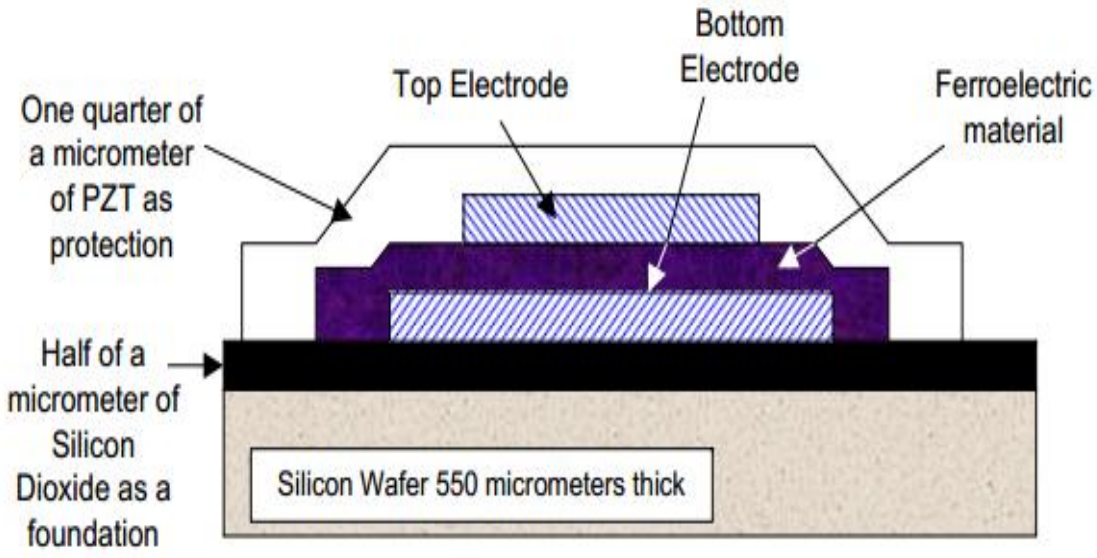

Figure 3.5 AB white capacitor structure [22]

D. Hysteresis of the AB white Ferroelectric Capacitor

The behavior of the PZT AB white capacitor was studied using the Vision 4.6.0 Software Package from Radiant Technologies. The capacitor has an area of 10,000μ^2 and has a thickness of 2550Å undoped 20/80 PZT. Fig 3.4 was obtained using the 'charge function' that shows the relation between the charge and the drive voltage.

In linear and paraelectric capacitors shown in Fig 3.2 and 3.3 we see that the charge is zero when the applied voltage is zero whereas in Fig 3.6, the measured charge is non-zero at zero volts. The hysteresis loop moves counterclockwise from 0V to +6V, +6V to 0V, 0V to -6V and -6V back to 0V. Point 'a' is the starting point of the charge state of the capacitor after a previous state which left it at a fully down condition. The point 'b' is the charge state of the capacitor when the voltage changes from +6V to -6V. Point 'c' is the final point of measurement. It is to be noted that the loop did not end exactly where it started. When point 'c' is measures again after a few seconds the charge will decay to point 'a'. In the same way if the measurement was at point 'b' instead of going all the way to point 'c', the charge would have decayed to point'd'. Thus there is always an excess charge or remnant charge in the capacitor that contributes to the memory component of the capacitor. Fig 3.6 shows the hysteresis of the AB white ferroelectric capacitor whose maximum polarization, P_{max} = 35.64$\mu C/cm^2$, Remnant polarization, $P_r = \pm 24\mu C/cm^2$ and the Coercive voltages, $+V_c$ = 2.48V $-V_c$ = -1.46V.

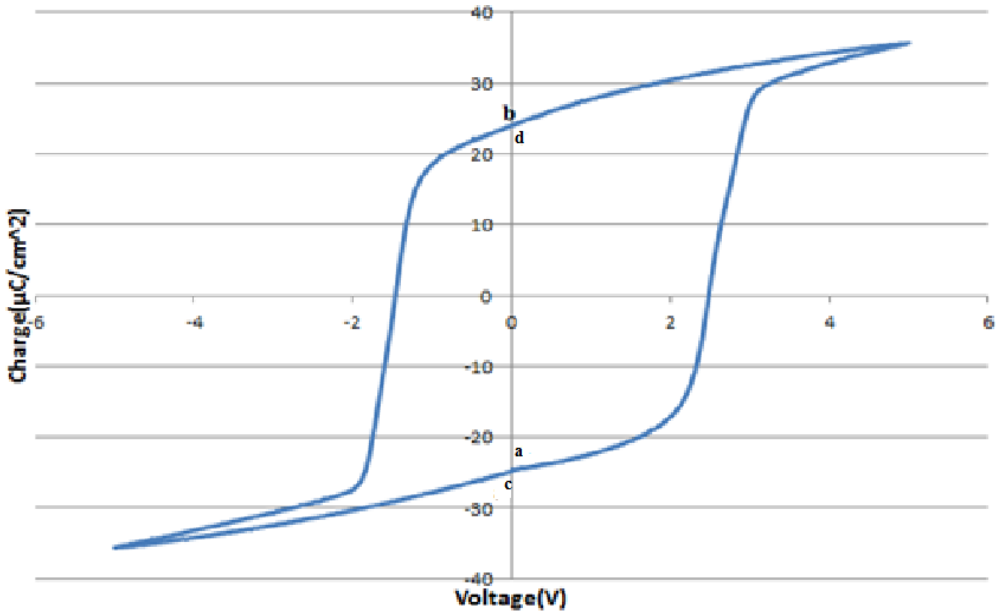

Figure 3.6: Hysteresis of a PZT AB white ferroelectric capacitor.

E. Measurement of Polarization

Polarization is measured as the total charge per unit area of the conductor plates in the ferroelectric capacitor. As mentioned earlier, the amount of charge flow through a ferroelectric capacitor can be measured using a Sawyer-Tower Circuit. Polarization in the AB white test capacitor was measured using Vision 4.6.0. Fig 3.7 shows the pulse train from the AC source and the points at which the polarization in the capacitor is measured. The first pulse in the negative direction is a preset pulse where no measurement is made. The second pulse is made in the positive direction and the switched polarization, P* is measured at the top of this pulse. The next measurement is made after the pulse delay in order to measure the remnant switched polarization, P*r. The third pulse is in the same direction of the second and the non-switched polarization, P^ is made. The non-switched remnant polarization, P^r is made at the end of the following pulse delay. The fourth pulse is made in the negative direction in order to measure the switched polarization, -

P*in the negative direction. After the pulse delay the negative switched remnant polarization, -P*r is measured. The Fifth pulse is in the direction of the previous pulse. The non-switched polarization –P^ and the corresponding remnant polarization, -P^r are made. Fig 3.8 indicates the polarization measured with each pulse. These polarization measurements are used to calculated the effective capacitance, dielectric constant of the capacitor, and also the remnant polarization is a measure of retention which is the primary memory characteristic of the ferroelectric capacitor used in the design of the autonomous non- volatile memory latch.

Table 3.1 shows the polarization parameters of the AB white ferroelectric capacitors measured at V_{max} = ±5V, Pulse width = 1ms, Pulse delay = 1000 ms.

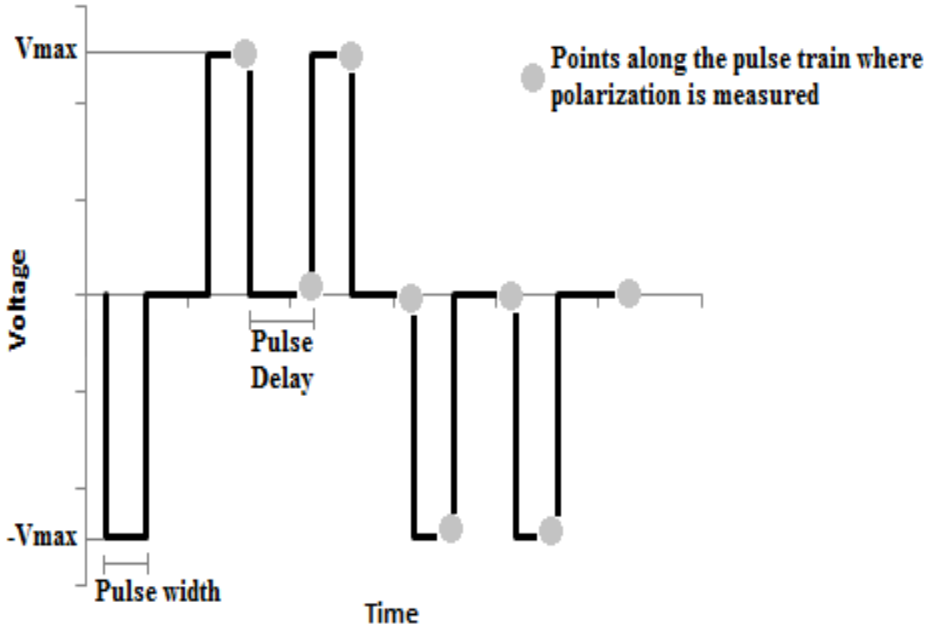

Figure 3.7: Pulse train used to measure polarization

V_{max}/-V_{max}(V)	Polarization(μC/cm^2)	
5	P*	60.95
0	P^*_r	48.25
5	P^	12.71
0	$P^\wedge_r$	0.47
-5	-P*	-59.68
0	$-P^*_r$	-48.35
-5	-P^	-11.55
0	$-P^\wedge_r$	-0.36
Pulse Width(ms) = 1		
Delay Time(ms) = 1000		

Table 3.1: Polarization parameters of AB white ferroelectric capacitor

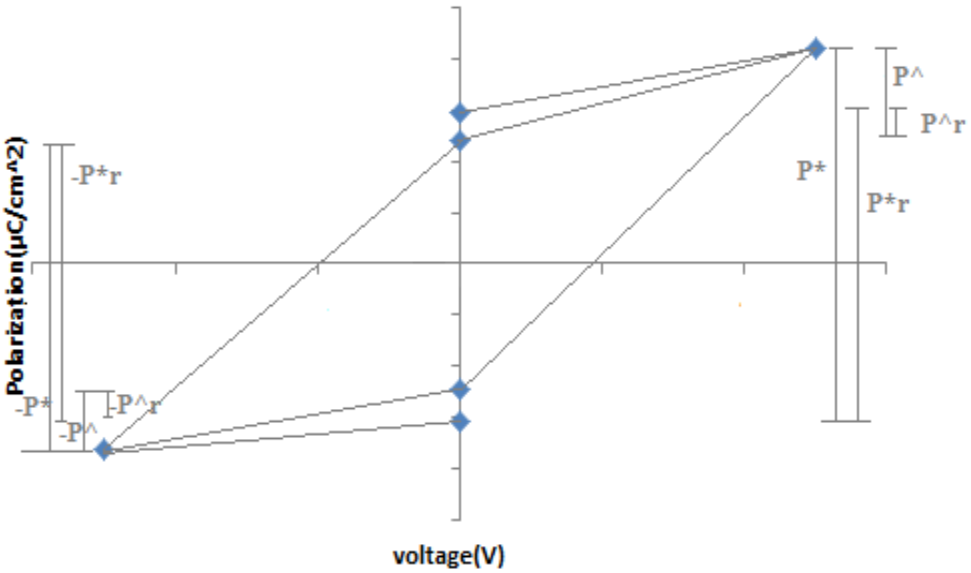

Figure 3.8: Polarization measured with each pulse [23]

F. Calculation of Effective Capacitance

Using the polarization parameters made by the measurement discussed above the Effective Capacitance of the AB white was calculated.

$$\text{Effective Capacitance} = [(\text{Delay}) \text{ x } (P^*) \text{ x } (A)] / V_{max} \quad (3.3)$$

Where

Delay = Pulse delay specified in the input pulse train in ms

P^* = Switched polarization measured atop of the second pulse in $\mu C/cm^2$

A = Area of the capacitor in cm^2

V_{max} = Maximum input voltage

Using the parameters from Table 3.1 the effective capacitance for that particular measurement can be calculated as follows

Effective Capacitance sample of the AB white Capacitor (C_{ef})

$$= ((1000) \text{ x } (60.95) \text{ x } (0.0001))/5$$

$$= 1.219 \text{ nF}$$

G. Calculation of Dielectric Constant

The dielectric constant of the capacitor material is usually calculated using the equation [20].

$$C = \frac{X\varepsilon A}{d} \tag{3.4}$$

Where

C = Capacitance in farads

X = Free Space Permittivity

ε = Permittivity of the capacitor material

A = Area of the capacitor in square centimeters

D = Distance between the capacitor plates in centimeters

Using the parameters measured using the Vision 4.6.0 featuring in Table 3.1 the sample effective capacitance is calculated as follows

$$K = \frac{((C_{ef}) \text{ x } (t))}{A \text{ x } \varepsilon_0} \tag{3.5}$$

$$= 3099.59$$

Where

K = Sample dielectric constant

C_{ef} = Sample effective capacitance in nF

t = thickness of the dielectric material in μm

$\varepsilon_0 = 8.854 \text{ x } 10^{-12}$

A = Area of the capacitor in cm

Thus we see that the PZT material used in the AB white ferroelectric capacitor has a very high dielectric constant. It is to be noted that the dielectric constant is a measure of the electrical polarizability of a material and a crucial quantity in the construction of capacitive elements in electronics.

Materials with high dielectric constants are of great interest and are being developed for increased charge storage in a smaller area in memory chips. The ability of ferroelectrics to exist in two different polarizations in the absence of a field is being used for non-volatile ferroelectric memories.

H. Calculation of the total number of dipoles

The total number of electric dipoles present in PZT "AB" white capacitor by Radiant Technologies is calculated below.

Area of the capacitor = 10,000 μm^2

Thickness of the capacitor = 0.26 μm

Capacitor Volume = Area of the capacitor * Thickness of the capacitor

= 10,000 μm^2 * 0.26 μm

= 2,600 μm^3

The unit cell in PZT is 0.0004U per side. Hence,

Unit cell volume = $(0.0004\mu m)^3$

$= 0.64 * 10^{-10}\ \mu m^3$

Number of dipoles present in each capacitor = Capacitor Volume / Unit cell volume

$= 2{,}600\ \mu m^3 / 0.64 * 10^{-10}\ \mu m^3$

$= 40{,}625 * 10^{-9}$ dipoles.

CHAPTER IV

NON-VOLATILE FERROELECTRIC MEMORY LATCH

The non-volatile ferroelectric memory latch was constructed using the AB white ferroelectric capacitor in a Sawyer – Tower as its core functional circuit. The latch works on the principle that when an electric field is applied to a ferroelectric capacitor, the positive and negative remnant polarization charge is denoted as either data ‘0’ or data’1’.The properties of the ferroelectric material to store an electric polarization in distortions of their crystal lattice with or without a circuit attached in the absence of an electric field makes the device non-volatile. The latch holds the new data as long as power is applied and returns automatically to that state when the power is removed and reapplied ensuring non-volatility. Further the memory latch is autonomous as it operates with the ground, power and output node connections, without any externally clocked control line. This explains the ability of the latch to operate without the presence of control logic, a microprocessor, or logic-level voltage supplies. Additionally the latch can be written when powered off which will be explained in detail further in this chapter. This chapter will include the detailed design layout and functionality of the memory latch.

A. Circuit Design and Analysis

The circuit diagram of the autonomous non-volatile memory latch as shown in Figure 4.1 consists of a NPN transistor; T_1, PNP transistor; T_2, an AB white ferroelectric capacitor; C_{data} ; a linear capacitor; C_{sense}, an input node and a power supply node. The latch can be analyzed in three different stages as follows

- Primary Autonomous Memory Circuit.
- Addition of the feedback loop to the Memory Circuit to form a latch.
- Addition of charge-based Read Circuit.

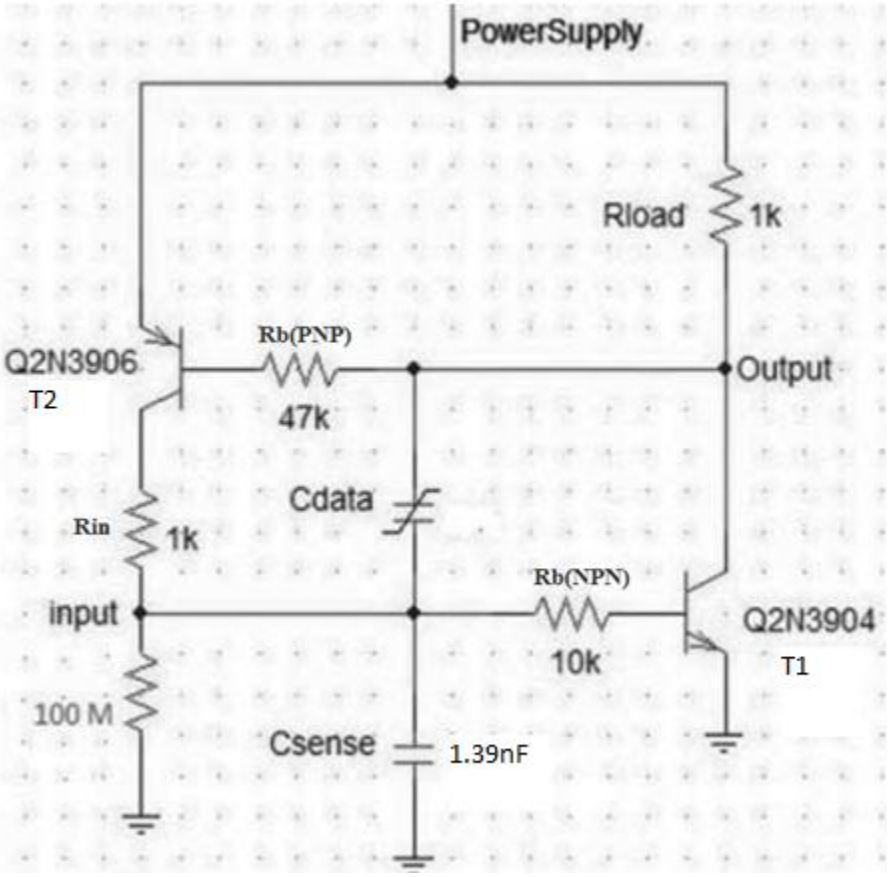

Figure 4.1 Autonomous non- volatile memory circuit [24]

The Primary Autonomous Memory circuit consists of the AB white ferroelectric capacitor, transistors T_1 which is of NPN type that does not turn ON unless the threshold voltage exceeds 0.7V and resistors R_b (NPN) and R_{load} as shown in Figure: 4.2.

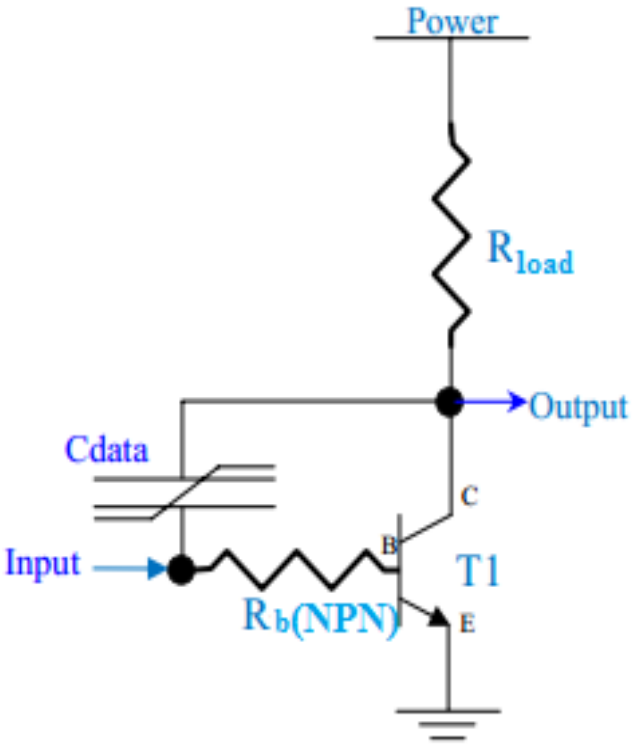

Figure 4.2: Primary Autonomous memory Circuit

For a single ferroelectric capacitor to operate as a memory element in an autonomous memory circuit we must make sure it eliminates any control lines and clocks, be associated with another device which can sense its state and will have a method of changing its state. In order to achieve the above specifications the ferroelectric capacitor can be combined with a transistor to produce variable impedance. In Figure 4.2 the NPN transistor T_1 acts as the state detector and the R_{load} translates the memory state [25].

When the power supply is turned ON, the ferroelectric capacitor C_{data} charges through the resistor R_{load} as shown in the equivalent circuit Figure 4.2 until it reaches saturation. The current from the ferroelectric capacitor passes through the base-emitter diode of T_1 resulting in a larger current through the collector-emitter terminal of T_1 by a factor of $\beta * I_{BE}$ as shown in the equivalent circuit Figure 4.3

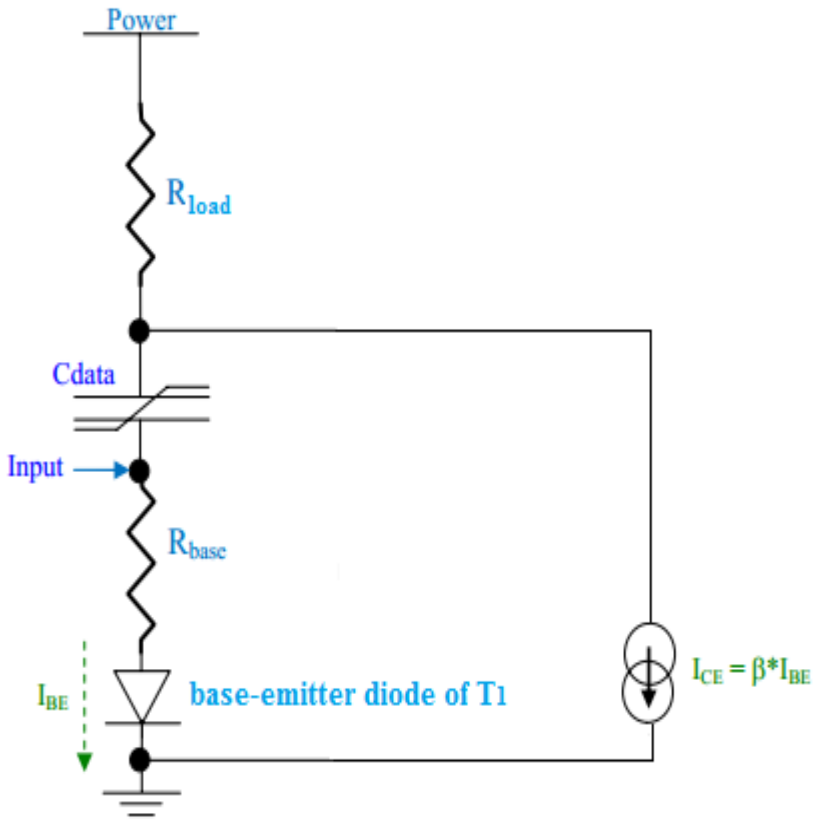

Figure 4.3: Equivalent circuit showing charge and current flow through the circuit

Hence, the current through the resistor R_{load} is given by the equation

$$I_{load} = I_{data} + \beta\ (I_{data}) \quad (4.1)$$

$$I_{load} = I_{data}\ (1+ \beta) \quad (4.2)$$

However, the current through R_{load} determines the voltage drop, V_{load} across it and thus the voltage across the ferroelectric capacitor is given as

$$V_{data} = V_{power} - V_{load} - I_{data} R_{b(NPN)} - V_{th} \quad (4.3)$$

$$V_{data} = V_{power} - V_{load} - I_{data} R_{b(NPN)} - 0.7V \quad (4.4)$$

Substituting for V_{load} we get

$$V_{data} = V_{power} - [(1+\beta) I_{data}] R_{load} - I_{data} R_{b(NPN)} - 0.7V \quad (4.5)$$

The final output voltage is the difference the voltage at the power node and the voltage drop across the resistor R_{load} as follows

$$V_{output} = V_{power} - [(1+\beta) I_{data}] R_{load} \quad (4.6)$$

In the above equation the current across the ferroelectric capacitor, I_{data} depends on both the output voltage and the remnant polarization state of the ferroelectric capacitor. This is affirmed by the following plot in Figure: 4.4 which is a measure of the charge generated by the ferroelectric capacitor as a function of the voltage using the Vision 4.6.0 package.

The voltage applied across the capacitor makes the horizontal axis while the vertical axis is the sum of all the charge that comes out of or gone into the ferroelectric capacitor at each voltage on the horizontal axis since the beginning of the test. The voltage across the ferroelectric capacitor that is necessary to bring the value of the charge to zero is termed as the Coercive Voltage, V_c. It is to be noted from the Figureure that the coercive voltage for the AB white type ferroelectric capacitor used in the design of the autonomous non-volatile ferroelectric memory latch is around ± 2 V.

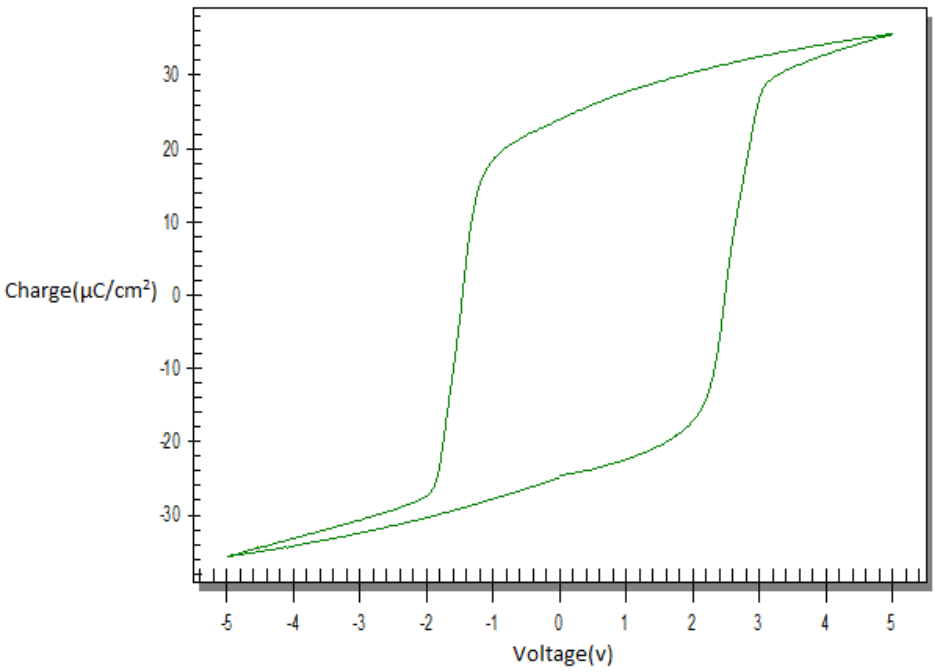

Figure 4.4 Hysteresis loop of the AB white ferroelectric capacitor

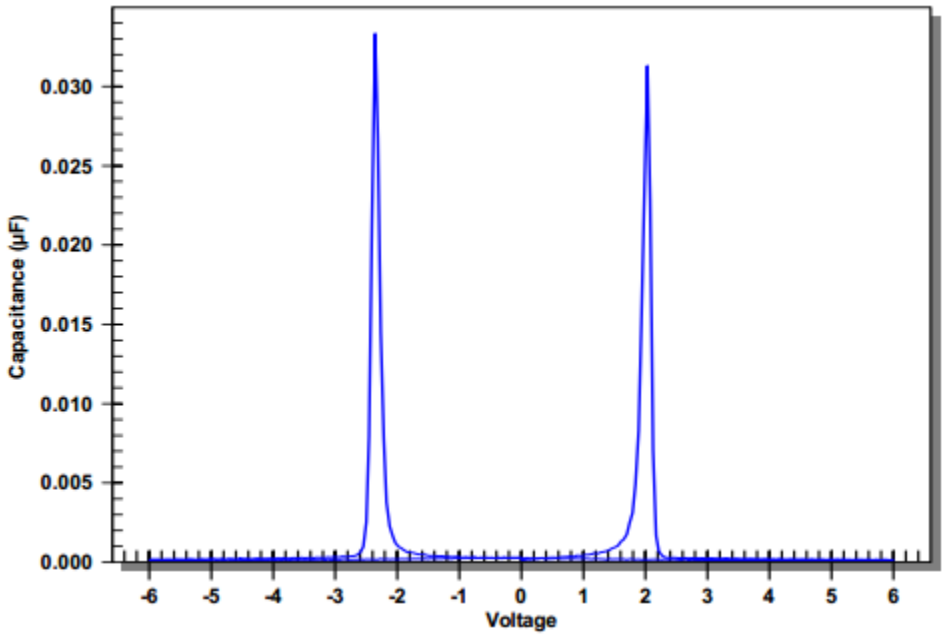

Figure 4.5 Instantaneous capacitance Vs voltage for an AB white ferroelectric capacitor

Figures 4.4 and 4.5 are keys to understanding the autonomous memory of the latch. Figure 4.5 shows the mathematical derivative of Figure 4.4 with the instantaneous capacitance on the y-axis and the applied voltage on the x-axis. The plot shows peaks of 0.033 μF which is termed as the switching capacitance. The interesting fact is that switching voltages around which the switching capacitances occur correspond to the coercive voltages shown in Figure 4.4. Thus once the latch design is complete the data states can be switched by switching the remnant polarization states of the ferroelectric capacitor, which in turn can be switched by an externally applied switching voltage whose value is around the coercive voltage of the AB white type ferroelectric capacitor. For design purposes the peaks of switching capacitances are termed as the capacitor DOWN states whereas the non-switching capacitances are termed as capacitor UP states. The DOWN and UP states of the capacitor will be translated to Data '0' and Data '1' of the latch which will be further explained in under 'device functionality' in this chapter.

The next stage of the design is the addition of the feedback circuit as shown in Figure: 4.6. The feedback circuit should latch to the data '0' state if an input voltage occurs but let the circuit stabilize to the data '1' state in case there is no applied input voltage. The feedback circuit must also serve rewrite the UP state in case of data '1' and DOWN state in case of data '0' back into the ferroelectric capacitor. Transistor $T_{2,}$ a PNP bipolar transistor is added on to the memory bit in Figure: 4.3 as a feedback transistor to form latch. This transistor does not turn ON until the voltage across the R_{load} is less than the base emitter threshold voltage, V_{BE} which is approximately 0.7 V.

The feedback circuit must compare the output voltage to some sort of reference voltage in order to latch to either data '0' or data '1'. In this case the voltage drop across

the resistor R_{load} is used as the reference voltage for latching. The value of R_{load} is chosen relative to the value of C_{data} so that it can be forced to generate only a small voltage drop across R_{load} when data '0' needs to be latched and to generate a much larger voltage drop across the R_{load} to latch to data '1'.

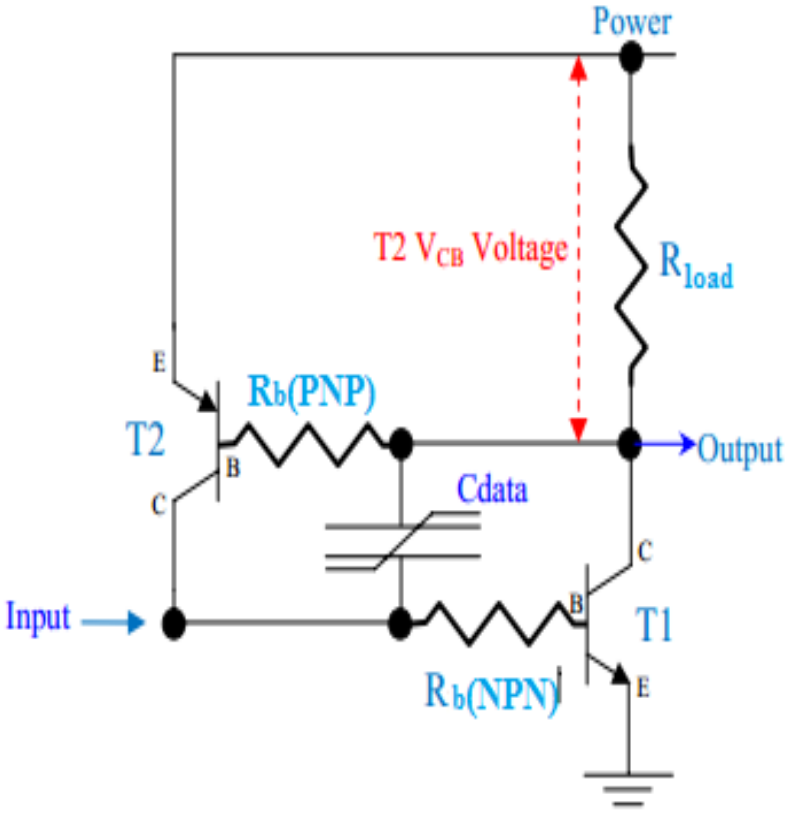

Figure 4.6: Addition of feedback loop

The operation of Figure 4.6 can be explained as follows. When there is a non - switching ferroelectric current across the ferroelectric capacitor C_{data}, the voltage across the resistor R_{load} is way below the base - emitter threshold voltage, V_{BE}. Hence the transistor T_2 remains OFF. With T_2 OFF, T1 also remains OFF pulling the output node high to represent data '1'. On the other hand when there is a switching current across the

ferroelectric capacitor, the voltage across the resistor R_{load} exceeds the base – emitter threshold voltage of 0.7 V that turns ON transistor T_2 forcing T_1 also to turn ON. This pulls the voltage at the output node low to represent data'0'.

In the next stage of design small resistances are added to the circuit in order to limit the power required to change the state of the latch.

In the circuits shown in Figure 4.2 and 4.6, the current flow through the base circuit of the bipolar transistor T_1 is used to modulate the state of the latch. A charge – based method enable us to carry out this operation more precisely. Thus a Sawyer tower circuit is constructed using the sense capacitance, C_{sense} around the base of the transistor T_1.

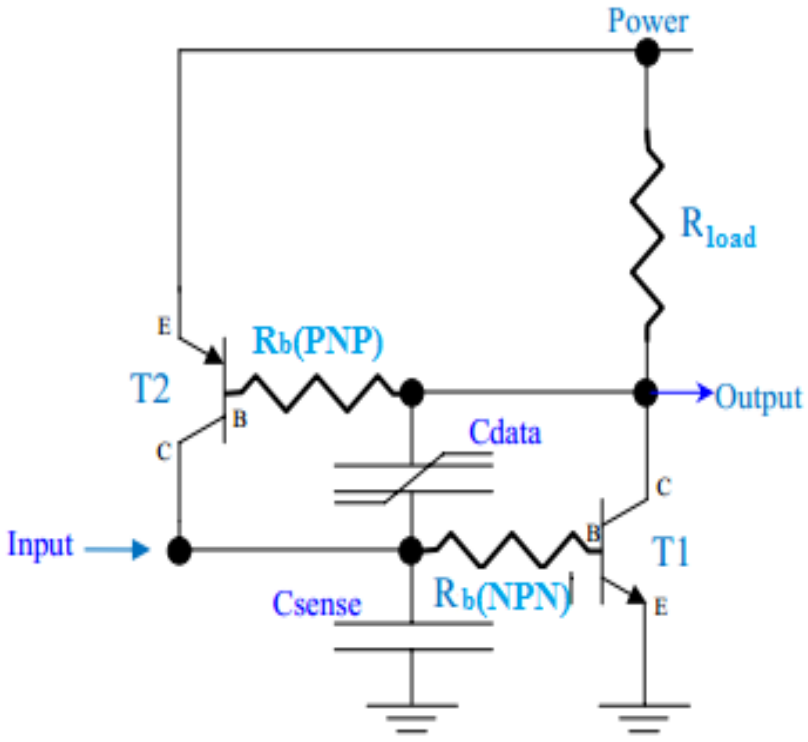

Figure 4.7: Addition of charge based Read Circuit

The sense capacitance collects the charge from the ferroelectric capacitor which enables the voltage on the base of the transistor T_1 to be equal to

$$V_{b\ (NPN)} = Q_{data} * C_{sense} \quad (4.7)$$

The sense capacitance is chosen in such a way that if there is no switching in the ferroelectric capacitor, C_{data}; the total charge that is collected from the ferroelectric capacitor is such that the voltage generated is way below the threshold voltage of the transistor, T_1. If the ferroelectric capacitor in its switched state, the voltage at the base of the transistor, T_1 rises above the threshold voltage of the transistor. The size of the capacitor also depends on the amount of charge generated by the ferroelectric capacitor. The sense capacitance range will be discussed in detail in the next chapter using experimental data as well as hysteresis half loops measured for the ferroelectric capacitor using the Vision 4.6.0 package.

B. Device Functionality

The coercive voltage V_c described earlier in this chapter which is required to bring the charge in the ferroelectric capacitance to zero is termed as the Write Enable voltage with respect to the designed autonomous non-volatile ferroelectric memory latch. The write enable voltage is very crucial when it comes to changing the states of the latch between data ‘0’ and data ‘1’.

C. Write Operation [28]

In order to write a data ‘1’, the voltage at the power supply is brought down to 2 volts which is the write enable voltage. Meanwhile, there is no applied input voltage. With zero volts at the input node, the charge collected by the sense capacitance is not sufficient enough to make the base emitter voltage of T_1 higher than its threshold. This turns OFF transistors T_1 and T_2 setting the output node high in order to represent data ‘1’.

In order to write a data ‘0’, the voltage at the power supply is brought down to 2 volts corresponding to the write enable voltage which switches the state of the ferroelectric capacitance C_{data}. Now an input voltage of +2V at the input node. The switching of the ferroelectric capacitor causes a higher amount of charge to be collected across the C_{sense} which enables the base emitter voltage of transistor T_1 to cross its threshold turning on the transistors T1 and eventually also T2. This sets the voltage at the output node to be low in order to represent a data ‘0’.

Figures 4.8 and 4.9 show that the data ‘0’ and data ‘1’ have been written to the latch. The arrow indicates the data written. The voltage at the power supply node is denoted in blue while the voltage at the node between the capacitors, C_{data} and C_{sense} is denoted in yellow.

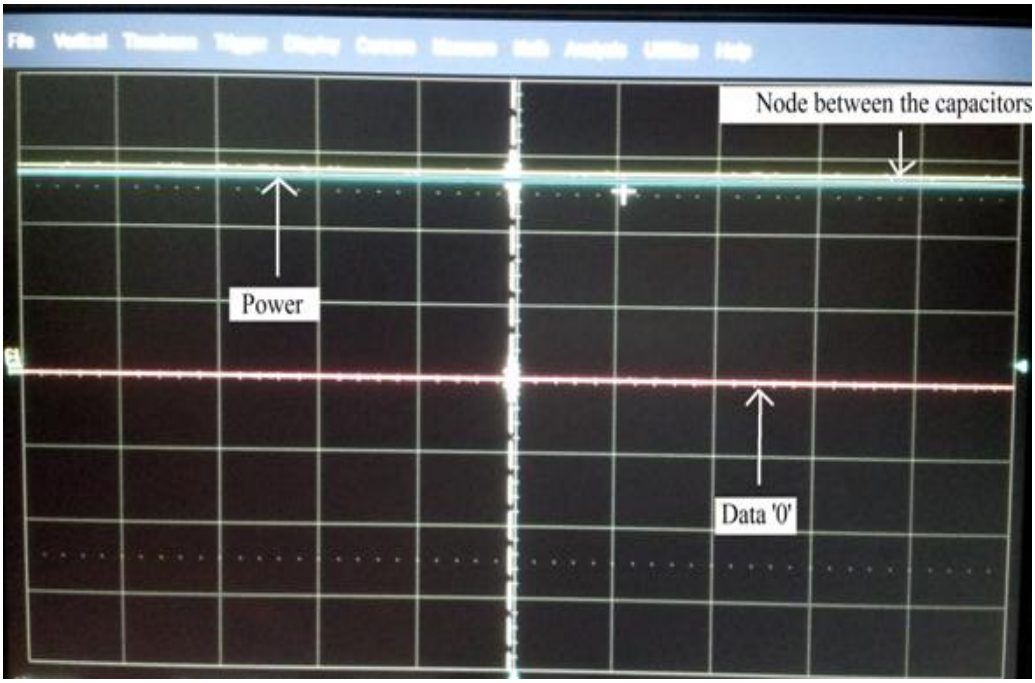

Figure 4.8: Writing a ‘0’ to the latch [28]

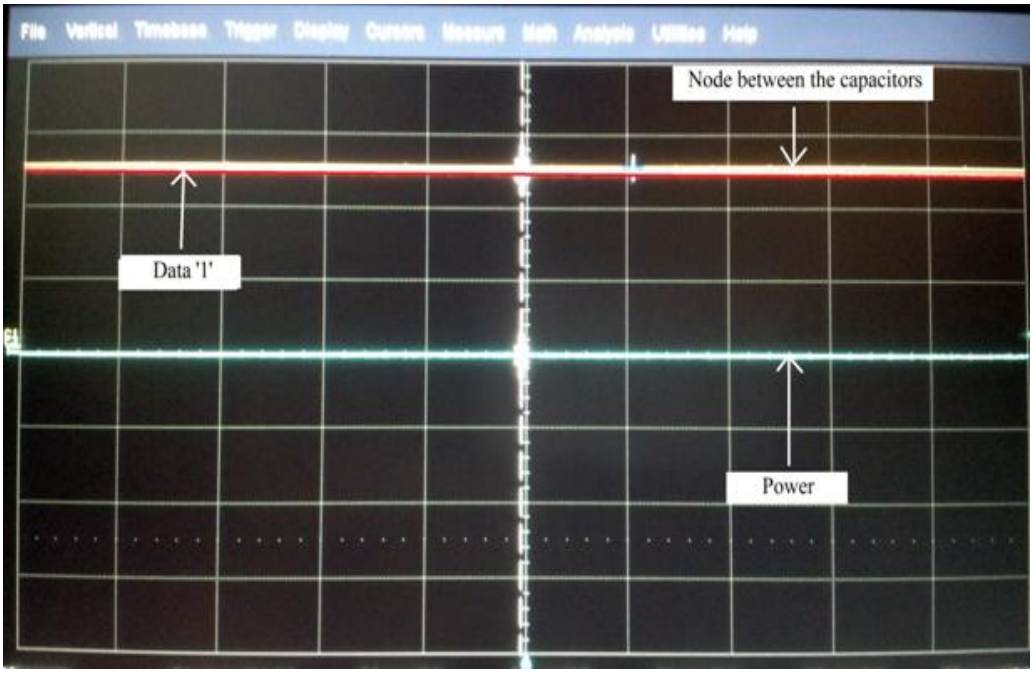

Figure 4.9: Writing a ‘1’ to the latch [28]

D. Read Operation [28]

Once the power is turned ON, the C_{sense} acquires the data state from the ferroelectric capacitance C_{data}. The two capacitors in the Sawyer tower circuit are in the ratio such that if the C_{data} is in a switched state, the charge collected by the C_{sense} will produce a base emitter voltage high enough to turn ON transistor T_1 and eventually T_2. This makes the voltage at the output node low which is read as data '0'.

On the other hand if the ferroelectric capacitor C_{data} produces a non-switching current through the C_{sense}, the base emitter at T_1 will be significantly way lower than the threshold which turns OFF transistor T_1 and T_2. With transistors T_1 and T_2 in the OFF state, the output node is pulled high which is read as data '1'.

Figures 4.10 and 4.11 show that the data '0' and data '1' have been read from the latch. The arrow indicates the data being read. The voltage at the power supply node is denoted in blue while the voltage at the node between the capacitors, Cdata and Csense is denoted in yellow.

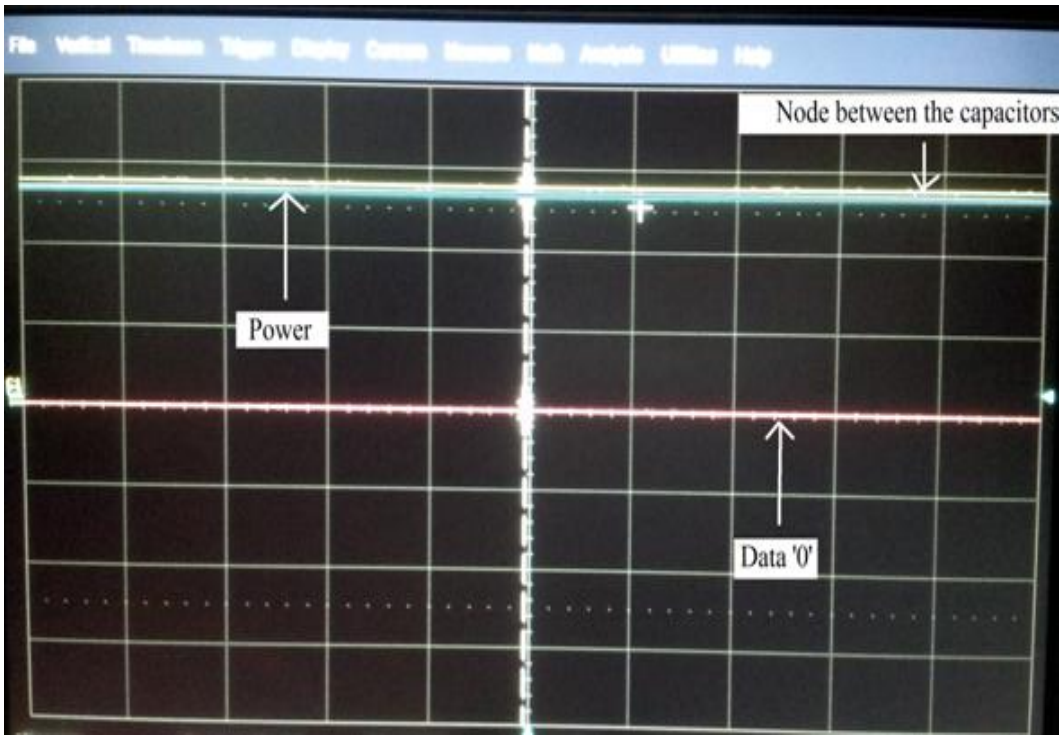

Figure 4.10: Reading a ‘0’ from the latch [28]

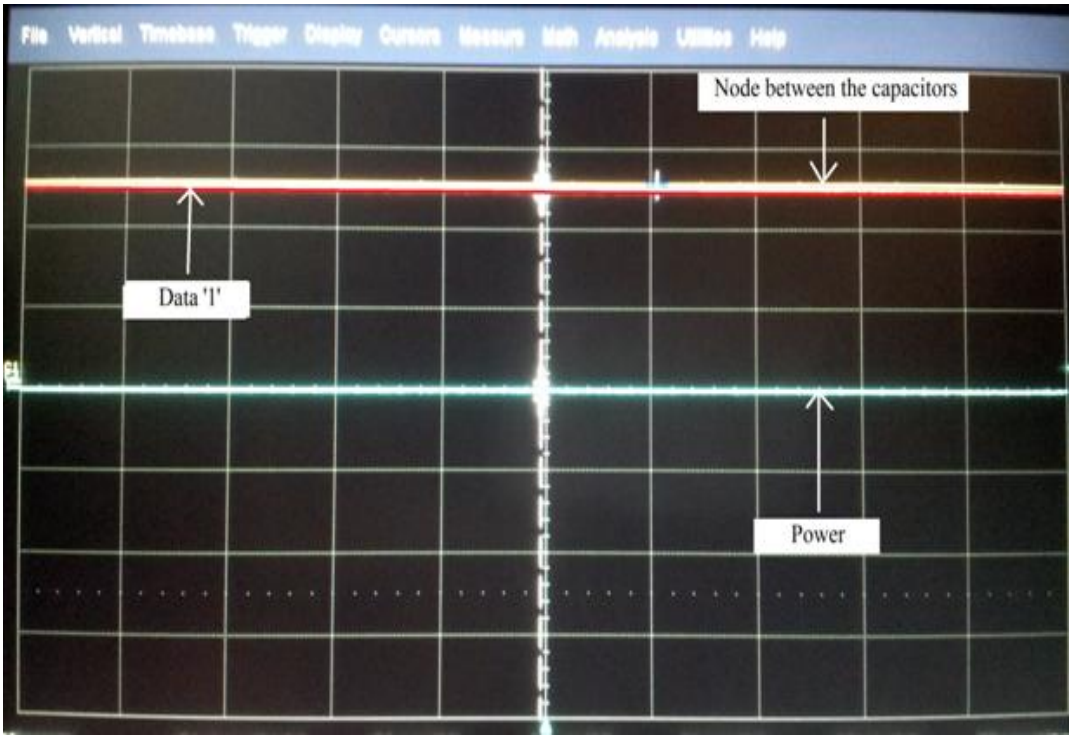

Figure 4.11: Reading a ‘1’ from the latch [28]

CHAPTER V

ELECTRICAL CHARACTERIZATION OF THE LATCH

Having thoroughly discussed the design as well as the device functionality of the autonomous non-volatile ferroelectric memory latch, this chapter will focus on its electrical characterization. The working range of the vital parameters such as the input voltage, write enable voltage and the sense capacitance are experimentally measured and compared with the theoretical data [30].

A. Input voltage range for a data '0' write

The input voltage is very important while writing the data '0' on to the latch. It corresponds to the coercive voltage that is required to change the state of the charge flow from the ferroelectric capacitor to the sense capacitor to a switched state in order to produce a voltage large enough to turn ON transistor T_1 which will in turn pull the output node to a low state to represent a data'0' [31].

Table 5.1 is a representation of the experimental data for the different input voltages which were used to write a data'0' on to the latch ranging from 5.2 to 0.5 volts.

From the table it can be clearly noted that a minimum input voltage of 0.8 volts is required in order to make a successful data ‘0’ write. For the sake of the latch an optimal input voltage of 2 volts is chosen to write data’0’ on to it.

Input Voltage (V)	Data’0’ Write Status
5.2	Successful
4.1	Successful
3.8	Successful
2.5	Successful
1.5	Successful
1.0	Successful
0.8	Successful
0.7	Unsuccessful
0.6	Unsuccessful
0.5	Unsuccessful

Table 5.1: Input Voltage range for writing a ‘0’.

B. Write enable voltage for a data ‘1’ write

The write enable voltage is the minimum voltage below which a data ‘1’ is written on to the ferroelectric memory latch. The voltage is required to bring the capacitance of the ferroelectric capacitor C_{data} to its non-switching state as shown in Figure 4.5 of the previous chapter. The charge flow to the sense capacitor in this state is maintained in such a way that the voltage generated at the base-emitter terminal of transistor, T_1 is always less than its threshold voltage to maintain the OFF state [32]. This keeps the voltage at the output node high which is represented as data’1’.

Table 5.2 is a representation of the experimental data for the different write enable voltages which were used to write a data’1’ on to the latch ranging from 5 to 0 volts. From the table it can be clearly noted that a data ‘0’ is written onto the latch when

the voltage at the power supply node is any lesser than 3 volts. For the sake of the latch an optimal write enable voltage of 2 volts is used to write data ’1’ on to it.

Write Enable Voltage (V)	Data ‘1’ Write Status
5.0	Unsuccessful
4.8	Unsuccessful
4.6	Unsuccessful
4.4	Unsuccessful
4.2	Unsuccessful
4	Unsuccessful
3.8	Unsuccessful
3.6	Unsuccessful
3.4	Unsuccessful
3.2	Unsuccessful
3	Unsuccessful
2.9	Successful
2.8	Successful
2.6	Successful
2	Successful
1	Successful
0	Successful

Table 5.2: Write Enable voltage for writing a ‘1’.

C. Current at Power Supply Vs. Write Enable Voltage

Once the input voltage and the write enable voltage ranges were determined, the current at the power supply node was measured for the different write enable voltages with data ‘1’ in memory. This is shown in Figure 5.1 where the voltage at the power supply node is represented on the Y-axis while the write enable voltages are represented on the X axis. The data shown in this figure was measured with the sense capacitance, C_{sense} value to be 1.39 nF.

Figure 5.2 shows the current measured at the power supply node for the different write enable voltages when data ‘0’. It is to be noted that the measurements were made

after the 2 V input was removed from the input node. The current at the power supply node after the removal of the input voltage required to switch the capacitance of the ferroelectric capacitor is represented on the Y axis while the corresponding write enable voltage is represented on the x-axis.

Figure 5.3 is the measure of the current at the power supply node for the different write enable voltages with data '0' in memory and also the without the removal input voltage used to switch the ferroelectric capacitance.

As shown by the figures discussed above, the voltage at the power supply node for all the three different cases is pretty linear with the respective write enable voltages.

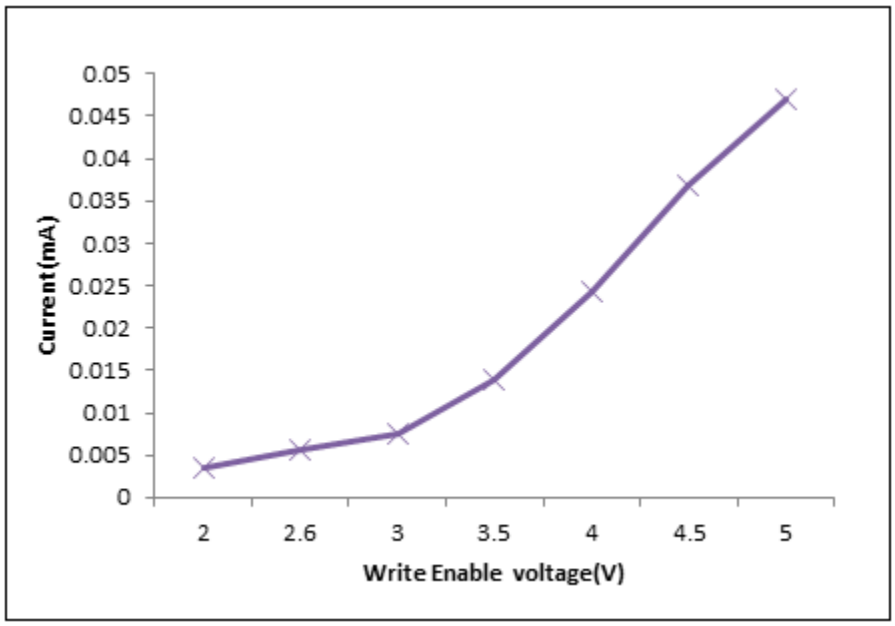

Figure 5.1: Current at power supply when data '1' is in memory

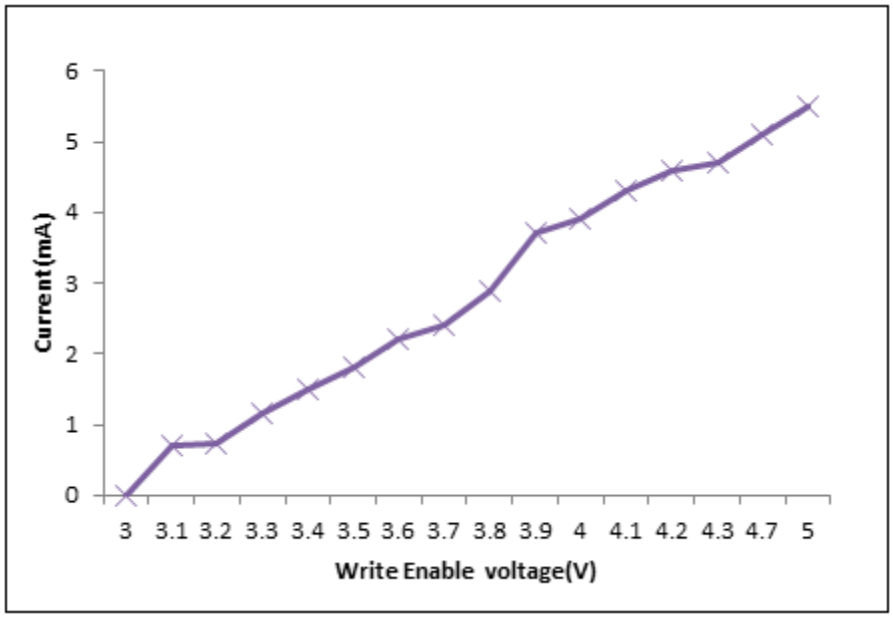

Figure 5.2: Current at power supply when data '0' is in memory after the removal of the 2V Input

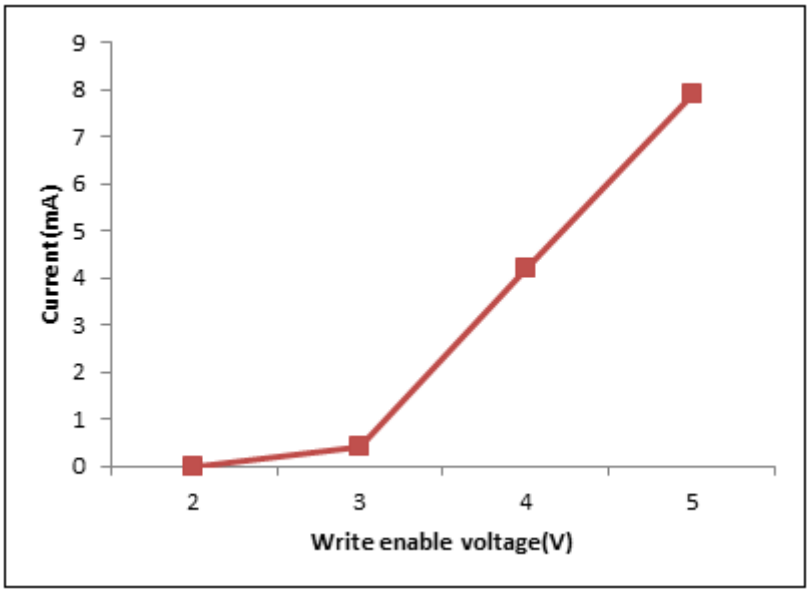

Figure 5.3: Current at power supply when data '0' is in memory without the removal of the 2V Input

D. Current at Input node Vs. Write Enable Voltage

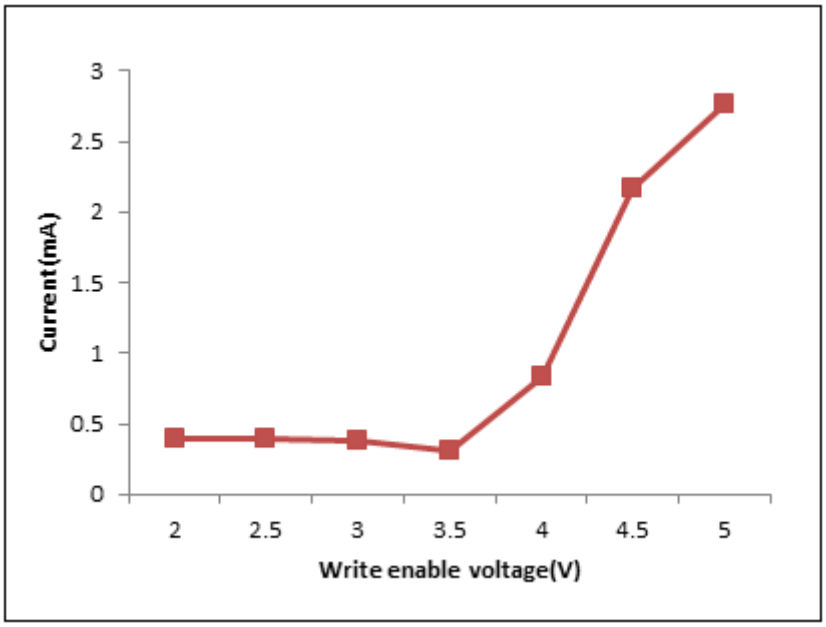

Figure 5.4: Current at the Input node with data '0' in memory

E. Sense capacitance working range

The value of the sense capacitance, C_{sense} is very crucial in the operation of the autonomous non-volatile ferroelectric memory latch as it collects the charge flow from the ferroelectric capacitor which produces the necessary voltage to turn the transistor T_1 ON and OFF. C_{sense} is chosen in such a way so that when there is no switch in the ferroelectric capacitor, C_{data} ; the total charge coming out of the ferroelectric capacitor influences the base voltage of transistor,T_1 remains well below the threshold voltage and latch the circuit to latch high in order to represent data '1'. On the other hand if there is a switch in the ferroelectric capacitance the charge should cause the base voltage to rise above the threshold voltage of T_1 and latch the circuit to low to represent a data '0'.

Table 5.3 shows the experimental data which shows the different sense capacitances ranging from 1nF to 7nF with their write statuses for both data '0' and data '1'. It working range of the sense capacitor for successful data writes can be deduced from the table to be 1.3 to 4.3 nF.

This working range of the ferroelectric can be further confirmed using the switching and non-switching half loop hysteresis curves of the ferroelectric capacitor.

Sense Capacitance (nF)	Data	Write Status
1	0	Unsuccessful
	1	Unsuccessful
1.2	0	Successful
	1	Unsuccessful
1.3	0	Successful
	1	Successful
1.5	0	Successful
	1	Successful
2	0	Successful
	1	Successful
4	0	Successful
	1	Successful
4.3	0	Successful
	1	Successful
4.5	0	Unsuccessful
	1	Successful
5	0	Unsuccessful
	1	Successful
6	0	Unsuccessful
	1	Successful
7	0	Unsuccessful
	1	Successful

Table 5.3: Sense capacitance working range

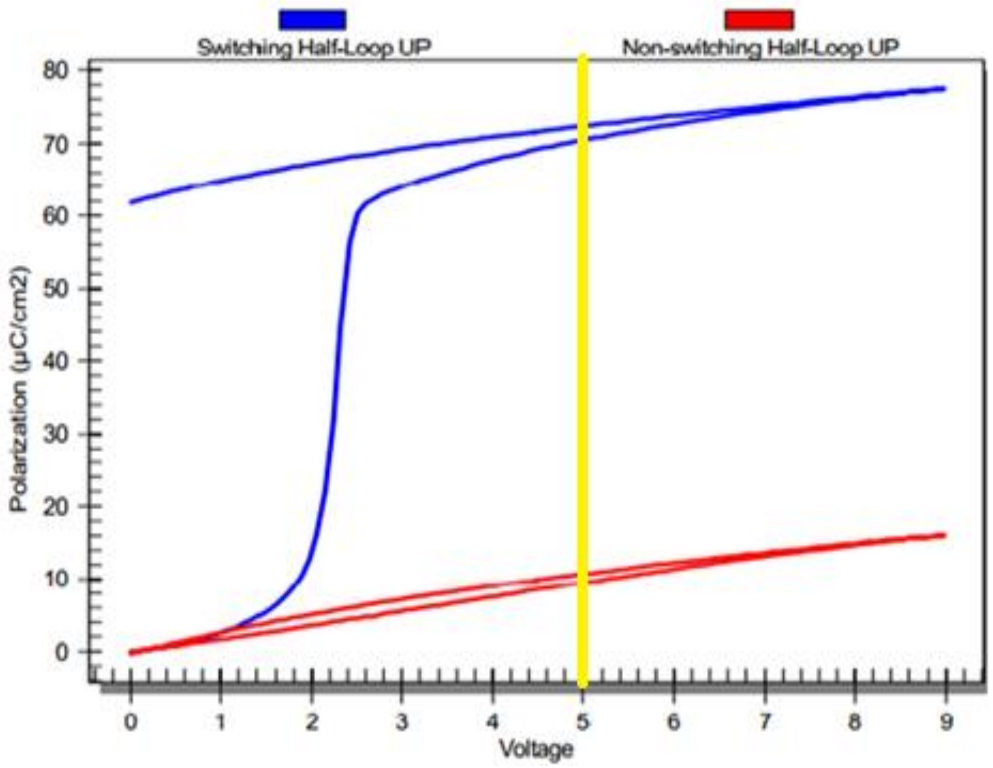

Figure 5.5: Switching and non-switching polarizations of the AB white capacitor [30]

Figure 5.5 shows the switching hysteresis half loop of the AB white ferroelectric capacitor in blue whereas the non-switching hysteresis loop is represented in red. The working range of the can be deduced from these loops as follows.

The absolute charge generated by the by the AB white ferroelectric capacitor for a 5V applied voltage

Switched State to represent data '0' $= 70\mu C/cm^2 * 0.001cm^2 = 7nC$

Non-switched State to represent data '1' $= 9\mu C/cm^2 * 0.001cm^2 = 0.9nC$

The value of the sense capacitance should be chosen so that for the switched state should turn ON T_1 and the non-switched state should turn it OFF. For a sense capacitance of 1.39 nF the voltage generated for the two states of the ferroelectric capacitor can be calculated as

Switched State = 7nC/1.39nF = 5.04 V > V_t = 0.7 V => Output low (data '0')

Non-Switched State = 0.9nC/1.39nF = 0.65 V < V_t = 0.7V => Output high (data '1')

F. Retention Testing

Further characterization of the autonomous non-volatile ferroelectric memory latch was done by carrying out retention analysis for a range of sense capacitors [33]. As seen in Figure 5.6 the retention times are represented on the y-axis and the sense capacitance range for which retention was measured is represented in the x- axis. The values represented by red dots are actual measured retention times. Since the measurements of retention times exceeding two weeks was not practical we developed an empirical mathematical model based on our actual measured values, the decay rate of polarizations in the ferroelectric capacitor and also the effective capacitance ratio of the ferroelectric capacitor and the sense capacitor that is required to ensure the device functionality [34]. The blue curve is the retention times predicted by the mathematical model.

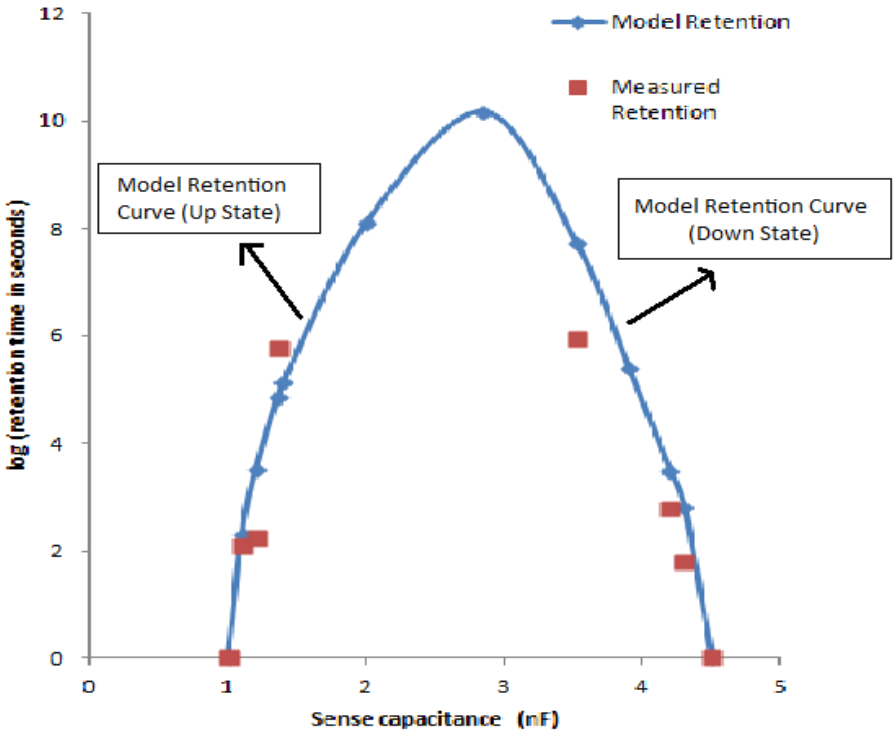

Figure 5.6: Retention time Vs Sense capacitance

$$\text{Model Retention [UP]} = \frac{\text{Ps[UP]} - (\text{Threshold Ratio} * \text{Csense})}{\text{Decay Rate}} \quad 5.1$$

$$\text{Model Retention [DOWN]} = \frac{\text{Ps[DOWN]} - (\text{Threshold Ratio} * \text{Csense})}{\text{Decay Rate}} \quad 5.2$$

Model retention is measured in log (retention time in seconds). Polarizations are measured in μC/cm^2. While the Decay rate is in polarization per decade of log. The Threshold Ratio is the ratio of C_{data} / C_{sense} that allows the Latch to operate properly. The Decay rate of the capacitance state is 0.33333 polarizations per decade of log.

Equations 5.1 and 5.2 are those which were used to formulate the mathematical model in Microsoft Excel. Equation 5.1 is the curve on the left hand side where the ferroelectric capacitor is in the UP, un-switched state which is when data '1' can be

written to the latch. While curve on the right is the representation of Equation 5.2 where the capacitor is in it's DOWN, switched state which is when data '0' is written to the latch. From experimental data, it was noted that data '1' could not be written to the latch for values of the sense capacitor below 1.1 nF. In the same fashion, data '0' could not be written to the latch for values of the sense capacitor above 4.5 nF. The two curves were made to intersect so that for any point under the curve the device would retain both data '0' and data '1'.

CHAPTER VI

CONCLUSION

This thesis introduced and analyzed the concept of autonomous memory operation using the ferroelectric capacitance theory. It began by reviewing the history of ferroelectrics along with its characteristic properties of polarization and hysteresis. Then, the ferroelectric capacitor was differentiated from the linear and paraelectric counterparts on the basis of its non-linear charge when subjected to an external electric field. The measurement of the amount of charge flow in a ferroelectric capacitor when electrically pulsed was also reviewed.

The packaging and internal structure of the AB white capacitor developed by Radiant Technologies Inc., was explained. Further, the electrical properties of the capacitor was analyzed using Vision 4.6.0 testing package which included Hysteresis measurement of switched and non-switched remnant polarization, calculation of effective capacitance, total number of dipoles and di-electric capacitance using experimental data. Measurements of the ferroelectric capacitor's polarization data taken at different delay time intervals were also presented.

After reviewing the characteristics of the AB white capacitor, the design of the non-volatile autonomous ferroelectric memory latch was discussed in different stages. The importance of using the AB white ferroelectric capacitor for the development of the latch was also explained thoroughly. Once the design was set up, the device functionality was examined by performing READ and WRITE operations. The crucial voltages involved in the READ and WRITE cycles were also elaborated. Experimental data for successful READ and WRITE were also expounded.

Further, electrical characterization of the memory latch was carried out by analyzing the voltage ranges for its write enable and input voltages. The working range of the sense capacitor used in the Sawyer tower component of the latch was also determined using experimental research. Finally, the data retention with respect to a range of sense capacitances was also characterized and predicted.

Future research shall include the precise calculation of the data retention properties for the studied ferroelectric memory latch using a mathematical model. The device can also be studied under different temperature profiles. Specifically, retention measurements of the device at elevated temperatures may allow predictions of retention performance under normal operating conditions. Potential applications of this device in harsh environments which include aerospace, industrial and automotive can also be studied.

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