4-27-2023

On Synchronizing Many Solvable Chaotic Oscillators

Sidney Lovelady

Title:

by

Name:

An Honors Capstone

submitted in partial fulfillment of the requirements

for the Honors

to

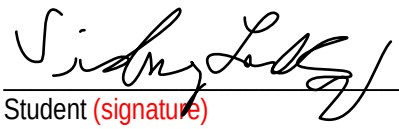
The Honors College

of

The University of Alabama in Huntsville

Honors Capstone Director:

Program Director:



Student (signature) Date

Director (signature) Date

Department Chair (signature) Date

Honors College Dean (signature) Date

HONORS COLLEGE
THE UNIVERSITY OF ALABAMA IN HUNTSVILLE

Honors College
Frank Franz Hall
+1 (256) 824-6450 (voice)
+1 (256) 824-7339 (fax)
honors@uah.edu

Honors Thesis Copyright Permission

This form must be signed by the student and submitted with the Capstone manuscript.

In presenting this thesis in partial fulfillment of the requirements for Honors Diploma or Certificate from The University of Alabama in Huntsville, I agree that the Library of this University shall make it freely available for inspection. I further agree that permission for extensive copying for scholarly purposes may be granted by my advisor or, in his/her absence, by the Chair of the Department, Director of the Program, or the Dean of the Honors College. It is also understood that due recognition shall be given to me and to The University of Alabama in Huntsville in any scholarly use which may be made of any material in this thesis.

_____

Student Name (printed)

Student Signature

_____

Date

On Synchronizing Many Solvable Chaotic Oscillators

Sidney Lovelady, *Member, IEEE*

***Abstract*—We present efforts toward the synchronization of many solvable chaotic oscillator circuits. Seminal work on experimental chaotic oscillator circuits has shown that although these systems are practically unpredictable, they surprisingly are capable of synchronization in several fashions when they are coupled in networks. These types of systems have historically exhibited interesting dynamical behaviors such as Arnold tongues and oscillator death. However, when these networked populations consist of chaotic oscillators, the dynamics of both the collective network and the individual oscillator nodes generally do not allow closed-form analytic solutions. Here, we build a network of coupled solvable chaotic oscillators where individual nodes permit closed-form solutions and have enabled closed-form solutions for network behavior and parameters in specific configurations. These synchronization experiments are significant extensions of a senior design project designed to meet UAH's Honor's Capstone requirements. Further, the simulation, design, and fabrication of these oscillator circuits supported an Electrical Engineering senior design team with the goal of creating chaotic oscillator-based beacons that are capable of attracting Braitenberg vehicles. By exploiting the solvable nature of these chaotic oscillators, the vehicle beacon may be hidden by blending in with surrounding audio noise. Interestingly, the vehicles are designed to detect these hidden signals resulting in tracking schemes. In the work presented here, we show an audio frequency chaotic oscillator circuit with both SPICE simulation and hardware results for the synchronization of a population of three oscillators. We find that the oscillators synchronize in three modes with varying coupling strengths.**

***Index Terms*—Chaos, Solvable Chaos, Chaotic Networks, Synchronization**

I. Introduction

With congestion of the electromagnetic spectrum in the last twenty years comes a litany of issues related to multi-user broadcast reception and security. Current technologies in radio communications attempts to remedy these issues with spread spectrum broadcasting [1] and the use of wideband signals [2]. Many of these schemes rely on synchronization and in one of the most influential findings in the field of nonlinear dynamics, it was shown that remarkably, chaotic systems are capable of synchronization [3]. The synchronization of chaotic systems also has a range of applications in securing communications [6]. While special types of solvable chaotic waveforms have been proposed to solve these issues - thanks to the the advent of specially solvable chaotic systems and their accompanying matched filters [3], [4] - these chaotic systems demonstrate interesting behavior when coupled via bidirectional links [4]. These links, practically, can take the form of transducers, transmission lines, or simple resistors [5].

Sidney Lovelady is with the Electrical & Computer Engineering Department at the University of Alabama in Huntsville, scl0014@uah.edu

Electronic systems tend to couple despite efforts to minimize unwanted environmental influence [7]. Although chaotic systems are random [9], [8], when they couple they are capable of various states of synchronization [5]. Synchronization may or may not add benefit to engineering design and is an important property to study as chaos is considered for applications in communication [10], [11], [13], [14], sonar [16], radar [12], joint radar-communication systems [20] and even as test structures for conventionally engineered systems [9], [15]. As efforts are made to find new chaotic systems [19], extend the bandwidth of existing chaotic systems [17] and stabilize periodic orbits via chaos control [18], the importance of understanding and observing chaotic synchronization grows. This is especially true as it has been recently shown that truly random chaotic systems can be implemented in hybrid analog/digital modes on FPGAs [21] where these systems may exhibit long-range pulse coupling [22]. Interestingly, other nonlinear systems have been shown to perform computation and information via their synchronization capability [23], [24], [26] and also show capacity for chaotic behavior [25].

In general, chaotic systems are highly sensitive to initial and operating conditions, thus making synchronizing many "sources" intended to operate in conjunction (say, multiple satellites in different locations meant to broadcast the same signal) seem impracticable. This is because the starting and continual operating conditions for these systems cannot be guaranteed to be identical. However, by exploiting these systems' properties of bidirectional synchronization by various means, we can obtain an effect similar to starting these systems with a guarantee of similar initial and operational conditions. for prolonged durations.

Previously, it has been shown that by simply connecting two of these chaotic oscillators (as shown in Fig. 1) via varying resistance values, synchronicity can be achieved in a repeatable and verified via closed-form solution [4]. Here, we show the effect of a bidirectional resistive link (as shown in Fig. 2) between three of these special oscillators, along with the effect on catch-up times and reliability of the synchronization as the resistance of these links varies. This experiment was conducted using both simulation in LTSpice and in hardware via PC Boards designed to support an undergraduate Electrical Engineering senior design project.

II. Background

The solvable chaotic oscillators that were designed and manufactured for this project can be seen in Fig. 1. These oscillators utilize an unstable, negative-RLC tank circuit paired

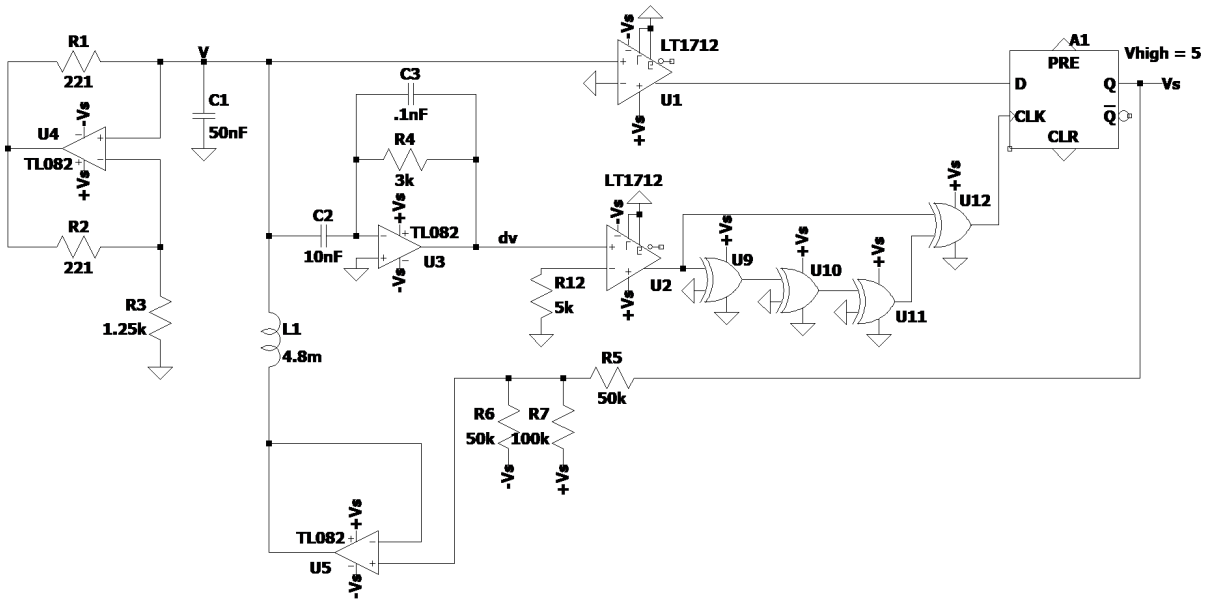


Fig. 1. Schematic of a 10kHz solvable chaotic oscillator circuit in LTSpice. Here, node "V" represents the chaotic signal.

with a guard condition that imposes a forcing function which keeps the oscillations within bounds of roughly $\pm$2V as the -RLC circuit rings around $\pm$1V upon transitions. The oscillator's -RLC circuit consists of a negative resistor (R1-3, U4), a capacitor (C1), and an inductor (L1). Each component here is sized appropriately to set the bandwidth of the chaotic signal that spans from D.C. to 10kHz.

The remainder of the circuit is a feedback loop. Here, the signal V is quantized by a comparator and results in a digital signal that indicates zero-crossings (via comparator U1). Meanwhile, V is simultaneously differentiated (by a differentiator circuit at U3) into dV, where dV is results in an impulse train (via U2 and U9-12). These short impulses that correspond to the zero-crossings of dV (i.e. local maxima/minima of V) act as clock triggers for the D-flip flop (A1) which, when fed in V's digital signal counterpart, outputs a digital signal (Vs) that corresponds to the crossing of the zero-volt threshold. Based on the direction of said crossing, Vs will be either +5V (for - to + crossing) or 0V (+ to - crossing). These conditions are then converted into a sign function ($\pm$1V) via the resistive ladder R5-7 and fed back into the -RLC loop via a buffer amplifier (U5).

This somewhat unassuming system creates extremely complex behavior, but in a solvable way [3]. When implemented practically, however, such a system's high sensitivity to initial conditions along with manufacturing tolerances and operational conditions introduce practically incalculable voltage fluctuations as time progresses. But, when coupled via bi-directional links, these practical oscillators (which when apart normally become unsynchronized within milliseconds) exhibit a catch-up behaviour, where the speed and sustainment of synchronicity depends on the strength of the coupling. Previous research by Tamseel Mahmood Syed and Dr. Aubrey Beal has modeled the synchronicity of two of these chaotic systems and proven its viability [4] for the case of two coupled oscillators. This paper, however, will take their work and scale it to three oscillators to examine phenomena that may be exclusive nth-degree synchronicity, especially with regards to the "star" shaped resistive bidirectional link shown in Fig. 2.

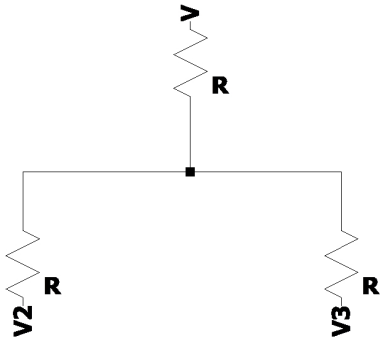


Fig. 2. Star-type resistor ladder with equal R, for even loading.

III. Simulations

Simulations for this experiment were performed in LTSpice XVII using three models that closely relate to the PC Board designed for the aforementioned senior design project. In order to synchronize three of the oscillators from Fig. 1, a bidirectional resistor formation (Fig. 2) was used to even loading on the chaotic input/output nodes (hereby denoted as v-nodes), which will aid in synchronicity. Initial conditions for the three oscillators are slightly different to represent the oscillators in an random state at time zero and are listed in

Table 1. Resistor values of 100Ω, 500Ω, 1kΩ will be tested and synchronization of the three oscillators' nodes are displayed in Fig. 5-7. Results for this simulation portion of this experiment are discussed in the *Simulation Results* section below.

Table 1 - ICs			
IC	Osc. 1	Osc. 2	Osc. 3
I(L)	0	0.01	-0.01
V(dv)	0	0.00382	0.003
V(vs)	5	4.992	5.027
V(v)	0.1	0.2	0.10041

IV. PC Boards Experiment

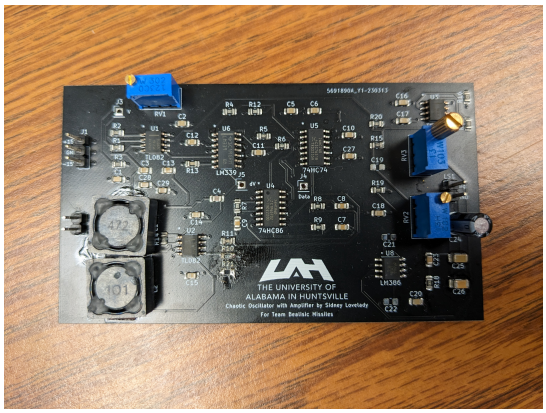


Fig. 3. 10kHz solvable chaotic oscillator PC Board. Designed in KiCad 6.0 and manufactured at JLCPCB

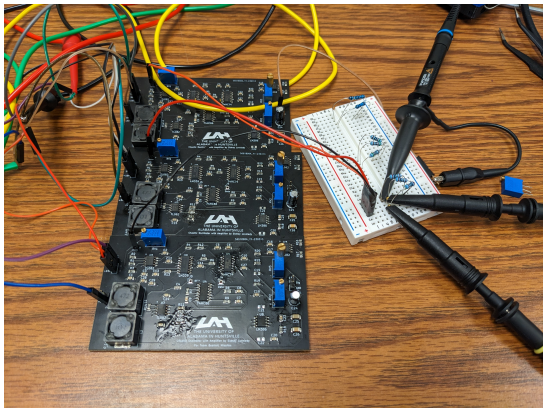


Fig. 4. Synchronization experiment setup. Three oscillators (left) and breadboard with the three resistor ladders tested in this experiment (right).

A prefabricated PC Board design of the oscillator circuit above was created and manufactured for the aforementioned senior design project (Fig. 3). Three of these boards underwent synchronization testing during this experiment. The boards in this experiment were powered by a Keithley 2231A-30-3 isolated triple-channel DC power supply, where +15V, -15V, and +5V were split evenly between the circuits. Waveforms were observed and saved on a Tektronix TBS2000 quad-channel digital oscilloscope. The three values of resistor ladders from the simulation section were implemented on a breadboard for quickly switching between ladders during testing. The bidirectional v-nodes were tied to 3 male pin headers which were taped together for as accurate as possible transient analysis. The ability to easily and repeatably dis/reconnect the v-nodes allowed ample time for "random" initial conditions to build within the oscillators before connecting them to the resistor ladder. These connections were made several times throughout testing to ensure results were repeatable and accurate. The lab setup for this experiment can be viewed in Fig. 4. Results for this PC Board section are discussed in the *Hardware Results* section below.

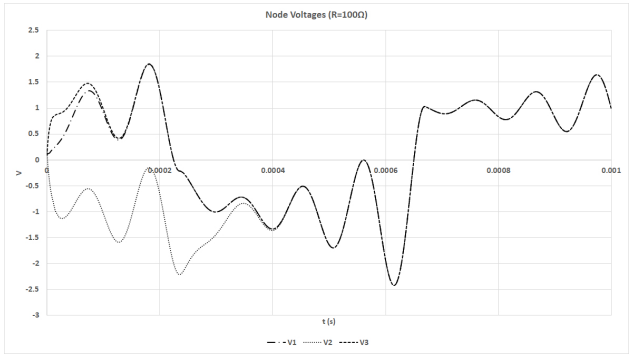


Fig. 5. Node Voltages for R=100. Notice V1 and V3 catch up in below 0.2ms while node V2 takes double the time to synchronize with the group.

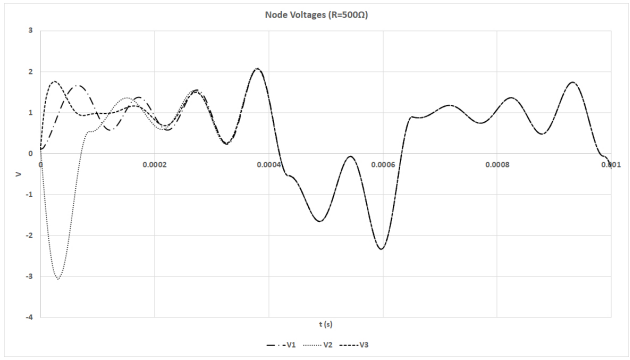


Fig. 6. Node Voltages for R=500. Notice similar catch-up times between all nodes.

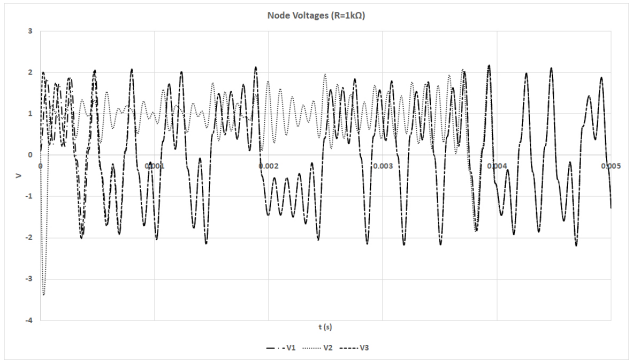


Fig. 7. Node Voltages for R=1k. Notice the much longer catch-up time with node V2, while V1 and V3 synchronize almost instantly.

V. Results

A. Simulation Results

SPICE simulation provided the data in Figures 5-7 which show the synchronization results of the chaotic oscillator network population from Fig. 1's circuit with varying resistor values on the star-ladder. In Fig. 5, the 100Ω ladder allows for total synchronization among the three lines in roughly 0.4ms. In the 500Ω run (Fig. 6), it is shown that full synchronization is achieved around 0.1ms quicker than the 100Ω run, in total around 0.3ms. The discrepancy here is likely due to loading effects on the v-nodes incurred by the low 100Ω resistance (notice how peak voltage is lower in the 100Ω test vs. the 500Ω test). This loading effect seemed to slow down catch-up behavior. The 1kΩ results in Fig. 7 are more in line with expectations due to much lower loading, pushing the total synchronization time for all three lines back to nearly 4ms, indicating that the relationship between these resistive couplings and synchronization times are likely related nonlinearly.

B. Hardware Results

Time-series results from the PC Board synchronization tests were surprising in lieu of the simulations. After a number of connects and disconnects from the three unsynchronized oscillators to the resistive ladders, time-series data of the three oscillators (Fig. 8-10) shows they are synchronized almost instantaneously. This result is surprising given that the oscillators uncoupled for a long enough time to desynchronize from each other, however this process was repeatable. This seemingly immediate synchronization could be due to imperfect connections to the resistor ladders (intended to act as transient analysis with random IC's) and/or capacitive interference from the oscilloscope probes. This phenomena is a future topic of research.

In Fig. 8 another surprising result was found; a seemingly unprovoked amplitude "desynchronization", yet with signals remaining in phase lock between all three lines. This phenomenon was not unique to the 100Ω ladder, as it also shows up in the 1kΩ ladder's transient as well. In fact, it showed up in all three resistor ladders in seemingly random locations and times during the test runs. The Appendix contains a collection of these "desynchronization" events captured in steady-state analysis, ranging from only amplitude to complete amplitude and phase desynchronization. Steady-state captures of these desynchronization events (Fig. 13-18) showed that they occurred more frequently and lasted longer in proportion to increasing the resistance of the coupling lines. In an effort to validate this behaviour, four XY Mode plots were made (Fig. 19-22) to test the tendency and to what degree these desynchronization events occurred between nodes V1 and V2. Fig. 19 shows the nodes completely unsynchronized (R=∞), Fig. 20 shows them in the 100Ω ladder, Fig. 21 in the 500Ω ladder, and Fig. 22 in the 1kΩ ladder. Notice the increase in deviations from tangent as resistive load increases, marking the notable increase in desynchronization events. These deviations and how to alleviate them are another excellent topic of future research.

It should be noted that these events did not correspond with circuit disturbance, as the steady-state desynchronization events occurred with no physical touching of the connectors or circuit in any way. Since these chaotic systems are highly dependent on starting and operating conditions, it can be reasonably postulated that these events were caused by some parameter or dynamical mismatch/disturbance. A few possible sources of interference that may contribute to these desynchronization events include electromagnetic interference, either from the mains supply to the DC source and/or oscilloscope, and slight electrostatic discharge, although the latter is unlikely. β-values (also known as growth factors in chaotic systems [4]) for each board were also controlled for and ensured equal before testing, however we note that these systems are exponentially sensitive to any non-zero mismatch in this parameter. Even though the oscillators were manufactured with tight component tolerances, the PC Boards themselves are not perfect, as each component has a slight variance in its rated value that could contribute to this unpredictable behavior.

VI. Conclusion, Discussion and Future Work

In this paper, we show the synchronicity of three 10kHz solvable chaotic oscillators designed for use in an Electrical Engineering senior design project. While some dynamical behavior or unintentional interference may introduce desynchronization events, the overall synchronization of the circuits can easily be retained for significant periods of time via the bidirectional, resistively-coupled links introduced in this experiment. We also conclude that higher resistance links decrease the ease of synchronization and increase the chances of desynchronization events occurring. Resistance values must be chosen carefully to reduce loading effects, but not so much so that the synchronization loses long-term stability. Future work includes better methods of transient analysis, interference deterrence to minimize the chances of desynchronization events from occurring, more effective linking mechanisms between the oscillators, and higher degrees of oscillator synchronization.

Acknowledgment

The author would like to thank Dr. Aubrey Beal for providing the opportunity to study this phenomena and Sidni Hale for his gracious funding for the senior design project this paper supports. This work was performed in the support of and with significant extension to an Electrical Engineering senior design project with Team Bealistic Missiles.

References

[1] S. Hengstler, D. P. Kasilingam and A. H. Costa, "A novel chirp modulation spread spectrum technique for multiple access", *IEEE Seventh Int. Symp. on Spread Spectrum Techniques and Applications*, vol. 1, pp. 73-77, 2002.

[2] P. Ramabadran, S. Madhuwantha, P. Afanasyev, R. Farrell and J. Dooley, "Wideband interleaved vector modulators for 5g wireless communications", *2018 IEEE MTT-S Int. Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G)*, pp. 1-3, 2018.

[3] Pecora, Louis M., and Thomas L. Carroll. "Synchronization in chaotic systems." Physical review letters 64.8 (1990): 821.

[4] N. J. Corron, M. T. Stahl and J. N. Blakely, "Exactly solvable chaotic circuit," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, France, 2010, pp. 1356-1359, doi: 10.1109/ISCAS.2010.5536943.
[5] T. M. Syed, D. R. Oh and A. N. Beal, "Synchronizing Solvable Chaotic Oscillators," SoutheastCon 2021, Atlanta, GA, USA, 2021, pp. 1-4, doi: 10.1109/SoutheastCon45413.2021.9401842.
[6] Qu Shaocheng, Wang Xiaoyan and Gong Meijing, "Synchronization of unified chaotic systems and application to secure communication," 2008 27th Chinese Control Conference, Kunming, 2008, pp. 370-373, doi: 10.1109/CHICC.2008.4605825.
[7] Dean, Robert, et al. "Microfibrous metallic cloth for acoustic isolation of a MEMS gyroscope." Industrial and Commercial Applications of Smart Structures Technologies 2011. Vol. 7979. SPIE, 2011.
[8] Rashid, Md Imtiaz, et al. "True random number generation using latency variations of FRAM." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 29.1 (2020): 14-23.
[9] Beal, Aubrey N., et al. "A random stimulation source for evaluating MEMS devices using an exact solvable chaotic oscillator." Additional Papers and Presentations 2015.DPC (2015): 001594-001625.
[10] Beal, Aubrey N., et al. "Design and simulation of a high frequency exact solvable chaotic oscillator." MILCOM 2012-2012 IEEE Military Communications Conference. IEEE, 2012.
[11] Bailey, J. P., et al. "High-frequency reverse-time chaos generation using digital chaotic maps." Electronics Letters 50.23 (2014): 1683-1685.
[12] Beal, A. N., et al. "High frequency oscillators for chaotic radar." Radar Sensor Technology XX. Vol. 9829. SPIE, 2016.
[13] Bailey, J. Phillip, et al. "A digital matched filter for reverse time chaos." Chaos: An Interdisciplinary Journal of Nonlinear Science 26.7 (2016): 073108.
[14] Beal, Aubrey N., et al. "Generating and detecting solvable chaos at radio frequencies with consideration to multi-user ranging." Sensors 20.3 (2020): 774.
[15] Syed, T. M., et al. (2020, November). Solvable chaos as a tool for evaluating wideband delay cells in matched filters. In 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS) (pp. 1-4). IEEE.
[16] Syed, T. M., et al. "Drastically reduced sensor hardware for solvable chaos-based sonar." Electronics Letters 58.21 (2022): 810-812.
[17] Beal, Aubrey N., et al. "Extended-bandwidth negative impedance converters by nested networks." IEEE Transactions on Circuits and Systems II: Express Briefs 65.9 (2018): 1134-1138.
[18] Beal, A. N., et al. "Stabilizing Long-period Orbits in Chaotic Oscillators with Open-source Hardware." 2020 SoutheastCon. IEEE, 2020.
[19] Corron, Ned J., et al. "Exact analytic solution for a chaotic hybrid dynamical system and its electronic realization." Chaos: An Interdisciplinary Journal of Nonlinear Science 30.7 (2020): 073112.
[20] Pappu, Chandra S., et al. "Chaos based frequency modulation for joint monostatic and bistatic radar-communication systems." Remote Sensing 13.20 (2021): 4113.
[21] Beal, A. N., et al. "Driven ring oscillators as FPGA entropy sources." 2019 SoutheastCon. IEEE, 2019.
[22] Cohen, Seth D., et al. "Long-Range Pulse Interactions in Unclocked FPGAs." IEEE Access (2023).
[23] Li, XiaoFu, et al. "A four-state adaptive Hopf oscillator." Plos one 16.3 (2021): e0249131.
[24] Li, XiaoFu, et al. "Stochastic effects on a Hopf adaptive frequency oscillator." Journal of Applied Physics 129.22 (2021): 224901.
[25] Xiaofu, L. İ., et al. "Chaos in a Pendulum Adaptive Frequency Oscillator Circuit Experiment." Chaos Theory and Applications 5.1 (2023): 11-19.
[26] Li, XiaoFu, et al. "Field-programmable analog array (FPAA) based four-state adaptive oscillator for analog frequency analysis." Review of Scientific Instruments 94.3 (2023): 035103.

APPENDIX
FURTHER IMAGES

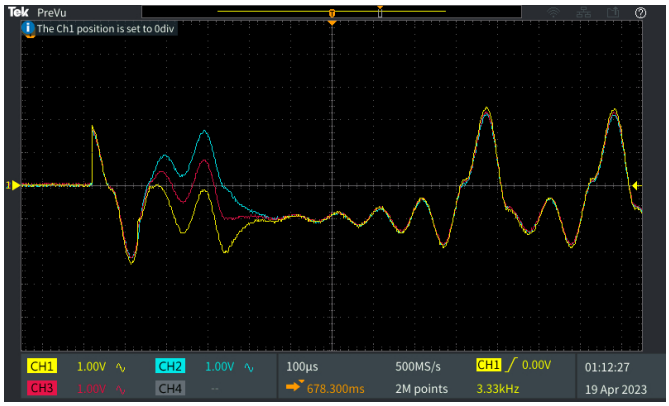


Fig. 8. 100Ω ladder PCB transient synchronicity test. Notice seemingly instantaneous synchronization on connection followed up by a short amplitude desynchronization on all three nodes.

Fig. 9. 500Ω ladder PCB transient synchronicity test. Notice similar synchronization upon time zero. No visible desynchronization events.

Fig. 10. 1kΩ ladder PCB transient synchronicity test. Notice instant synchronization followed by a major fall-out of phase and amplitude synchronicity, which then begin to resychronize at the end of the screenshot.

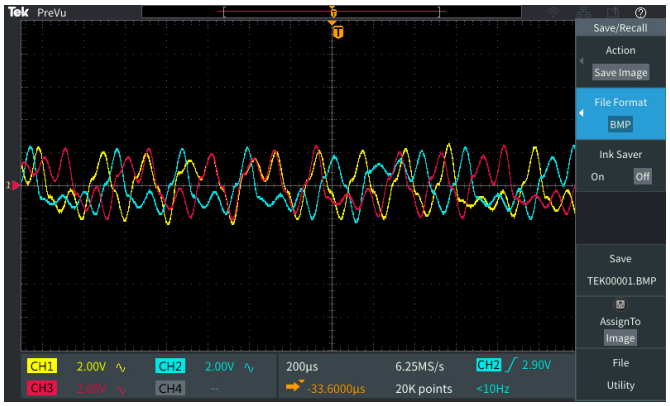


Fig. 11. Three unsynchronized oscillators for R=∞. This state was enforced between synchronicity transient analysis tests by disconnecting nodes V1-3 from the resistor ladder.

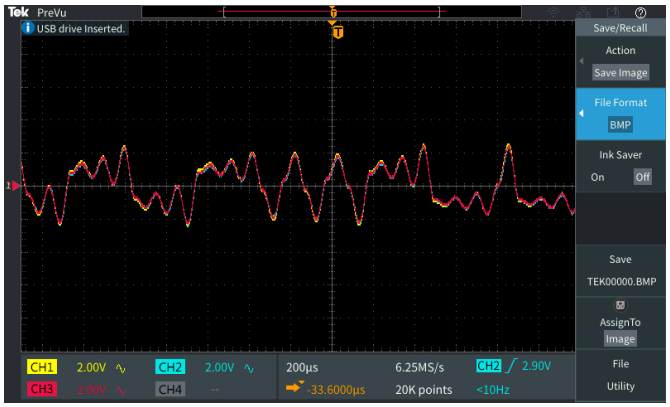


Fig. 12. Three synchronized oscillators. An example of how we expect nodes V1-3 to behave depending on the strength of their coupling.

Fig. 13. 100Ω ladder steady-state: ”medium” desynchronization event. Notice how the discontinuity is similar in shape to the other nodes, indicating a mild amplitude desynchronization.

Fig. 14. 100Ω ladder steady-state: multiple ”short” desynchronization events. Notice the lack of similarity to other waveforms, indicating a complete jump out of synchronicity.

Fig. 15. 500Ω ladder steady-state: ”short” complete desynchronization event

Fig. 16. 500Ω ladder steady-state: multiple ”short” complete desynchronization events

Fig. 17. 1kΩ ladder steady-state: ”medium” complete desynchronization event

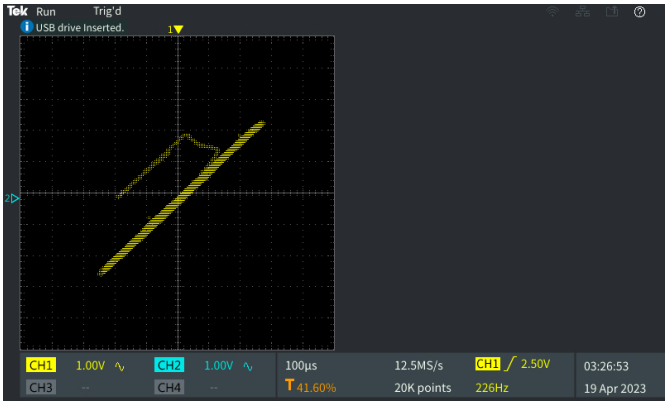


Fig. 20. 100Ω ladder in XY Mode (X=V2, Y=V1): Notice the single deviation off the slope in the middle. This indicates a desynchronization event in relation to the two channels being compared.

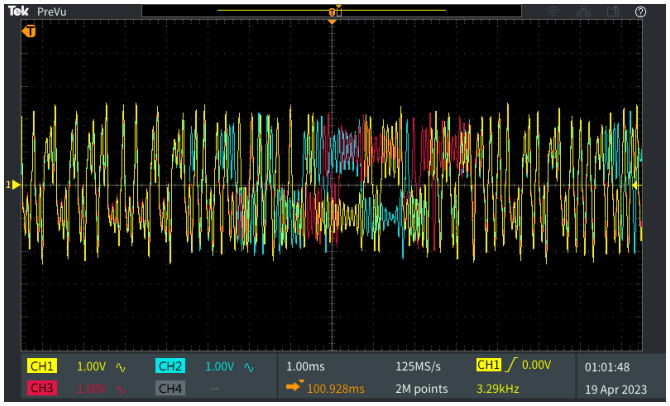


Fig. 18. 1kΩ ladder steady-state: ”long” complete desynchronization event

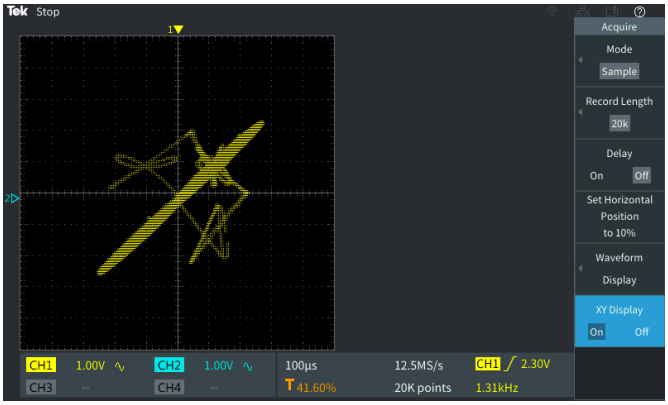


Fig. 21. 500Ω ladder in XY Mode (X=V2, Y=V1): Notice more symmetrical deviations off the middle slope. This indicates stronger ”jumps” out of synchronicity that last for longer periods of time. The symmetry indicates that the discontinuity lasts long enough to allow it to oscillate around zero independently of the other node being compared.

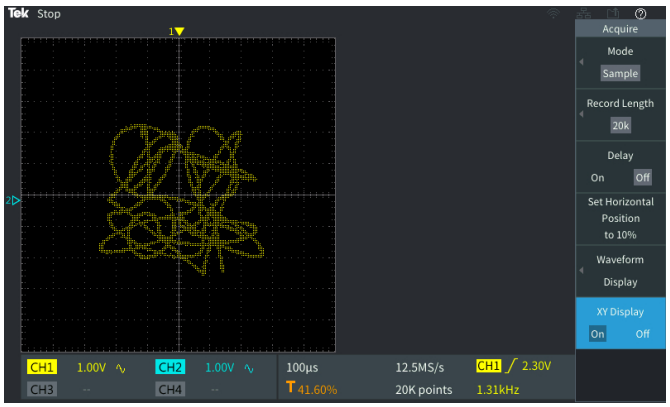


Fig. 19. XY view of two unsynchronized v-nodes (X=V2, Y=V1)

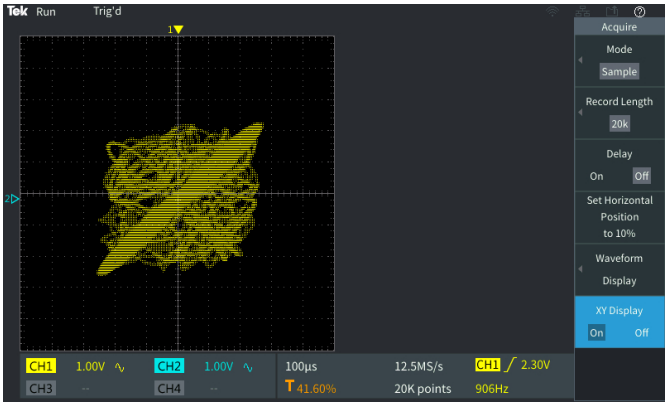


Fig. 22. 1kΩ ladder in XY Mode (X=V2, Y=V1): Notice the many deviations off-tangent, indicating plentiful, strong, and long-lasting desynchronization events.